Fusion Starter Kit

User's Guide

Actel®

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Introduction

Thank you for purchasing the Actel Fusion Starter Kit.

This guide provides the information required to easily evaluate the Fusion devices.

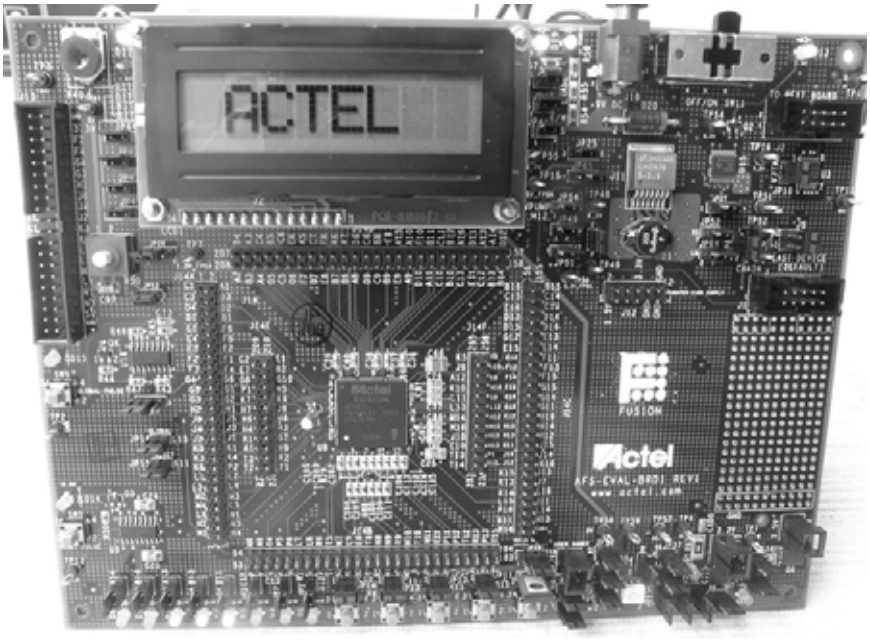

Figure 1. The Fusion Evaluation Board

Document Contents

Chapter 1 – "Contents and System Requirements" describes the contents of the Fusion Starter Kit.

Chapter 2 – "Hardware Components" describes the components of the Fusion Evaluation Board.

Chapter 3 – "Setup and Self Test" describes how to setup the Fusion Evaluation Board and how to perform a self test.

Chapter 4 – "Description of Test Design" describes the existing design on the Fusion Evaluation Board.

Chapter 5– "Test Procedures for Board Testing" details the test procedure to be carried out at the Actel designated manufacturer's testing facility on the Fusion Evaluation Board with silkscreen labeling AFS-EVAL-BRD-1 REV1.

Appendix A – "FG256 Package Connections for AFS600 Devices" provides a table listing the board connections.

Appendix B – "Board Schematics" provides illustrations of the Fusion Evaluation Board.

Appendix C – "Signal Layers" provides illustrations for the six signal layers of the Evaluation Board.

Appendix D– "Product Support" describes Actel support services.

Document Assumptions

This user's guide assumes the following:

- You intend to use Actel Libero IDE software.
- You have installed and are familiar with Actel Libero IDE v7.0 SPa or later software.
- You are familiar with PCs and the Windows operating system.

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Contents and System Requirements

This chapter details the contents of the Fusion Starter Kit and lists the power supply and software system requirements.

Starter Kit Contents

The starter kit includes the following:

- Fusion Evaluation Board
- Libero IDE Gold
- FlashPro v4.1
- CD with design examples
- Switching brick power supply (rated from 110 V to 240 V AC) from 50 Hz to 60 Hz input, providing 9 V DC output at up to 2 A, part number DTS090220U-P5P-SZ from CUI INC. A RoHS compliant, lead-free, version of this Power supply will be shipped with all kits very shortly.

For the CD contents, review the *ReadMe.doc* file at the top level of the CD.

2 Hardware Components

This chapter describes the hardware components of the Fusion Evaluation Board.

Fusion Evaluation Board

The Fusion Evaluation Board consists of the following:

- Wall mount power supply connector, with switch and LED indicator
- Jumpers to select either 1.5V or 3.3V for I/O Bank0 or Bank1
- 10-pin 0.1 inch pitch programming connector compatible with Altera connections
- 40 MHz oscillator and two independent manual clock options for global reset and pulse
- Eight LEDs (driven by outputs from the device)
- Jumpers (allow disconnection of all external circuitry from the FPGA)
- Two monostable pulse generator switches ("global" and "reset")
- Four switches (provide input to the device)
- Potentiometer for variable analog input
- Large LCD alphanumeric display to facilitate detailed message outputs from the FPGA application
- Multicolor LED for illustrating PWM fan control and temperature measurement
- 1.5V and 3.3V MOSFET driven fan control circuits with shrouded headers for external fans

For further information, refer to the following appendices:

Appendix A – "FG256 Package Connections for AFS600 Devices" on page 33.

Appendix B – "Board Schematics" on page 47.

Detailed Board Description and Usage

The Fusion Starter Kit board has various advanced features that are covered in later sections of this chapter. Note that the AFS600-FG256 Actel FPGA is soldered directly to the board. The Fusion architecture provides access to a one-chip Flash FPGA solution containing both analog and digital components, including a built-in Flash drive. The Fusion Starter Kit board is available only in a directly soldered configuration. Socketed configurations are not available.

Full schematics are available on the Starter Kit Tutorial CD supplied with the Starter Kit or from the Actel website. The electronic versions of the dedicated schematics can be enlarged to a far greater degree than can be shown in the printed version of this manual or even in the electronic version of this manual, hence the interested reader is referred to the dedicated schematics to see the appropriate level of detail.

Power Supplies

A 9 V power supply is provided with the kit. There are two power supply components for the FPGA in the starter kit board to provide 1.5 V and 3.3 V to the Fusion FPGA. An additional +5 V voltage bank is provided for use by the LCD display module and for use in illustrating an analog voltage input to the analog aspects of the Fusion board.

The external +9 V positive center power supply provided to the board via connector J18 goes to a voltage regulator chip U11 on the evaluation board. This regulator has been protected against reverse supply voltage being applied by a reverse polarity protection diode. As soon as the external voltage is connected to the board, the red "power applied" LED (D19) (the only red LED on the board) illuminates to indicate that an external supply has been connected to the board. As soon as switch SW11 is moved to the ON position (to the right, as labeled on the board "OFF/ON") the disabling ground signal is removed from pin 7 of U11 and the regulator begins to provide power at its output.

The U11 switching voltage regulator provides a dedicated 3.3 V supply at its output. The board's 3.3 V supply is used for feeding a separate regulator that delivers 1.5 V (via U15). Although all Fusion FPGAs can also support 1.8 V– and 2.5 V–based I/O standards, these voltages are not provided on the Fusion Starter Kit board. The 1.5 V supply is required for the core voltage of the Fusion family and the 3.3 V supply is required for extended I/O bank capability, such as LVTTL. The presence of these voltages is indicated by two yellow LEDs (D13 for 1.5 V and D11 for 3.3 V) located at the top right of the board. Each LED is labeled with the voltage it represents and its component identifier. Both voltages are selectable on the I/O banks 0 and 1 (the two northernmost banks on a Fusion device). (Note that only the larger Fusion devices (AFS600 and AFS1500) have 5 I/O banks.)

The 3.3 V supply is also used for optionally providing the VPUMP programming voltage. This VPUMP voltage may be provided to the chip during programming by applying a FlashPro3 programmer to the J1 interface and selecting VPUMP from the FlashPro v4.1 (or later) programming software and may also be provided directly to the chip from the board. The user simply leaves the JP54 jumper in place to apply the 3.3 V supply to the VPUMP pin M12 of the FG256 packaged FPGA. Note that if both FlashPro3 and the board are selected to provide VPUMP then it is the connection on the board that will override as FlashPro3 will detect that a voltage is available, issue an information message in the programming software, and then move its VPUMP output pin to a tristate value, allowing the board to provide all the power.

Note also that the board must be powered up during programming, as the chip's core voltages must be provided and VJTAG must be detected by the FlashPro3 programmer before it can set its JTAG signal voltages to the right level. The value of VJTAG can be set to 1.5 V or 3.3 V on the board by setting the position of jumper JP27 to join pins 1 and 2 for 1.5 V and join pins 2 and 3 for 3.3 V. It is recommended that VJTAG be left to 3.3 V on the Fusion board because an interboard buffer chip is used that has limited low-voltage capability and needs the higher setting of 3.3 V to ensure good signals at the output of the buffer chip array U3.

Note that the LCD has its own dedicated 5 V power supply, all components of which, including the regulator U20, are mounted on the circuit board underneath the LCD module. A yellow LED (D17) representing the 5 V supply availability is positioned at the top left of the board.

The external +9 V power supply is rated at 2.2 A maximum. On page 1 of the dedicated schematics (a reduced view of which is shown in Appendix B of this tutorial) it will be noted that the 3.3 V supply is rated at 5 A maximum. The derived power supply of 1.5 V is rated at 2 A max. and the LCD 5 V power supply is rated at 500 mA.

The components at U11 (LM2678S-3.3) and U20 (LM2674M-5.0) are rated for an input voltage range of +8 V to +40 V, so a wide range of power supplies may be used with the board with no worry of over-voltage conditions occurring from inadvertent accidental usage of the wrong power supply. It is expected that the voltage provided will be positive at the center pin of the J18 connector and grounded on the outside. There is protection in the Fusion Starter Kit for reverse voltages to prevent damage but correct polarity must be provided for the Fusion Starter kit to function. It will be noted that greater heating of the regulator chips will be observed with higher voltages and it is recommended that only the supplied power supply or an equivalent substitute be used with the evaluation kit as this has been rated for this board including Actel daughter cards that may be attached to the board.

Daughter Card Power Supply Connections

Limited power may be supplied by the board to a daughter card. The connector for the daughter card is shown on page 5 of the dedicated schematic PDF and is the J12 header. All the FPGA voltages of 1.5 V and 3.3 V are provided to the daughter card via a 12-pin, 0.1" pitch connector. The reason for 12 pins is that this is compatible with the 12 pins used on the ProASIC3 Starter Kits and makes the daughter cards potentially compatible between the kits. The voltages are arranged with no-connection pins interspersing the voltage pins to prevent use of a jumper to inadvertently short a supply rail to ground by connecting differing supply rails together. This is not to protect the power supply regulators, as these will go high-impedance when an over-voltage condition is detected, but to protect the FGPA from a higher voltage being unintentionally applied to the 1.5 V core. Three of the 12 pins are ground pins to provide more than sufficient current return capability for future Actel daughter cards that will work with this board. The remaining pins are no-connection to prevent accidental shorting.

Power Supplies and Chaining Boards Together

There is a special note to be made of VPUMP connections when chaining boards together. This is detailed here. Actel recommends that the reader, unless experienced with Actel Starter Kit boards, return to this section after reading the subsequent section on standard JTAG programming connections via a FlashPro3.

When joining multiple Fusion or ProASIC3 starter kit boards together via the chain programming connection it should be borne in mind that J2 connector is used to connect to the J1 connector of the

next board in the chain by attaching a standard 10-pin, 0.100" pitch programming cable. Ideally, twisted-pair ribbon cabling should be used for this connection. The length of the cable should be kept as short as possible, as multiple boards connected to form a JTAG chain of Fusion and ProASIC3/E and/or ARM7-enabled Fusion or ProASIC3 devices will provide much greater noise pick-up and may degrade the TCK clock for devices remote from the FlashPro3 programmer. Actel recommends that VJTAG be set at 3.3 V to help with signal integrity when chaining boards together. On all boards the jumper at JP10, if connected, is used for providing VJTAG to a downstream board that needs to know what VJTAG setting is being used by your board (e.g. some arbitrary board of your own design that you wish to supply with the VJTAG voltage used by the Fusion component). In most normal cases this shunt should be disconnected. The shunt normally in this location can be safely stored across pins 11 and 12 or 9 and 10 of the J12 daughter card power supply connector. For particularly long chains, the value of TCK used during programming should be reduced. The lowest value it can take is 1 MHz.

To date, only one revision of the Fusion Starter Kit board has been produced. This first version of the board is labeled REV1 next to the AFS-EVAL-BRD1 label on the board. If the Fusion Board is connected in a chain manner to ProASIC3/E boards, the documentation related to the ProASIC3/E board should be read in detail to determine the appropriate connection setting depending on version of the ProASIC3/E board being used. The following notes are only for the Fusion Starter Kit board versions.

Procedure for Rev1 Fusion Boards

To determine if the board is a Rev1 Board:

To identify a Rev1 Board, examine the front of the board and look for the part number located just beneath the large Actel logo silkscreened on the board. The part number will be "AFS-EVAL-BRD1" followed by "REV1".

To chain Rev1 Fusion boards together:

All boards, starting from the board nearest the FlashPro3 programmer, should have the shunt moved from the default location connecting pins 3 and 4 of the J5 header to connect pins 1 and 2 of the J5 header. On the board and schematic this is labeled "CHAIN" (pins 1 and 2) and "LAST DEVICE (DEFAULT)" (pins 3 and 4). Only the very last board in the chain should have the shunt remaining across pins 3 and 4 of the J5 connector.

When connecting these boards together via a connection from J2 of one board to J1 of another board, VPUMP will be connected from one board to another. When powering on one board with a connector in place, notice that the 1.5 V and 3.3 V LEDs will light on the board to which no power has been applied and the FPGA on that board, if programmed, will start operating. This is clearly an inappropriate situation for a large chain of boards. This is caused by having the JP54 connector supplying VPUMP from the board connected to other boards in the chain as VPUMP is itself connected to the 3.3 V supply output that is used to generate the other FPGA voltages on a board. To prevent VPUMP from being used as the source of a 3.3 V supply, you should remove the shunt

that is in place on the JP54 connector to force JP54 open-circuit. To prevent loss of the shunt, it may safely be stored on the J12 header for the daughter card power supply as it is impossible to cause a short by joining any adjacent pins.

Programming the AFS-EVAL-BRD1 with a FlashPro3

The base board used for all Fusion starter kits is the AFS-EVAL-BRD1.

In an AFS EVAL KIT the Actel part number for the board is AFS-EVAL-BRD600-SA. The part number indicates that the board is fitted with an AFS600-FG256 part that is directly soldered (-SA) to the board.

Connecting the FlashPro3 Programmer to the Board

Connect the FlashPro3 programmer to your computer via the USB cable. Follow the instructions in the FlashPro v4.1 (or later) User Guide to install the software and connect to the FlashPro3 programmer. The amber (yellow) power LED on the FlashPro3 should be illuminated at this stage. If it is not, recheck the procedure in the FlashPro user's guide until you obtain a steady amber (yellow) power LED illumination.

Make sure the board power switch SW11 is in the OFF position and only the red board external power LED is illuminated on the board.

Connect the 3 programmer to the board via the 10-pin programming cable supplied with the FlashPro3 programmer hardware. The connector to use on the board is labeled "FP3" and is the lower J1 shrouded and keyed header. The pin 1 location on the cable indicated by the red ribbon running along the side of the cable will be on the left side as it enters into the board. After connecting the FlashPro3 programmer, using the FlashPro v4.1 software, select "Analyze Chain" from the File menu. If all is well the appropriate device ID for the Fusion part will appear in the software display on the PC. If you suspect a JTAG communication issue, try changing the VJTAG voltage to 3.3 V using JP27.

Programming or Re-Programming the Example Design

On the Starter Kit CD you will find a *Designer* directory containing a STAPL file for programming the target design. Select the TOP_AFS.STP file from the CD and use that as the STAPL file in the FlashPro v4.1 software. Selecting the "PROGRAM" action will erase, program and verify the part. The total programming time is approximately 2 minutes 30 seconds.

Jumpers for Isolating Switches, LEDs from FPGA

It will be noted that thee are many jumpers on the board. These are provided to allow the user to disconnect various switch combinations or LEDs from the FPGA I/O banks.

The jumpers are shown in the schematic and are labeled on the top-layer silkscreen as JP*, where * is a number. All jumpers are also labeled with the FPGA I/O pin number to which they are connected, e.g. JP54 for 3.3 V connection of VPUMP to the FPGA is labeled with "M12" which indicates that it is connected to pin M12. Similarly, SW4 has a jumper above it called JP14 which is labeled with "C10" indicating that SW4 is connected through to pin C10 of the FPGA when this jumper is in place.

Figure 2-1 on page 15 shows the board's silkscreen layer overlaid with a grid, and Table 2-1 on page 16 describes the function of each jumper and its location.

By disconnecting the jumpers JP11, JP12, JP13, and JP14, the momentary push button switches SW1, SW2, SW3, and SW4, respectively, can be disconnected from the FPGA such that the I/O pins B11, A11, C11, and C10, respectively, may be used for other purposes. Disconnecting jumpers JP1–JP8 will disconnect the LEDs D1–D8 from the FPGA I/O pins B12, C13, E11, D11, B13, A13, B14, and A14, respectively.

The momentary push button switches SW5 and SW6 for applying a global pulse and a reset pulse are connected via jumpers JP15 and JP16 to I/Os K11 and L15, respectively. Again, all labeling is clearly shown on the silk screen. However, it should be noted that the silkscreen does not match the schematic in this regard; the silkscreen incorrectly labels SW5 as reset and SW6 as global. Apart from this inconsistency, there is no difference to either of the two connections.

The LCD display also has associated jumpers for its data, namely JP41, JP42, JP43, and JP44, located on the top left side of the board. These are connected to I/O pins E2, E3, F5, and F6, respectively. The LCD control signals Enable, R/W, and RS are provided from I/O pins D3, E5, and D1 via jumpers JP47, JP45, and JP46, respectively.

Analog Circuitry Provided on the Board

A variety of analog inputs and outputs are provided on the Fusion Starter Kit Evaluation Board to show what Fusion can do as a single chip solution. These components are detailed below and in the following Jumper tables enumerating all the different connectivity. As per all other components, the FPGA pins may be disconnected from these components to allow the board to be used for other functions.

A potentiometer R50 for simple user variation of analog input is provided on the board. This input is fed to the AV0 pad.

A multicolor LED U1 is also provided which has three individual color components that can be controlled by a set of AG pins (AG6 - Blue, AG7 - Orange, AG8 - Green). By using the analog outputs, PWM control as well as individual switch control by be effected. The multicolor LED is enabled by a MOSFET Q5 with the AG3 pad being connected to the gate of this P-channel MOSFET.

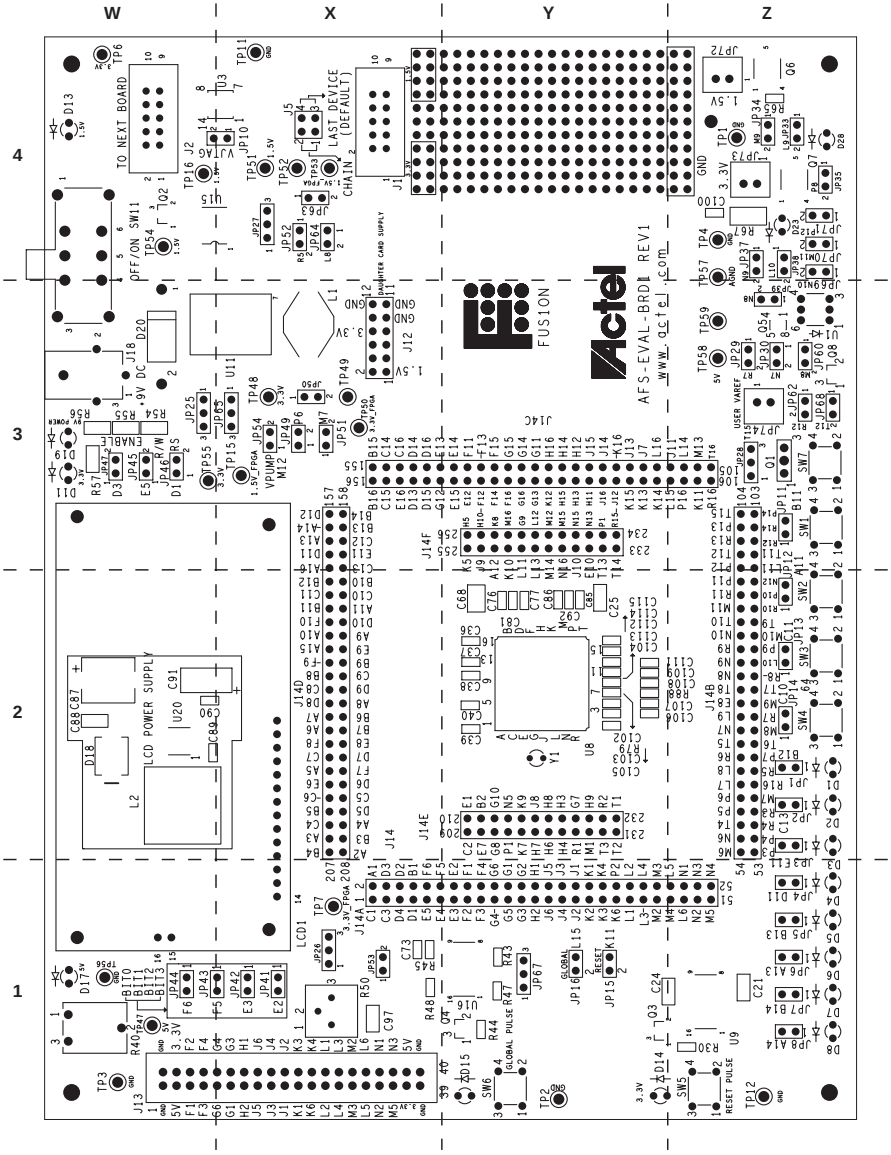

Figure 2-1. Fusion Evaluation Board Top Silkscreen

Table 2-1. Jumper Function Listings and Silkscreen Grid Locations

Jumper	Starter Kit Function	Notes	Grid Location
JP1	Disconnects green LED D1	Pin 1 to LED, pin 2 to FPGA B12	Z2
JP2	Disconnects green LED D2	Pin 1 to LED, pin 2 to FPGA C13	Z2
JP3	Disconnects green LED D3	Pin 1 to LED, pin 2 to FPGA E11	Z2
JP4	Disconnects green LED D4	Pin 1 to LED, pin 2 to FPGA D11	Z1
JP5	Disconnects green LED D5	Pin 1 to LED, pin 2 to FPGA B13	Z1
JP6	Disconnects green LED D6	Pin 1 to LED, pin 2 to FPGA A13	Z1
JP7	Disconnects green LED D7	Pin 1 to LED, pin 2 to FPGA B14	Z1
JP8	Disconnects green LED D8	Pin 1 to LED, pin 2 to FPGA A14	Z1
JP9	-- No such jumper --	--	--
JP10	Enables VJTAG Downstream to next board	Pin 1 to VJTAG of FPGA, pin 2 to programming header J2 pin 6 for next board	W4 and X4
JP11	Disconnects SW1	Pin 1 to switch, pin 2 to FPGA B11	Z3
JP12	Disconnects SW2	Pin 1 to switch, pin 2 to FPGA A11	Z2
JP13	Disconnects SW3	Pin 1 to switch, pin 2 to FPGA C11	Z2
JP14	Disconnects SW4	Pin 1 to switch, pin 2 to FPGA C10	Z2
JP15	Disconnects one shot pulse initiated by SW5	Pin 1 to U9 pin 13, pin 2 to FPGA K11	Y1
JP16	Disconnects one shot pulse initiated by SW6	Pin 1 to U16 pin 13, pin 2 to FPGA L15	Y1
JP17	-- No such jumper --	--	--
JP18	-- No such jumper --	--	--
JP19	-- No such jumper --	--	--
JP20	-- No such jumper --	--	--
JP21	-- No such jumper --	--	--

Table 2-1. Jumper Function Listings and Silkscreen Grid Locations (Continued)

Jumper	Starter Kit Function	Notes	Grid Location
JP22	-- No such jumper --	--	--
JP23	-- No such jumper --	--	--
JP24	-- No such jumper --	--	--
JP25	Selects value of VMV1	Pin 1 is 1.5V_FPGA, Pin 2 is VMV1, Pin 3 is 3.3V_FPGA	W3
JP26	Selects value of VMV0	Pin 1 is 1.5V_FPGA, Pin 2 is VMV0, Pin 3 is 3.3V_FPGA	X1
JP27	VJTAG voltage selection	Pin 1 is 1.5V, Pin 2 is VJTAG, Pin 3 is 3.3V	X4
JP28	Sets if 1.5V is internally generated or externally generated	Pin 1 is 1.5V_INT, Pin 2 is 1.5V, Pin 3 is 1.5V_EXT	Z3
JP29	Disconnects AV3	Pin 1 is TP58 (5.0V), Pin 2 is AV3_FLT (filtered to R7)	Z3
JP30	Disconnects AC3	Pin 1 is TP59, Pin 2 is AC3_FLT (filtered to N7)	Z3
JP31	-- No such jumper --	--	--
JP32	-- No such jumper --	--	--
JP33	Disconnects AV4	Pin 1 is 1.5V, Pin 2 is AV4_FLT (filtered to L9)	Z4
JP34	Disconnects AC4	Pin 1 is JP72 pin 1 for external 1.5V fan, Pin 2 is AC4_FLT (filtered to M9)	Z4
JP35	Disconnects AG4	Pin 1 is Gate of N-channel MOSFET Q6 for 1.5V fan, Pin 2 is AG4 (P8)	Z4
JP36	-- No such jumper --	--	--
JP37	Disconnects AV5	Pin 1 is 3.3V, Pin 2 is AV5_FLT (filtered to N9)	Z4
JP38	Disconnects AC5	Pin 1 is JP73 pin 1 for external 1.5V fan, Pin 2 is AC5_FLT (filtered to L10)	Z4
JP39	Disconnects AG5	Pin 1 is Gate of N-channel MOSFET Q7 for 3.3V fan, Pin 2 is AG5 (N8)	Z3
JP40	-- No such jumper --	--	--

Table 2-1. Jumper Function Listings and Silkscreen Grid Locations (Continued)

Jumper	Starter Kit Function	Notes	Grid Location
JP41	Disconnects LCD data Bit3	Pin 1 is MDL14 – Bit3, Pin 2 is FPGA E2	X1
JP42	Disconnects LCD data Bit2	Pin 1 is MDL13 – Bit2, Pin 2 is FPGA E3	X1
JP43	Disconnects LCD data Bit1	Pin 1 is MDL12 – Bit1, Pin 2 is FPGA F5	W1
JP44	Disconnects LCD data Bit0	Pin 1 is MDL11 – Bit0, Pin 2 is FPGA F6	W1
JP45	Disconnects LCD control R/W	Pin 1 is MDL5 – R/W, Pin 2 is FPGA E5	W3
JP46	Disconnects LCD control RS	Pin 1 is MDL4 – RS, Pin 2 is FPGA D1	W3
JP47	Disconnects LCD control ENABLE	Pin 1 is MDL6 – ENABLE, Pin 2 is FPGA D3	W3
JP48	-- No such jumper --	--	--
JP49	Disconnects AV1	Pin 1 is TP48 (3.3V), Pin 2 is AV1_FLT (filtered to P6)	X3
JP50	Disconnects TP48 and TP49	Allows ammeter to be connected between TP48 and TP49 to measure 3.3V_FPGA current	X3
JP51	Disconnects AC1	Pin 1 is TP59, Pin 2 is AC1_FLT (filtered to M7)	X3
JP52	Disconnects AV2	Pin 1 is TP51 (1.5V), Pin 2 is AV2_FLT (filtered to R5)	X4
JP53	Disconnects AV0 from Potentiometer R50	Pin 1 is center of R50 potentiometer, Pin 2 is AV0_FLT (filtered to M6)	X1
JP54	Disconnects 3.3V_FPGA from VPUMP	Pin 1 is VPUMP (M12), Pin 2 is 3.3V_FPGA	X3
JP55	-- No such jumper --	--	--
JP56	-- No such jumper --	--	--
JP57	-- No such jumper --	--	--
JP58	-- No such jumper --	--	--
JP59	-- No such jumper --	--	--

Table 2-1. Jumper Function Listings and Silkscreen Grid Locations (Continued)

Jumper	Starter Kit Function	Notes	Grid Location
JP60	Disconnects AG3 from multicolor LED	Pin 1 is gate of P-channel MOSFET Q5, Pin 2 is AG3 (M8)	Z3
JP61	-- No such jumper --	--	--
JP62	Disconnects AT9	Pin 1 is base-collector of temperature “diode”, Pin 2 is AT9 (R12)	Z3
JP63	Disconnects TP51 and TP52	Allows ammeter to be connected between TP51 and TP52 to measure 1.5V_FPGA current	X4
JP64	Disconnects AC2	Pin 1 is TP53, Pin 2 is AC2_FLT (filtered to L8)	X4
JP65	Selects value of VCCPLB	Pin 1 is 1.5V_FPGA, Pin 2 is VCCPLB (B15), Pin 3 is GND	X3
JP66	-- No such jumper --	--	--
JP67	Selects value of VCCPLA	Pin 1 is 1.5V_FPGA, Pin 2 is VCCPLA (B2), Pin 3 is GND	Y1
JP68	Disconnects ARTN4	Pin 1 is emitter of temperature “diode”, Pin 2 is ARTN4 (T12)	Z3
JP69	Disconnects AG6 from Blue	Pin 1 is tri-color LED U1 pin 1 (Blue), Pin 2 is AG6 (N10)	Z3 and Z4
JP70	Disconnects AG7 from Orange	Pin 1 is tri-color LED U1 pin 2 (Orange), Pin 2 is AG7 (M11)	Z4
JP71	Disconnects AG8 from Green	Pin 1 is tri-color LED U1 pin 3 (Green), Pin 2 is AG8 (P12)	Z4
JP72	Shrouded Header for 1.5V fan	Pin 1 is 1.5V, Pin 2 is drain of N-channel MOSFET Q6	Z4
JP73	Shrouded Header for 3.3V fan	Pin 1 is 3.3V, Pin 2 is drain of N-channel MOSFET Q7	Z4
JP74	Shrouded Header for User Supplied VAREF	Pin 1 is VAREF (T15), Pin 2 is GND	Z3
JP75	-- No such jumper --	--	--

Table 2-1. Jumper Function Listings and Silkscreen Grid Locations (Continued)

Jumper	Starter Kit Function	Notes	Grid Location
JP76	-- No such jumper --	--	--
JP77	-- No such jumper --	--	--
JP78	-- No such jumper --	--	--
JP79	-- No such jumper --	--	--
JP80	-- No such jumper --	--	--

Test Points

All test points on the board are fitted with small test loops. These test points are labeled on the silk screen as TP1, TP2 etc. All such test points are also labeled on the silk screen with the voltage expected to be observed at that test point. Voltages will be one of 5.0 V, 3.3 V, 1.5 V, or GND. When measuring the voltage at a test point with a DVM (digital voltage multimeter) the ground lead should be connected to a test point labeled GND and the voltage lead should be connected to the voltage to be tested. All voltage labels on the board are relative to a 0 V ground reference or GND.

Prototyping Area

The prototyping area to the right of the board has the bottom two rows of pins connected to ground, labeled as GND on the silk screen and enclosed in a box, giving 16 holes connected to 0V. The top two rows of pins are connected to various power supply rails internally in the board. They are grouped into rectangles of eight pins from left to right as follows: 3.3V to the left and 1.5V to the right, giving eight holes for each voltage level and six unconnected holes in the middle. All other holes in the prototyping area are unconnected and may be used to hold various discrete components as necessary for experimentation.

On the reverse side of the board there is an area labeled U5, which is a TQ100 pattern with some surrounding pads. This area may be used to solder a TQ100 part and then connect that part by adding discrete wires to the pads and connecting it to desired pins on the board. The main purpose of this is to allow a previously programmed TQ100 packaged device to be used to provide a more interesting system application

Layering on Board

The complete board design and manufacturing files are included on the Starter Kit CD. The board file is in Allegro format, which will allow an end user to create the appropriate Gerbers and other

board views as needed. Pictures of the layers of the board are included in "Signal Layers" on page 63. For your convenience, high-resolution PDFs of these layers are also provided on the Starter Kit CD.

The board is fabricated with six copper layers. The layers are arranged as follows from top to bottom:

- Layer 1 – Top Signal Layer
- Layer 2 – Ground Plane (split into separate digital ground and analog ground joined at a single point)
- Layer 3 – Signal Layer 3
- Layer 4 – Signal Layer 4
- Layer 5 – Power Plane
- Layer 6 – Bottom Signal Layer

See the diagrams in "Signal Layers" on page 63.

3

Setup and Self Test

This chapter outlines how to set up and test the Fusion Evaluation Board.

Software Installation

The Fusion Starter Kit includes the Libero® Integrated Design Environment (IDE) software (version 7.0 SPa). For Libero IDE software installation instructions, refer to the *Actel Libero IDE / Designer Installation and Licensing Guide for Software v7.0 SPa:*

http://www.actel.com/documents/install.pdf.

Hardware Installation

FlashPro v4.1 is required to use the Fusion Starter Kit. For software and hardware installation instructions, refer to the *FlashPro v4.1 User's Guide*:

http://www.actel.com/documents/flashproUG.pdf

Testing the Evaluation Board

Refer to "Test Procedures for Board Testing" on page 29.

Programming the Test File

To retest the evaluation board at any time, use the test program to reprogram the board. Use the TOP_AFS.stp file with an AFS600-FG256 fitted on the board.

This design is currently implemented for the AFS600 die size. For a device of a different size, it is possible to recompile the design into other device sizes. For information about retargeting the device, refer to the *Designer User's Guide* at http://www.actel.com/documents/designerUG.pdf. The design files are available under *actelprj/eval* in the Starter Kit CD.

For instructions on programming the device using FlashPro v4.1, refer to the *FlashPro v4.1 User's Guide* at http://www.actel.com/documents/flashproUG.pdf

4

Description of Test Design

This description of the test design is provided with the Starter Kit. This design contains a data generator block for LEDs, a clock divider, and an LCD display block. A block diagram of the design is shown in Figure 4-1.

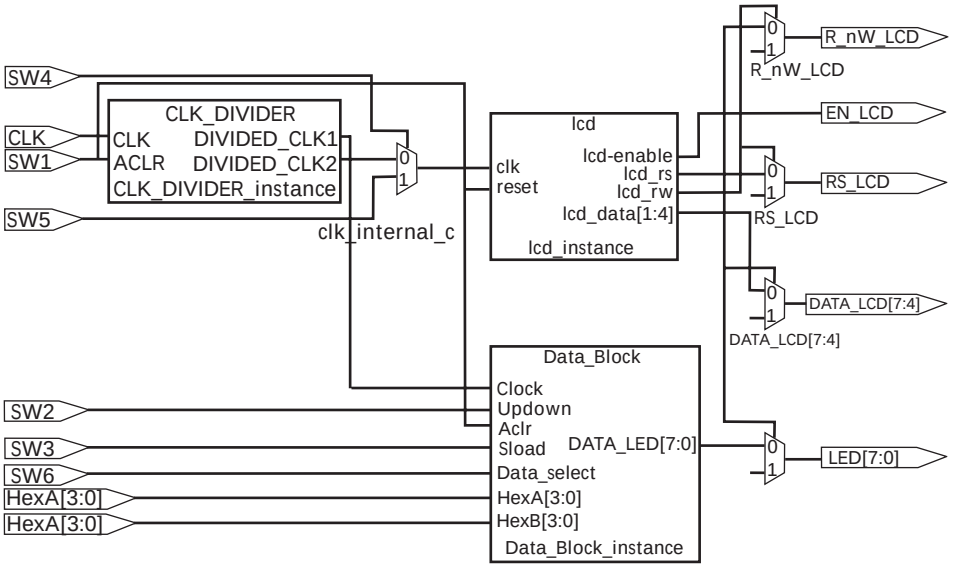

Figure 4-1. Design Block Diagram

The clock divider divides the 40 MHz oscillator clock and sends the divided clock to the LCD module and the counter. The data generator (Data_Block) generates an eight-bit up-down counter and eight-bit flashing signal. The data generator output is displayed on the Fusion Evaluation Board LEDs. You can switch between the data using the SW6 signal. The counter has a synchronous load and an asynchronous clear.

A block diagram of the Data_Block is shown in Figure 4-2.

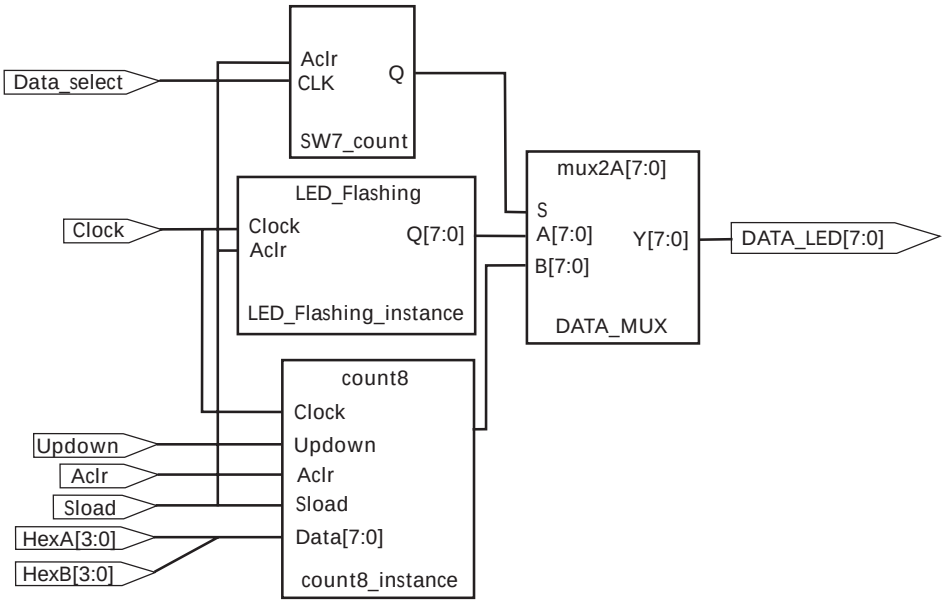

Figure 4-2. Data Block Diagram

A message is generated and displayed on the demo board LCD display. A state machine controls the LCD module.

Table 4-1. Switches

Action	Results
Press SW1	Asynchronous clear for the whole design
Press SW2	Up-Down Control for the 8-bit counter. Press and hold SW2 for down count.
Press SW3	Synchronous load for the 8-bit counter. Press SW3 for loading from the Hex switches.
Press SW4	Switching between manual clock(SW5) and 40 Mhz Oscillator Clock.
Press SW5	Manual clock (very useful for simulation)
Press SW6	Select for DATA_BLOCK. It allows switching LED output between the counter and Flashing data.
Change Hex Switch setting (U13 and U14)	Changes the loaded data for the eight-bit counter.

The state diagram is shown in Figure 4-3.

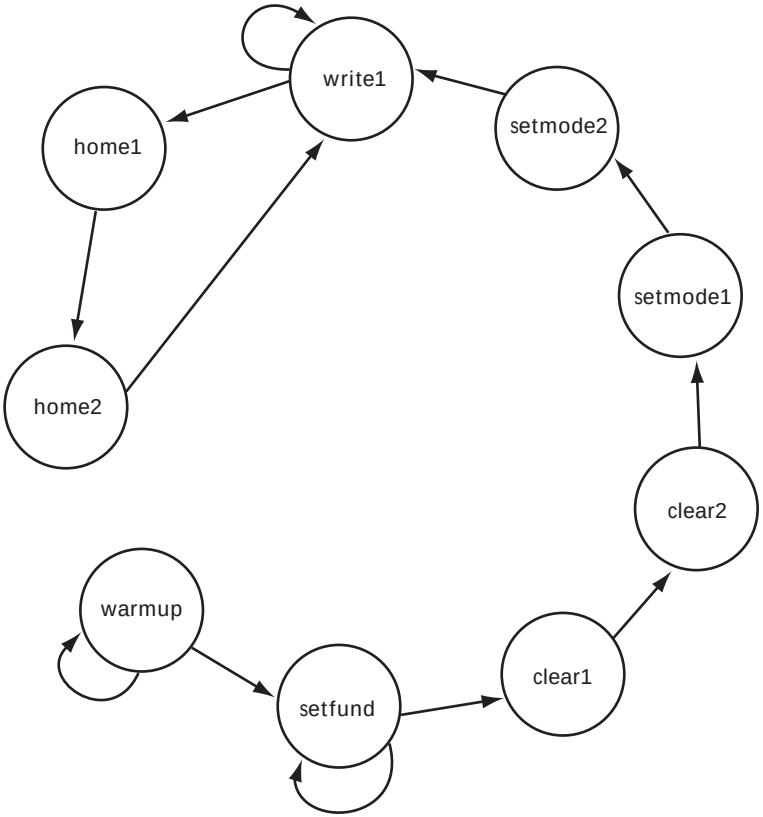

Figure 4-3. LCD State Diagram

5

Test Procedures for Board Testing

Overview

This document defines the test procedure required to be carried out by the Actel designated manufacturer's testing facility on the Fusion Evaluation Board with silkscreen labeling AFS-EVAL-BRD1. This testing is specific to the socketed version of the board. All steps in the following enumerated test procedure should be followed in sequence for testing the board. Deviations in the sequence are explained in the text.

Equipment Required

Actel Equipment Provided by Actel to Testing Facility

Actel will provide the following:

- This test procedure document.
- FlashPro v4.1 software on a CD-ROM.
- FlashPro3 programmer and programming cable for connecting to the AFS-EVAL-BRD1.
- Pre-programmed AFS600-FG256 silicon. Ten devices will be provided for ten boards. The initial silicon will not be labeled as having been programmed. (This is just for the testing associated with the first manufacturing build.) Additional devices will be provided for testing further boards and this change will be detailed in an update to the procedure.
- Power supply (+9 V, 2 A CUI) for the Fusion Starter Kit board plus a mains cable for the power supply.

Testing Facility Equipment to be Available for Testing

The manufacturer's testing facility will provide the following equipment for testing of the board:

- Digital Multimeter to measure voltages on the circuit board at the known test points.

Test Procedure for the AFS-EVAL-BRD1

In this section, full test procedure for the boards is outlined. This procedure applies to socketed boards. For boards fitted with directly soldered parts, the procedure is the same except for fitting of the FPGA. In such cases, the reader should adjust the procedure accordingly and ignore references to fitting parts to sockets.

Initial Power-On Procedure

This part of the procedure may be carried out independently and ahead of the other parts of the test procedure. Boards passing this procedure may be transferred to a passing set of boards.

To perform the initial power-on procedure:

1. Record the time of the test and the board serial number (written by the bar code on the back of the board) into a test log.
2. Plug the +9 V power supply into the wall.
3. Take an AFS-EVAL-BRD1 that has an empty socket. Make sure the switch SW11 is in the OFF position, (the switch should be moved to the left). This corresponds with the labeling of the silkscreen on the board.
4. Connect +9 V DC output of the CUI power supply to the J18 connector on the board. You should observe the red LED at the top right of the board, i.e. LED D19 should light indicating +9 V DC has been applied to the board.
5. Move the SW11 switch to the ON position, i.e., move the switch to the right. Observe that LEDs, D13, D9, D10, D11, and D17 light up green on the board. All LEDs are on the top edge of the board (same edge as red D19 power connector LED, which should remain lit).
6. Using a DVM, measure DC voltages using TP11 as ground:

   TP6 and TP7 – should be 3.3 V (values ±0.2 V are acceptable). Values outside this range are a failure.

   TP15 – should be 1.5 V (values ±0.1 V are acceptable).

   TP8 – should be 1.8 V (values ±0.1 V are acceptable).

   TP10 – should be 2.5 V (values ±0.2 V are acceptable).

   TP47 – should be 5.0 V (values ±0.2 V are acceptable).

   J14C pin 106 – should be 3.3 V (values ±0.2 V are acceptable). Note that jumper JP48 must be in place for this measurement, otherwise zero will be recorded.
7. That completes the initial power-on check. The board should now be switched off by moving SW11 to the OFF position (to the left).

Testing Board Functionality with AFS600-FG256 Silicon

To test board functionality:

1. Record the time of the test and the board serial number (written by the bar code on the back of the board) into a test log.
2. Make sure the switch SW11 is in the OFF position (i.e., to the left.)
3. Apply power to the board by attaching the +9 V DC supply to J18. Only the red LED should be illuminated.
4. Undo the four screws holding the socket of U8 in place. Remove the lid of the socket.
5. Place a pre-programmed AFS600-FG256 FPGA part into the socket using the appropriate vacuum pen while observing anti-static precautions. Make sure that pin 1 of the FPGA is oriented correctly. (The Actel logo on the part should match the orientation of the Actel logo on the board just above the AFS-EVAL-BRD1 part number.) Take great care to make sure all pins are in correct alignment so that the FPGA is on a level plane parallel to the board.
6. Carefully replace the socket cover and screw down all four corners to appropriate tightness. It is recommended to do opposite corners first so as to lessen rotational torque on the part.
7. Switch on SW11 to the ON position (slide it to the right).
8. Validate that all 5 LEDs at the top of the board including the red one turn on. D17, D11, D10, D9, D13, and D19.
9. Validate that the 8 LEDS: D8, D7, …, and D2, D1 all pulsate in either a counting pattern or a "center to outside swinging" pattern.
10. If no LEDs are visible, stop and switch off SW11. Rotate SW8 and SW9 clockwise to the 3.3 V selection. This is best described with the thicker arrow bar pointing upward. Switch the board back on. The LEDs should be visible. If very dim, stop, switch off the board and rotate the switches one quarter turn clockwise before switching board back on. Continue if the LEDs are glowing. If unable to get a display on the LEDs, the board must be tagged as bad.
11. If it is a bad board, carefully remove the AFS600-FG256 silicon from the socket and set it aside in an electrostatic-safe area. Using another piece of pre-programmed silicon, repeat steps 4 to 8 above.

    If still no response, mark the board as defective and re-use the silicon for other testing.

    If there is a good response, then place the previous silicon in a "bad" tray to prevent it from being retested.
12. Validate that the patterns can be switched by pressing SW6 (Global pulse) on the left side of board. When the switch is pressed, the LED D15 should momentarily light. The pattern on the 8 LEDs D8 through D1 will change.
13. Validate that the message "Actel Fusion Starter Kit" continually cycles on the LCD display. You may need to turn R40 clockwise to adjust contrast on the display until the message is dark enough to see.

If no message is observed, press buttons SW4 and SW3 simultaneously. This will usually reset the system after a few cycles of the counter.

14. Connect a FlashPro3 programmer to a PC USB port and observe the power light illuminating. Ensure that the FlashPro v4.1 software is installed on the PC being used.
15. Connect the programming cable of the FlashPro3 programmer to the J1 shrouded and keyed header labeled FP3. The red line labeling pin 1 should be close to pin 1 on the header – no other orientation is possible.
16. On the PC, run the FlashPro v4.1 software and connect to the programmer. Select Fusion as the device family. Once the software has shown a connection, select **Analyze Chain** from the **File** menu.

    If an error message of incorrect VJTAG is reported, then remove the jumper placed at J5 and place it instead at J12 across pins 11 and 12. It may safely be left there. Repeat the **Analyze Chain** command.

    If a message appears indicating that an AFS600 part (depending on the device fitted to the board) has been detected, then the board has passed this test. Leave the silicon in place in the socket and move to the next step.

    If a message of **11** or some other numeric indication appears, then record the message in a test log and fail the board. Remove the silicon from the socket and place it in the safe silicon holding area.
17. This concludes the testing of the board. Switch SW11 to the OFF position and remove the power connector from J18.

A

FG256 Package Connections for AFS600 Devices

Due to the comprehensive and flexible nature of Fusion device user I/Os, a naming scheme is used to show the details of the I/O. The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwBy

Gmn is only used for I/Os that also have CCC access – i.e., global pins.

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle)

n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2

u = I/O pair number in the bank, starting at 00 from the northwest I/O bank in a clockwise direction

x = P (Positive) or N (Negative) for differential pairs, or R (Regular – single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive-LVDS only) or V (Negative-LVDS only) restrict the I/O differential pair from being selected as LVPECL pair.

w = D (Differential Pair) or P (Pair) or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number [0..7]. Bank number starting at 0 from the northwest I/O bank in a clockwise direction

Figure A-1 on page 34 and Table A-1 on page 35 are extracted from the Fusion datasheet and provide package connections for the AFS600 device. Pinouts for other devices in the Fusion family may be found on the Actel website:

Fusion Flash Family FPGAs datasheet at www.actel.com/documents/Fusion_DS.pdf

This datasheet is included on the Fusion Starter Kit CD. However, the website should always be consulted for the most recent datasheet.

256-Pin FBGA (Bottom View)

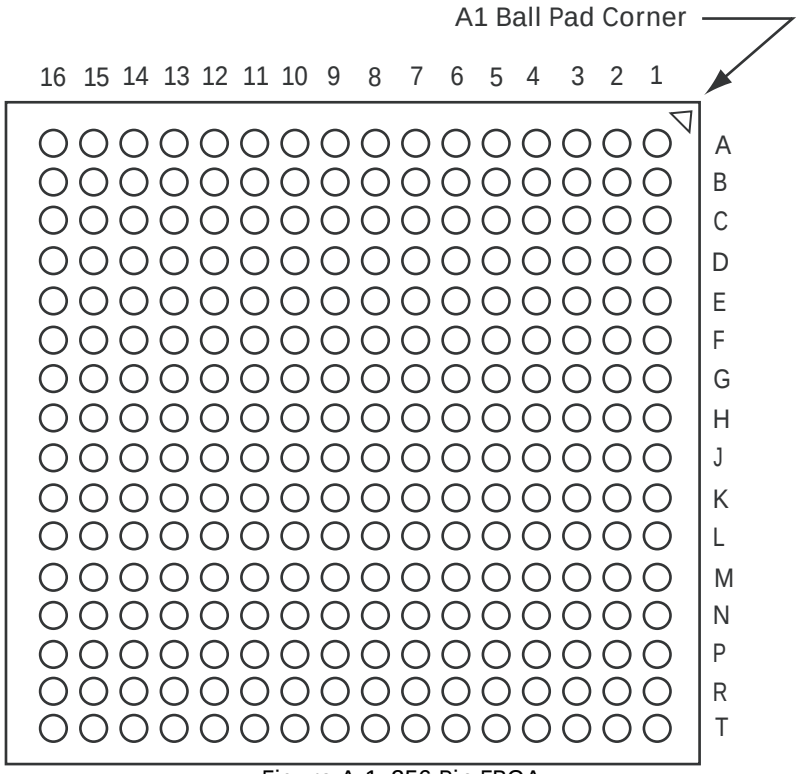

Figure A-1. 256-Pin FBGA

Note: For package manufacturing and environmental information, visit the Resource Center at http://www.actel.com/products/rescenter/package/index.html.

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board

Pin Number	Pin Name	Starter Kit Function	Notes
A1	GND	GND	Tied to GND
A2	VCCIB0	VMV0	Jumper JP26 ties to 1.5V_FPGA or 3.3V_FPGA
A3	GAA0/IO01NDB0V0	General I/O	Global
A4	GAA1/IO01PDB0V0	General I/O	Global
A5	GND	GND	Tied to GND
A6	IO10PDB0V1	General I/O	
A7	IO12PDB0V1	General I/O	
A8	IO12NDB0V1	General I/O	
A9	IO22NDB1V0	General I/O	
A10	IO22PDB1V0	General I/O	
A11	IO24NDB1V1	Pressing SW2 applies VMV1	Jumper JP12 can disconnect
A12	GND	GND	Tied to GND
A13	GBA0/IO28NDB1V1	Green LED D6	Jumper JP6 can disconnect
A14	IO29NDB1V1	Green LED D8	Jumper JP8 can disconnect
A15	VCCIB1	VMV1	Jumper JP25 ties to 1.5V_FPGA or 3.3V_FPGA
A16	GND	GND	Tied to GND
B1	VCOMPLA	GND	Tied to GND
B2	VCCPLA	VCCPLA	Jumper JP67 ties to 1.5V_FPGA or GND
B3	IO00NDB0V0	General I/O	
B4	IO00PDB0V0	General I/O	
B5	GAB1/IO02PPB0V0	General I/O	Global
B6	IO10NDB0V1	General I/O	
B7	VCCIB0	VMV0	Jumper JP26 ties to 1.5V_FPGA or 3.3V_FPGA

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board (Continued)

Pin Number	Pin Name	Starter Kit Function	Notes
B8	IO18NDB1V0	General I/O	
B9	IO18PDB1V0	General I/O	
B10	VCCIB1	VMV1	Jumper JP25 ties to 1.5V_FPGA or 3.3V_FPGA
B11	IO24PDB1V1	Pressing SW1 applies VMV1	Jumper JP11 can disconnect
B12	GBC0/IO26NPB1V1	Green LED D1	Jumper JP1 can disconnect
B13	GBA1/IO28PDB1V1	Green LED D5	Jumper JP5 can disconnect
B14	IO29PDB1V1	Green LED D7	Jumper JP7 can disconnect
B15	VCCPLB	VCCPLB	Jumper JP65 ties to 1.5V_FPGA or GND
B16	VCOMPLB	GND	Tied to GND
C1	VCCIB4	VMV4	Tied to 3.3V_FPGA
C2	GND	GND	Tied to GND
C3	VMV4	VMV4	Tied to 3.3V_FPGA
C4	VMV0	VMV0	Jumper JP26 ties to 1.5V_FPGA or 3.3V_FPGA
C5	VCCIB0	VMV0	Jumper JP26 ties to 1.5V_FPGA or 3.3V_FPGA
C6	GAC1/IO03PDB0V0	General I/O	Global
C7	IO06NDB0V0	General I/O	
C8	IO16PDB1V0	General I/O	
C9	IO16NDB1V0	General I/O	
C10	IO25NDB1V1	Pressing SW4 applies VMV1	Jumper JP14 can disconnect
C11	IO25PDB1V1	Pressing SW3 applies VMV1	Jumper JP13 can disconnect
C12	VCCIB1	VMV1	Jumper JP25 ties to 1.5V_FPGA or 3.3V_FPGA
C13	GBC1/IO26PPB1V1	Green LED D2	Jumper JP2 can disconnect
C14	VMV2	VMV2	Tied to 3.3V_FPGA
C15	GND	GND	Tied to GND

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board (Continued)

Pin Number	Pin Name	Starter Kit Function	Notes
C16	VCCIB2	VMV2	Tied to 3.3V_FPGA
D1	IO84NDB4V0	LCD MDL4 - RS	Jumper JP46 can disconnect
D2	GAB2/IO84PDB4V0	General I/O	Global
D3	IO85NDB4V0	LCD MDL6 - ENABLE	Jumper JP47 can disconnect
D4	GAA2/IO85PDB4V0	General I/O	Global
D5	GAB0/IO02NPB0V0	General I/O	Global
D6	GAC0/IO03NDB0V0	General I/O	Global
D7	IO06PDB0V0	General I/O	
D8	IO14NDB0V1	General I/O	
D9	IO14PDB0V1	General I/O	
D10	IO23PDB1V1	General I/O	
D11	GBB0/IO27NDB1V1	Green LED D4	Jumper JP4 can disconnect
D12	VMV1	VMV1	Jumper JP25 ties to 1.5V_FPGA or 3.3V_FPGA
D13	GBA2/IO30PDB2V0	General I/O	Global
D14	IO30NDB2V0	General I/O	
D15	GBB2/IO31PDB2V0	General I/O	Global
D16	IO31NDB2V0	General I/O	
E1	GND	GND	Tied to GND
E2	IO81NDB4V0	LCD MDL14 – Bit3	Jumper JP41 can disconnect
E3	IO81PDB4V0	LCD MDL13 – Bit2	Jumper JP42 can disconnect
E4	VCCIB4	VMV4	Tied to 3.3V_FPGA
E5	IO83NPB4V0	LCD MDL5 – R/W	Jumper JP45 can disconnect
E6	IO04NPB0V0	General I/O	
E7	GND	GND	Tied to GND
E8	IO08PDB0V1	General I/O	
E9	IO20NDB1V0	General I/O	

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board (Continued)

Pin Number	Pin Name	Starter Kit Function	Notes
E10	GND	GND	Tied to GND
E11	GBB1/IO27PDB1V1	Green LED D3	Jumper JP3 can disconnect
E12	IO33PSB2V0	General I/O	
E13	VCCIB2	VMV2	Tied to 3.3V_FPGA
E14	IO32NDB2V0	General I/O	
E15	GBC2/IO32PDB2V0	Global IO	
E16	GND	GND	Tied to GND
F1	IO79NDB4V0	J13 pin 5	J13 is 40-pin IP header
F2	IO79PDB4V0	J13 pin 6	J13 is 40-pin IP header
F3	IO76NDB4V0	J13 pin 7	J13 is 40-pin IP header
F4	IO76PDB4V0	J13 pin 8	J13 is 40-pin IP header
F5	IO82PSB4V0	LCD MDL12 – Bit1	Jumper JP43 can disconnect
F6	GAC2/IO83PPB4V0	LCD MDL11 – Bit0	Jumper JP44 can disconnect
F7	IO04PPB0V0	General I/O	
F8	IO08NDB0V1	General I/O	
F9	IO20PDB1V0	General I/O	
F10	IO23NDB1V1	General I/O	
F11	IO36NDB2V0	General I/O	
F12	IO36PDB2V0	General I/O	
F13	IO39NDB2V0	General I/O	
F14	GCA2/IO39PDB2V0	General I/O	Global
F15	GCB2/IO40PDB2V0	General I/O	Global
F16	IO40NDB2V0	General I/O	
G1	IO74NPB4V0	J13 pin 11	J13 is 40-pin IP header
G2	VCCIB4	VMV4	Tied to 3.3V_FPGA
G3	GFB2/IO74PPB4V0	J13 pin 12	J13 is 40-pin IP header
G4	GFA2/IO75PDB4V0	J13 pin 10	J13 is 40-pin IP header

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board (Continued)

Pin Number	Pin Name	Starter Kit Function	Notes
G5	GND	GND	Tied to GND
G6	IO75NDB4V0	J13 pin 9	J13 is 40-pin IP header
G7	GND	GND	Tied to GND
G8	VCC	1.5V_FPGA	
G9	GND	GND	Tied to GND
G10	VCC	1.5V_FPGA	
G11	GCC0/IO43NDB2V0	General I/O	Global
G12	GND	GND	Tied to GND
G13	GCC1/IO43PDB2V0	General I/O	Global
G14	IO41NPB2V0	General I/O	
G15	VCCIB2	VMV2	Tied to 3.3V_FPGA
G16	GCC2/IO41PPB2V0	General I/O	Global
H1	GFC2/IO73PDB4V0	J13 pin 14	J13 is 40-pin IP header
H2	IO73NDB4V0	J13 pin 13	J13 is 40-pin IP header
H3	XTAL2	One pin of crystal Y1	Y1 is 32.768 kHz
H4	XTAL1	Other pin of crystal Y1	Y1 is 32.768 kHz
H5	GNDOSC	GND	Tied to GND
H6	VCCOSC	3.3V_FPGA	
H7	VCC	1.5V_FPGA	
H8	GND	GND	Tied to GND
H9	VCC	1.5V_FPGA	
H10	GND	GND	Tied to GND
H11	IO47NDB2V0	General I/O	
H12	IO47PDB2V0	General I/O	
H13	GCA1/IO45PDB2V0	General I/O	Global
H14	GCA0/IO45NDB2V0	General I/O	Global
H15	GCB0/IO44NDB2V0	General I/O	Global

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board (Continued)

Pin Number	Pin Name	Starter Kit Function	Notes
H16	GCB1/IO44PDB2V0	General I/O	Global
J1	GFA0/IO70NDB4V0	J13 pin 19	J13 is 40-pin IP header
J2	GFA1/IO70PDB4V0	J13 pin 20	J13 is 40-pin IP header
J3	GFB0/IO71NDB4V0	J13 pin 17	J13 is 40-pin IP header
J4	GFB1/IO71PDB4V0	J13 pin 18	J13 is 40-pin IP header
J5	GFC0/IO72NDB4V0	J13 pin 15	J13 is 40-pin IP header
J6	GFC1/IO72PDB4V0	J13 pin 16	J13 is 40-pin IP header
J7	GND	GND	Tied to GND
J8	VCC	1.5V_FPGA	
J9	GND	GND	Tied to GND
J10	VCC	1.5V_FPGA	
J11	IO56NPB2V0	General I/O	
J12	GDB0/IO53NPB2V0	General I/O	Global
J13	GDA1/IO54PDB2V0	General I/O	Global
J14	GDC1/IO52PPB2V0	General I/O	Global
J15	IO51NSB2V0	General I/O	
J16	GDC0/IO52NPB2V0	General I/O	Global
K1	IO67NPB4V0	J13 pin 21	J13 is 40-pin IP header
K2	VCCIB4	VMV4	Tied to 3.3V_FPGA
K3	IO67PPB4V0	J13 pin 22	J13 is 40-pin IP header
K4	IO65PDB4V0	J13 pin 24	J13 is 40-pin IP header
K5	GND	GND	Tied to GND
K6	IO65NDB4V0	J13 pin 23	J13 is 40-pin IP header
K7	VCC	1.5V_FPGA	
K8	GND	GND	Tied to GND
K9	VCC	1.5V_FPGA	
K10	GND	GND	Tied to GND

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board (Continued)

Pin Number	Pin Name	Starter Kit Function	Notes
K11	GDC2/IO57PPB2V0	Pressing SW5 gives one-shot "global" pulse	Jumper JP15 can disconnect. Silk screen labeled incorrectly as "reset"
K12	GND	GND	Tied to GND
K13	GDA0/IO54NDB2V0	General I/O	Global
K14	GDA2/IO55PPB2V0	General I/O	Global
K15	VCCIB2	VMV2	Tied to 3.3V_FPGA
K16	GDB1/IO53PPB2V0	General I/O	Global
L1	GEC1/IO63PDB4V0	J13 pin 26	J13 is 40-pin IP header
L2	GEC0/IO63NDB4V0	J13 pin 25	J13 is 40-pin IP header
L3	GEB1/IO62PDB4V0	J13 pin 28	J13 is 40-pin IP header
L4	GEB0/IO62NDB4V0	J13 pin 27	J13 is 40-pin IP header
L5	IO60NDB4V0	J13 pin 31	J13 is 40-pin IP header
L6	GEC2/IO60PDB4V0	J13 pin 32	J13 is 40-pin IP header
L7	GNDA	GNDA	Analog ground is on a separate plane and joined to digital ground at regulator U15 ground pins
L8	AC2	Test point TP53 for 1.5V FPGA current sense	Jumper JP64 can disconnect
L9	AV4	1.5V of fan control circuit for current sense	Jumper JP33 can disconnect
L10	AC5	Current sense of 3.3V fan circuit	Jumper JP38 can disconnect
L11	PTEM		
L12	TDO	TDO	To FlashPro3 header J1 pin 3 (if J5 in across pins (3,4) as last device) and as TDI to J2 pin 9
L13	VJTAG	VJTAG	Jumper JP27 allows setting to either 3.3V or 1.5V
L14	IO57NPB2V0		
L15	GDB2/IO56PPB2V0	Pressing SW6 gives one-shot "reset" pulse	Jumper JP16 can disconnect. Silk screen labeled incorrectly as "global"

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board (Continued)

Pin Number	Pin Name	Starter Kit Function	Notes
L16	IO55NPB2V0	General I/O	
M1	GND	GND	Tied to GND
M2	GEA1/IO61PDB4V0	J13 pin 30	J13 is 40-pin IP header
M3	GEA0/IO61NDB4V0	J13 pin 29	J13 is 40-pin IP header
M4	VCCIB4	VMV4	Tied to 3.3V_FPGA
M5	IO58NPB4V0	J13 pin 35	J13 is 40-pin IP header
M6	AV0	Analog voltage from R50 potentiometer	Jumper JP53 can disconnect. Voltage varies from 0V to 5V.
M7	AC1	Test point TP50 for 3.3V FPGA current sense	Jumper JP51 can disconnect
M8	AG3	Gate of P-channel MOSFET Q5 driving Tri-color LED	Jumper JP60 can disconnect
M9	AC4	Current sense of 1.5V fan circuit	Jumper JP34 can disconnect
M10	AC6	AC6	Unfiltered
M11	AG7	Active low for orange part of tricolor LED	Jumper JP70 can disconnect. AG7 should be set to 25mA.
M12	VPUMP	3.3V programming	Jumper JP54 connects the board supplied voltage otherwise provided by FlashPro3
M13	VCCIB2	VMV2	Tied to 3.3V_FPGA
M14	TMS	TMS	From Flashpro3 header J1 pin 5
M15	TRST	TRST	From FlashPro3 header J1 pin 8
M16	GND	GND	Tied to GND
N1	GEB2/IO59PDB4V0	J13 pin 34	J13 is 40-pin IP header
N2	IO59NDB4V0	J13 pin 33	J13 is 40-pin IP header
N3	GEA2/IO58PPB4V0	J13 pin 36	J13 is 40-pin IP header
N4	VCC33PMP	3.3V_FPGA	
N5	VCC15A	1.5V_FPGA	
N6	AG0	AG0	Unfiltered

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board (Continued)

Pin Number	Pin Name	Starter Kit Function	Notes
N7	AC3	Test point TP59 for current flow through multicolor LED	Jumper JP30 can disconnect.
N8	AG5	Gate of N-channel MOSFET Q7 for 3.3V fan control	Jumper JP39 can disconnect
N9	AV5	3.3V of fan control circuit for current sense	Jumper JP37 can disconnect
N10	AG6	Active low for blue part of tricolor LED	Jumper JP69 can disconnect. AG6 should be set to 25mA.
N11	AC8	AC8	Optional filtering available
N12	GNDA	GNDA	Analog ground is on a separate plane and joined to digital ground at regulator U15 ground pins
N13	VCC33A	3.3V_FPGA	
N14	VCCNVM	1.5V_FPGA	
N15	TCK	TCK	From FlashPro3 header J1 pin 1
N16	TDI	TDI	From FlashPro3 header J1 pin 9
P1	VCCNVM	1.5V_FPGA	
P2	GNDNVM	GND	Tied to GND
P3	GNDA	GNDA	Analog ground is on a separate plane and joined to digital ground at regulator U15 ground pins
P4	AC0	AC0	Unfiltered
P5	AG1	AG1	Unfiltered
P6	AV1	Test point TP48 for 3.3V FPGA current sense	Jumper JP49 can disconnect
P7	AG2	AG2	Unfiltered
P8	AG4	Gate of n-channel MOSFET Q6 for 1.5 V fan control	Jumper JP35 can disconnect
P9	GNDA	GNDA	Analog ground is on a separate plane and joined to digital ground at regulator U15 ground pins
P10	AC7	AC7	Unfiltered

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board (Continued)

Pin Number	Pin Name	Starter Kit Function	Notes
P11	AV8	AV8	Optional filtering available
P12	AG8	Active low for green part of tricolor LED	Jumper JP71 can disconnect. AG8 should be set to 25mA.
P13	AV9	AV9	Optional filtering available
P14	ADCGNDREF	Tied to analog ground	
P15	PTBASE	Base of Q1 pass transistor for 1.5 V internal generation	Jumper JP28 selects 1.5V internal (Q1 pass transistor) or 1.5V external (U15 regulator)
P16	GNDNVM	GND	Tied to GND
R1	VCCIB4	VMV4	Tied to 3.3V_FPGA
R2	PCAP	PCAP	
R3	AT1	AT1	Unfiltered
R4	AT0	AT0	Unfiltered
R5	AV2	Test point TP51 for 1.5V FPGA current sense	Jumper JP52 can disconnect
R6	AT2	AT2	Unfiltered
R7	AV3	Test point TP58 for current flow through multicolor LED	Jumper JP29 can disconnect.
R8	AT5	AT5	Unfiltered
R9	AV6	AV6	Unfiltered
R10	AT7	AT7	Unfiltered
R11	AV7	AV7	Unfiltered
R12	AT9	Base-collector of Q8 temperature ”diode”	Jumper JP62 can disconnect
R13	AG9	AG9	Unfiltered
R14	AC9	AC9	Optional filtering available
R15	PUB	SW7	Pressing SW7 momentarily takes R15 to GND
R16	VCCIB2	VMV2	Tied to 3.3V_FPGA
T1	GND	GND	Tied to GND

Table A-1. AFS600-FG256 Pin Connections for Fusion Starter Kit Board (Continued)

Pin Number	Pin Name	Starter Kit Function	Notes
T2	NCAP	NCAP	
T3	VCC33N	VCC33N	Available on header pin
T4	ATRTN0	ATRTN0	
T5	AT3	AT3	Unfiltered
T6	ATRTN1	ATRTN1	Unfiltered
T7	AT4	AT4	Unfiltered
T8	ATRTN2	ATRTN2	Unfiltered
T9	AT6	AT6	Unfiltered
T10	ATRTN3	ATRTN3	Unfiltered
T11	AT8	AT8	Unfiltered
T12	ATRTN4	Emitter of Q8 temperature "diode"	Jumper JP68 can disconnect
T13	GNDA	GNDA	Analog ground is on a separate plane and joined to digital ground at regulator U15 ground pins
T14	VCC33ACAP	VCC33ACAP	
T15	VAREF	User VAREF	Shrouded header JP74 can be used to supply User VAREF
T16	GND	GND	Tied to GND

B

Board Schematics

This appendix provides illustrations of the Fusion Evaluation Board.

Top-Level View

Figure B-1 on page 48 illustrates a view of the top of the Fusion Evaluation Board. Figure B-2 on page 49 and Figure B-3 on page 50 illustrate views of the bottom of the Fusion Evaluation Board.

Fusion Schematics

The last pages of this appendix show the following illustrations of the Fusion Starter Kit board in order.

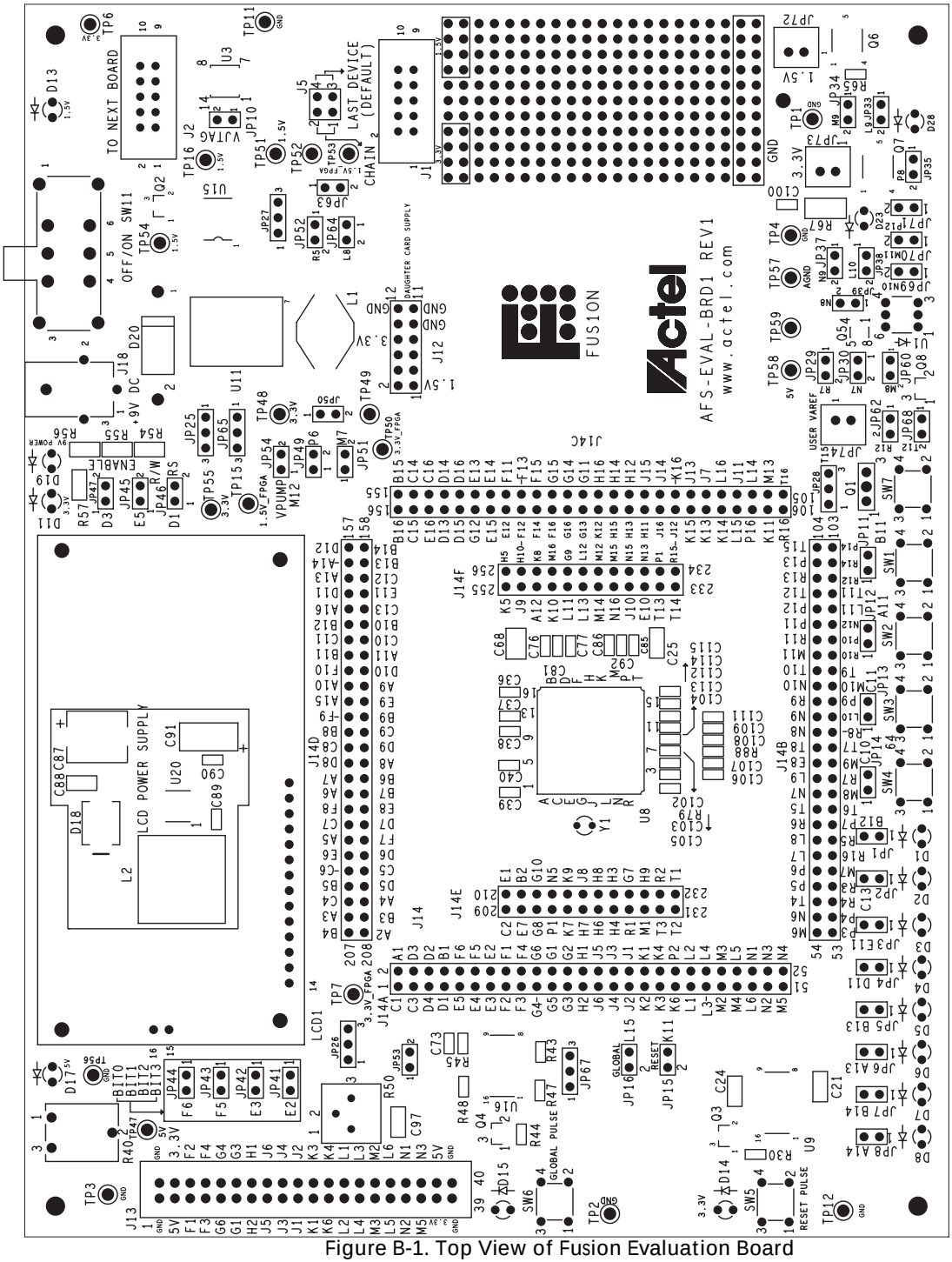

Figure B-1. Top View of Fusion Evaluation Board

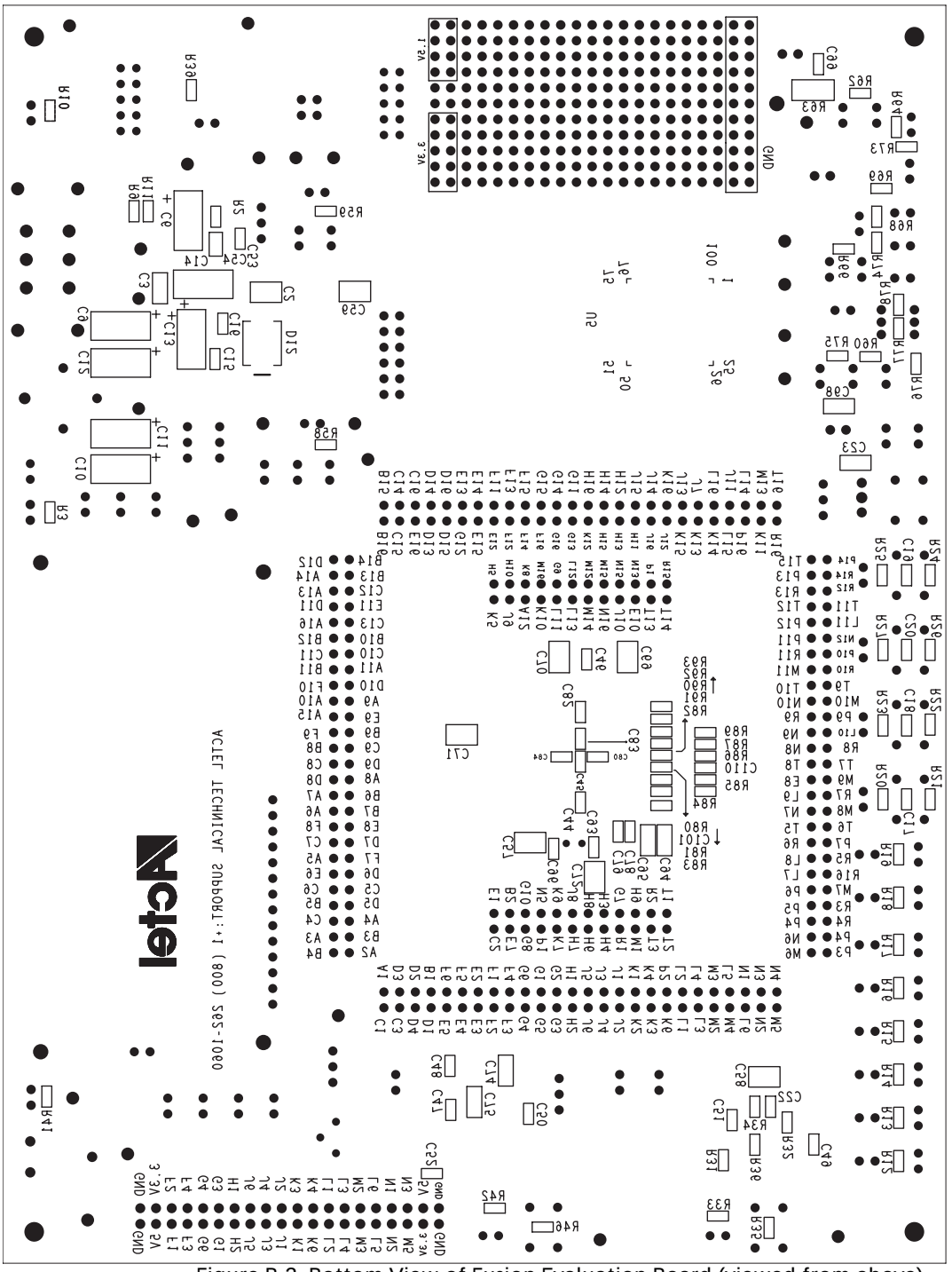

Figure B-2. Bottom View of Fusion Evaluation Board (viewed from above)

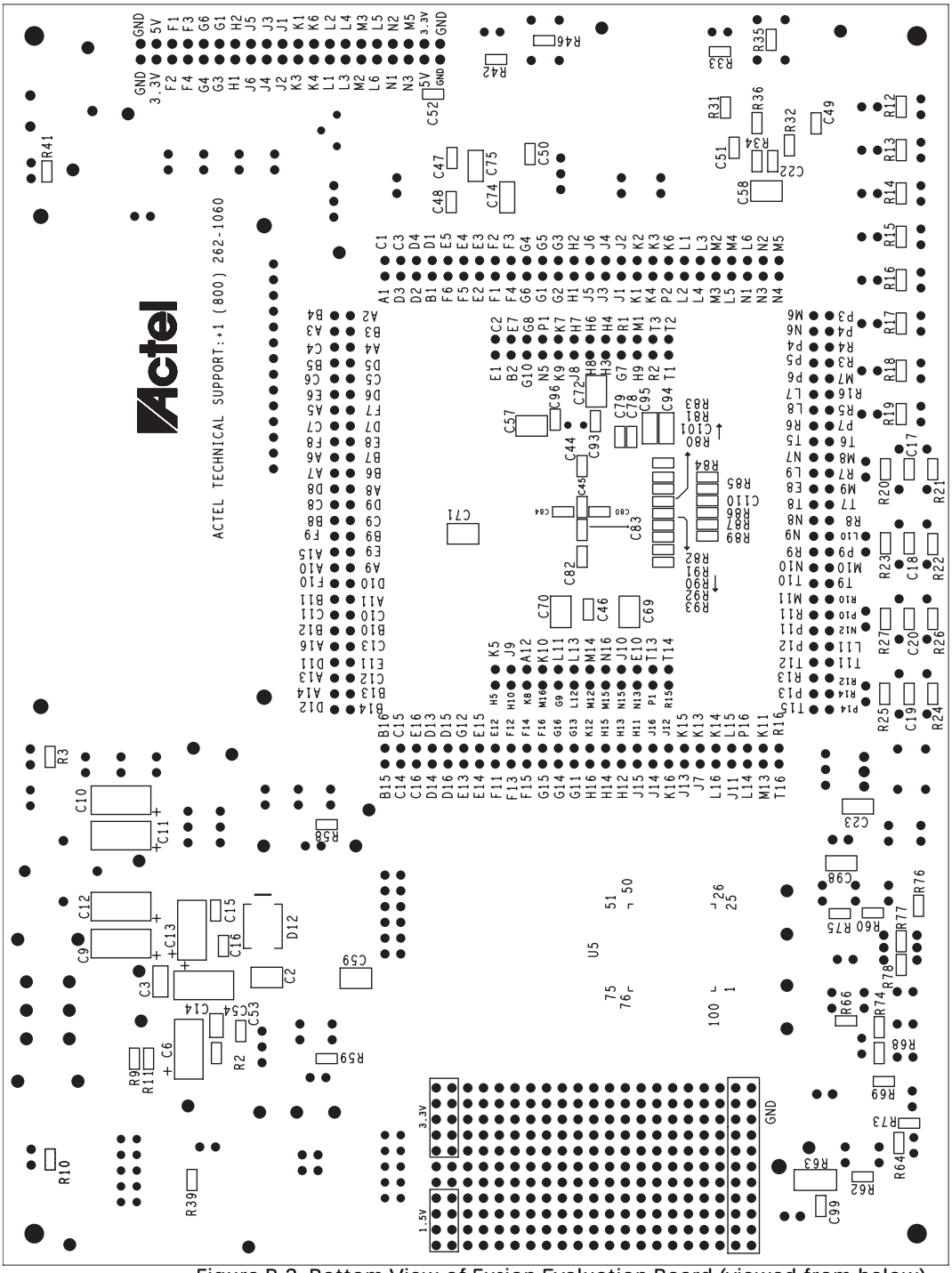

Figure B-3. Bottom View of Fusion Evaluation Board (viewed from below)

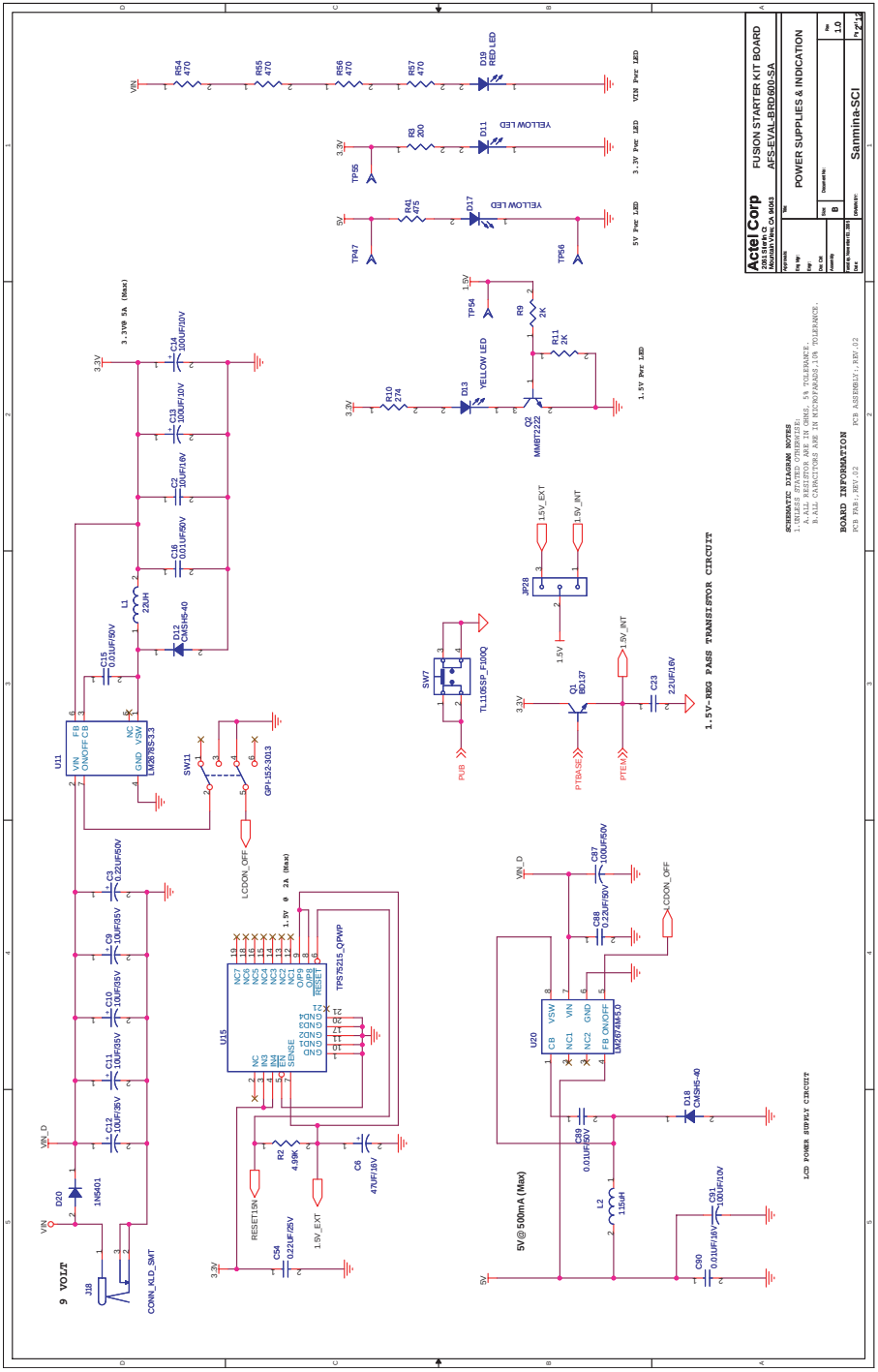

Figure B-4. Power Supplies and Indication

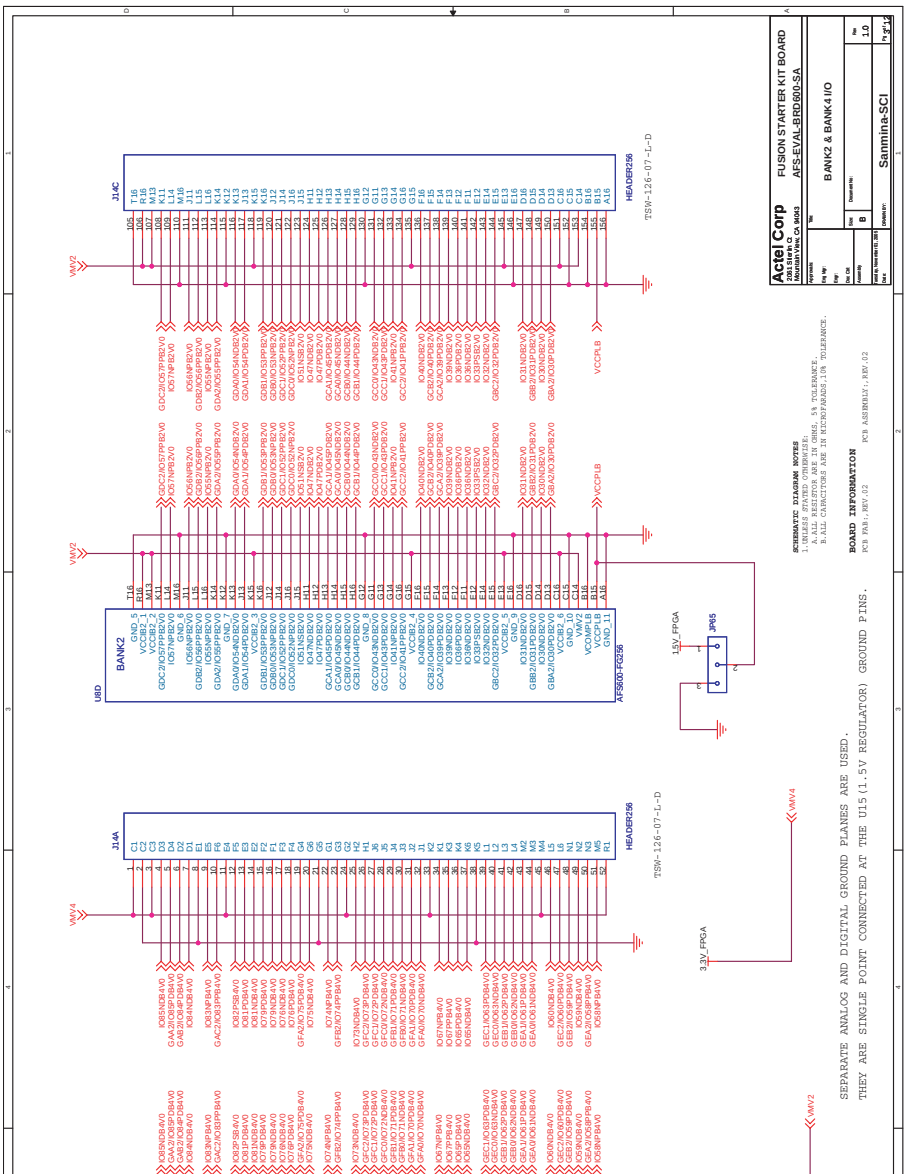

Figure B-5. Bank 2 and Bank 4 I/O

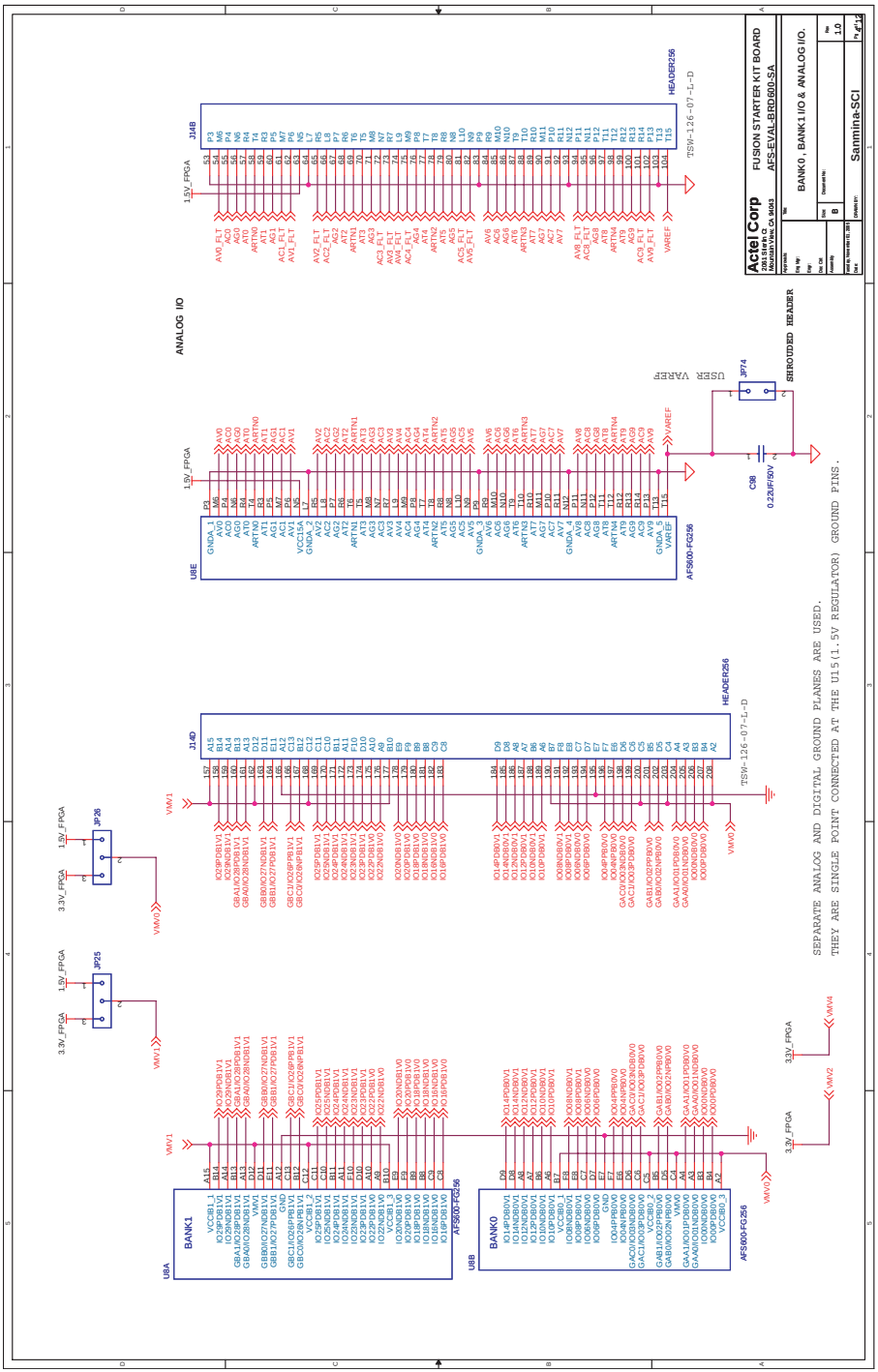

Figure B-6. Bank 0, Bank 1, and Analog I/O

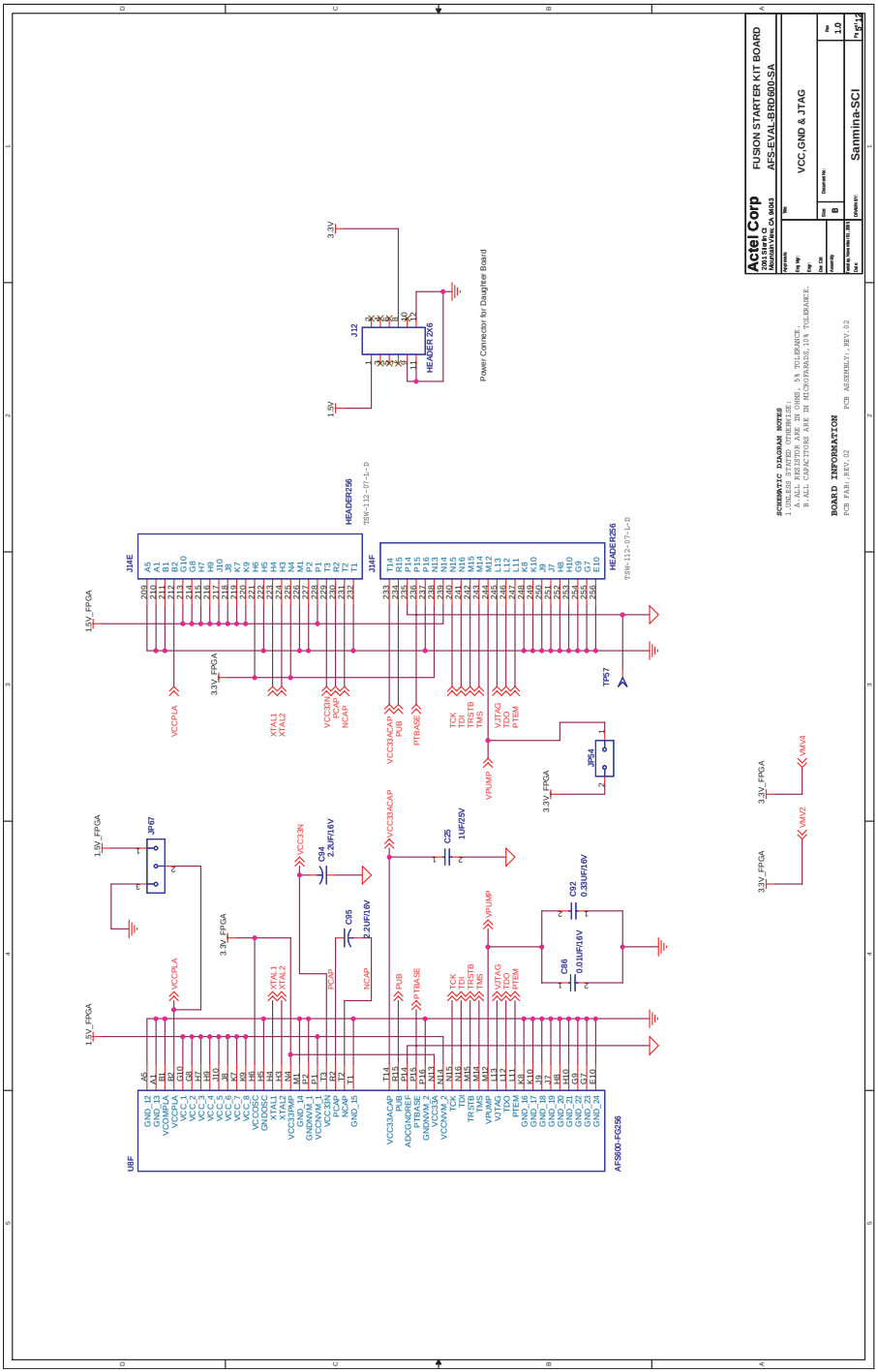

Figure B-7. VCC, GND, and JTAG

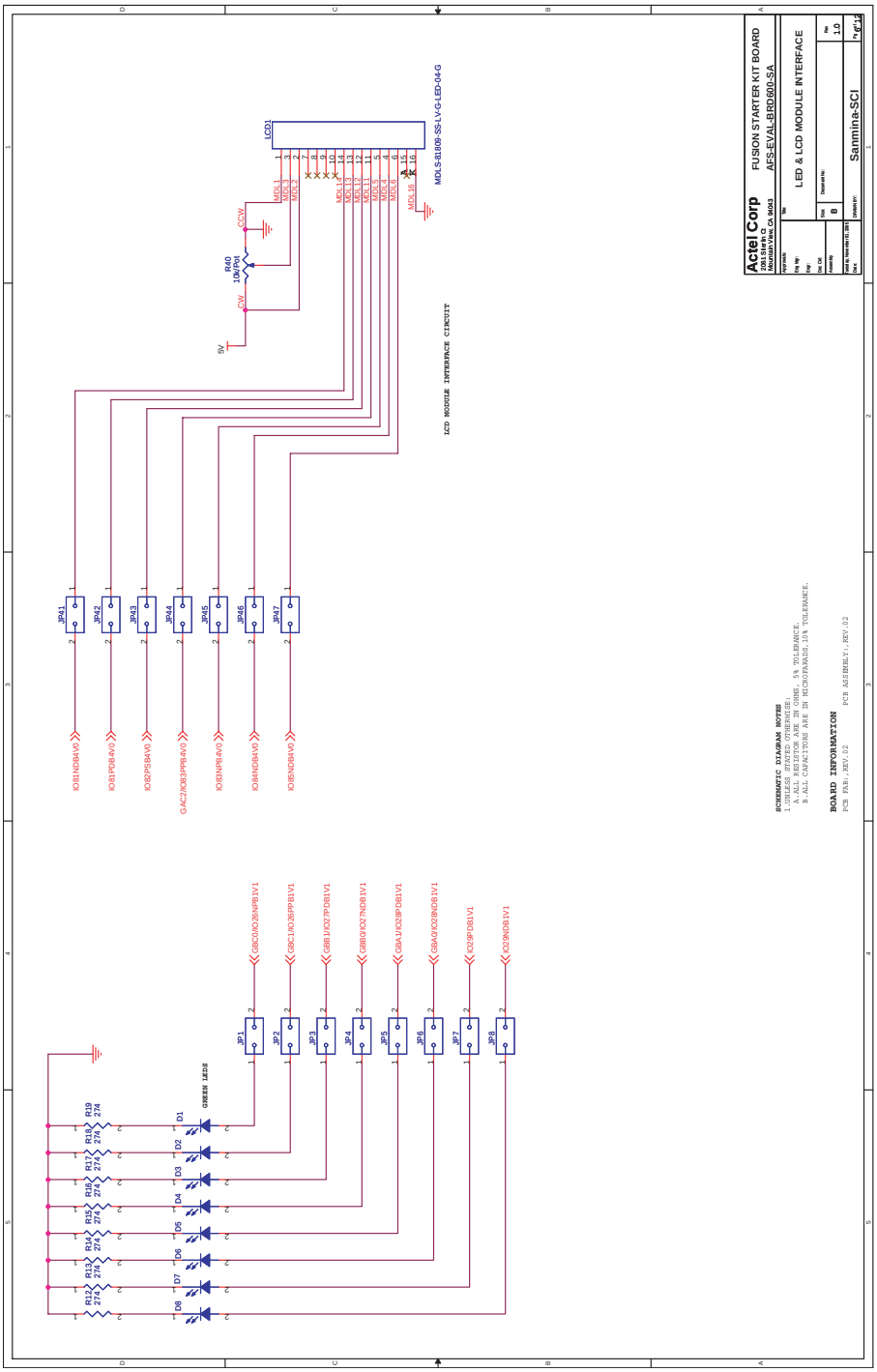

Figure B-8. LED and LCD Module Interface

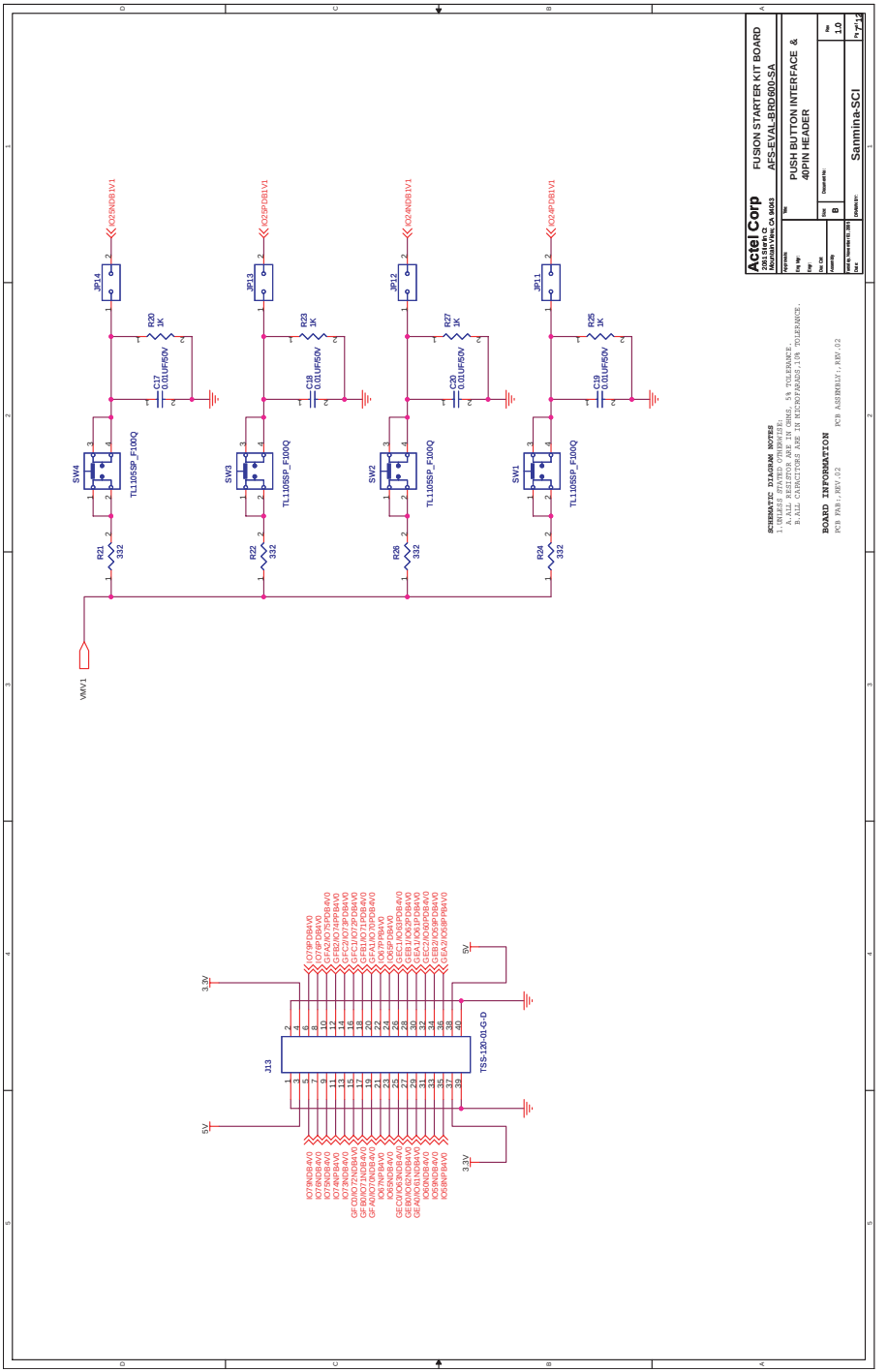

Figure B-9. Push Button Interface and 40-Pin Header

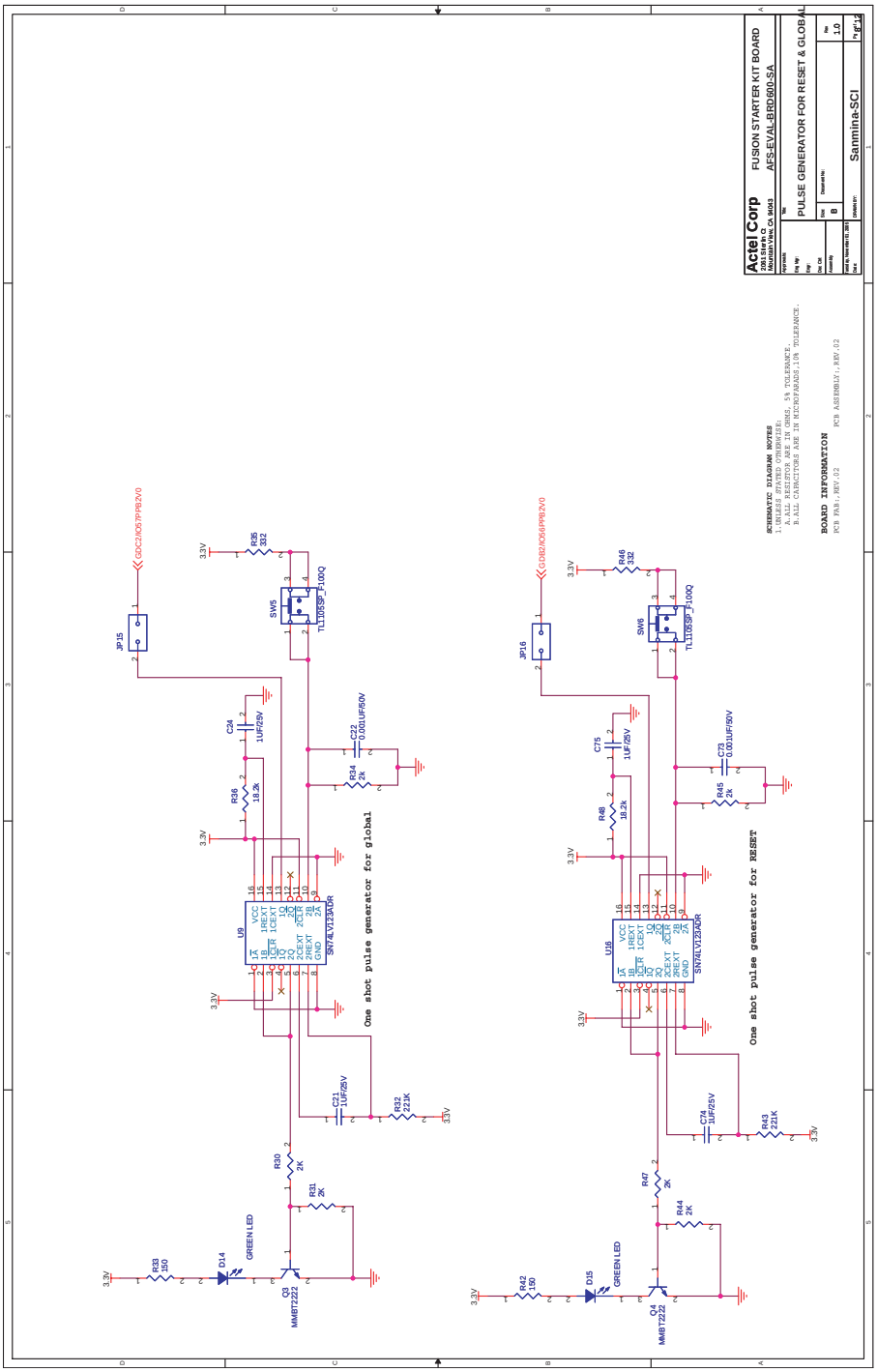

Figure B-10. Pulse Generator for Reset and Global

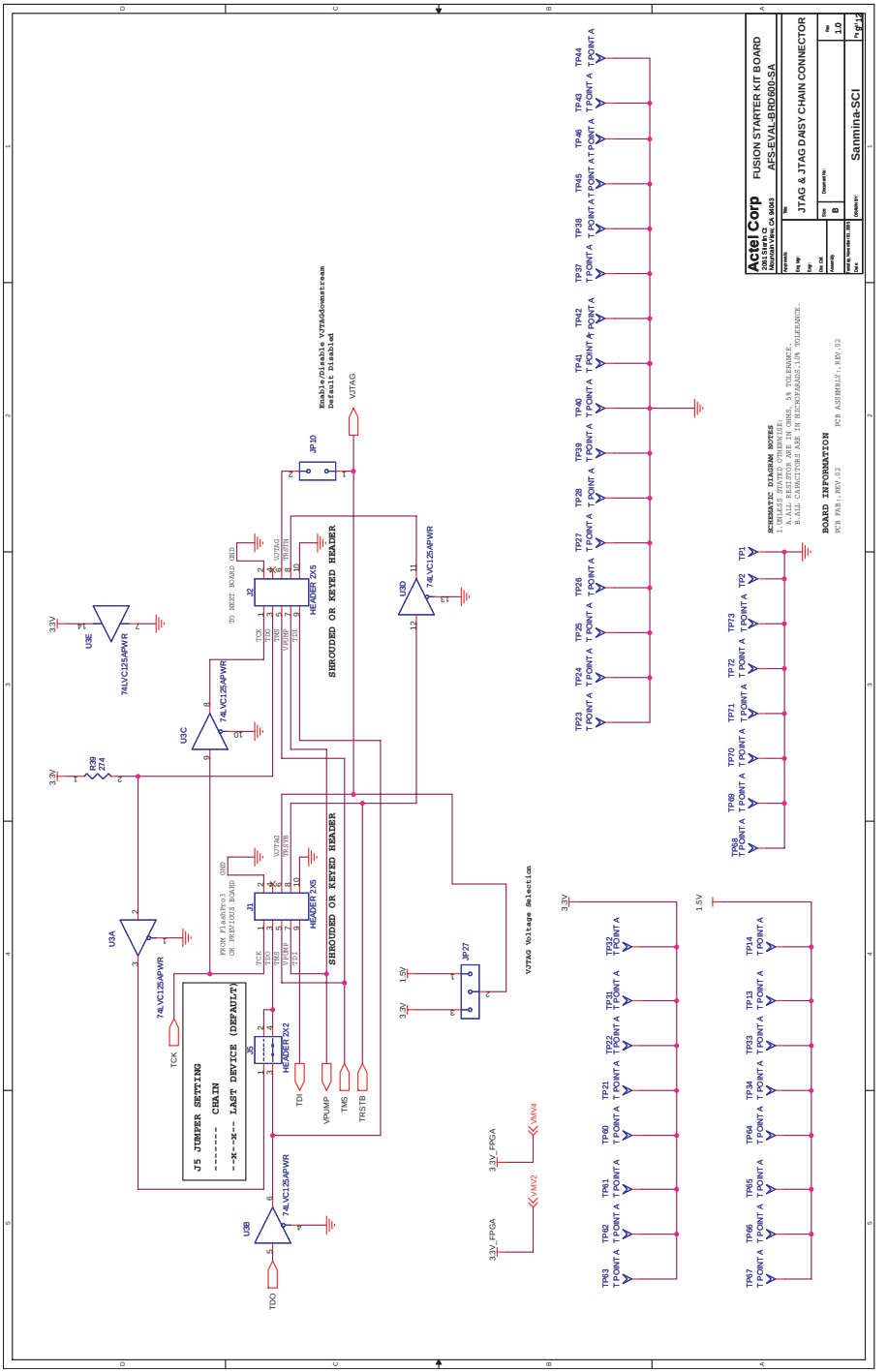

Figure B-11. JTAG and JTAG Daisy Chain Connector

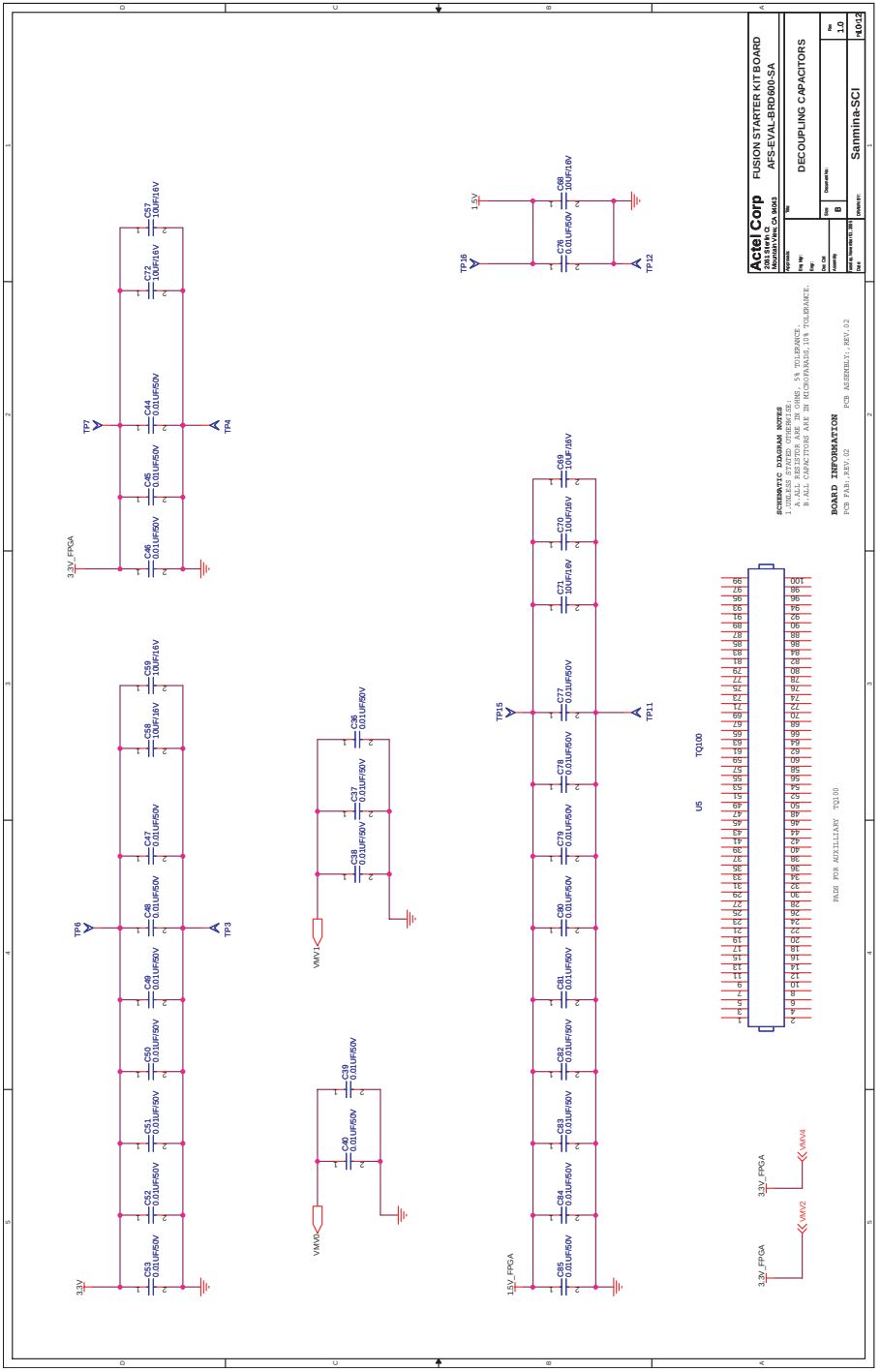

Figure B-12. Decoupling Capacitors

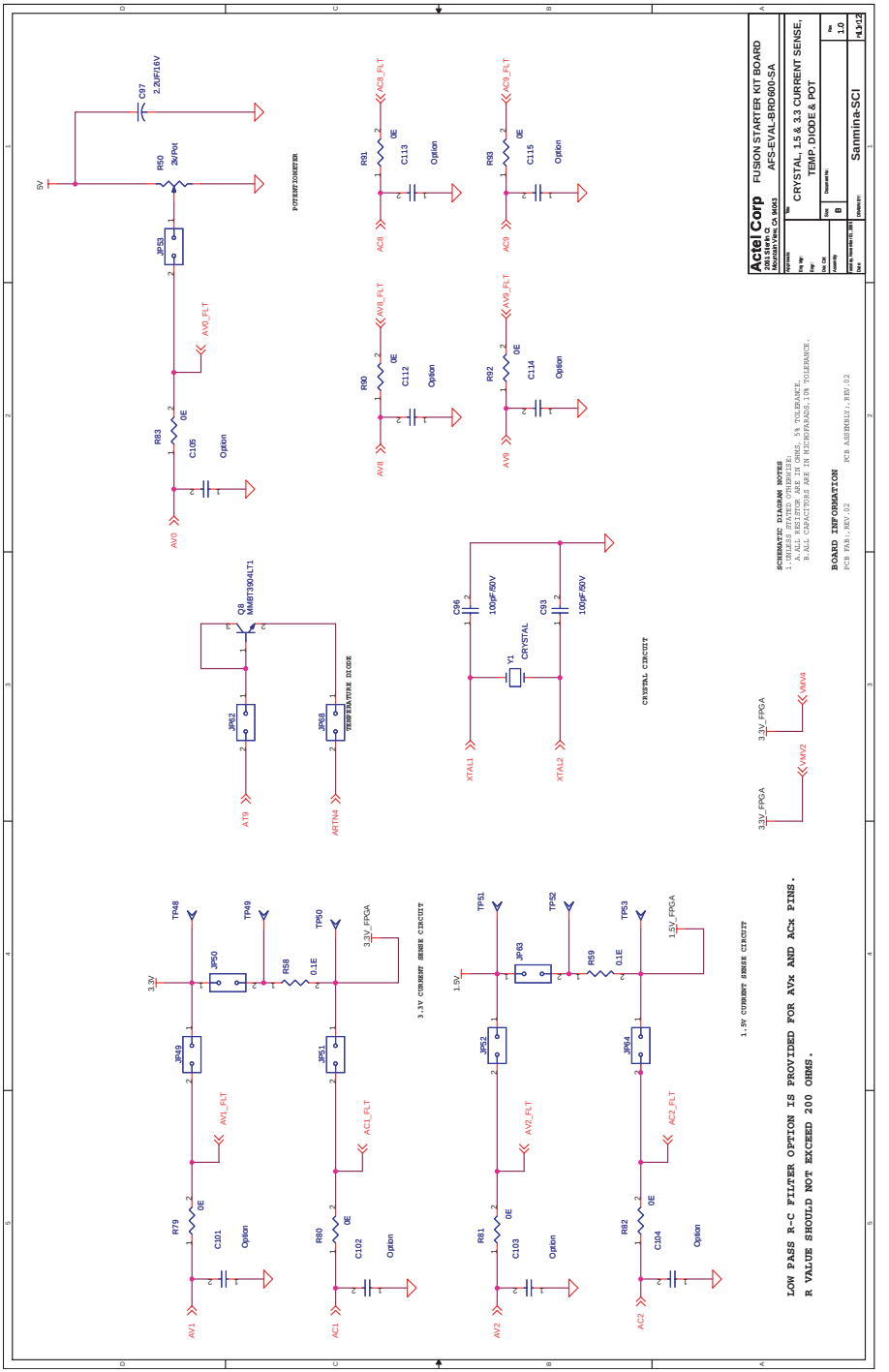

Figure B-13. Crystal, 1.5 V and 3.3 V Current Sense, Temperature Diode, and Pot

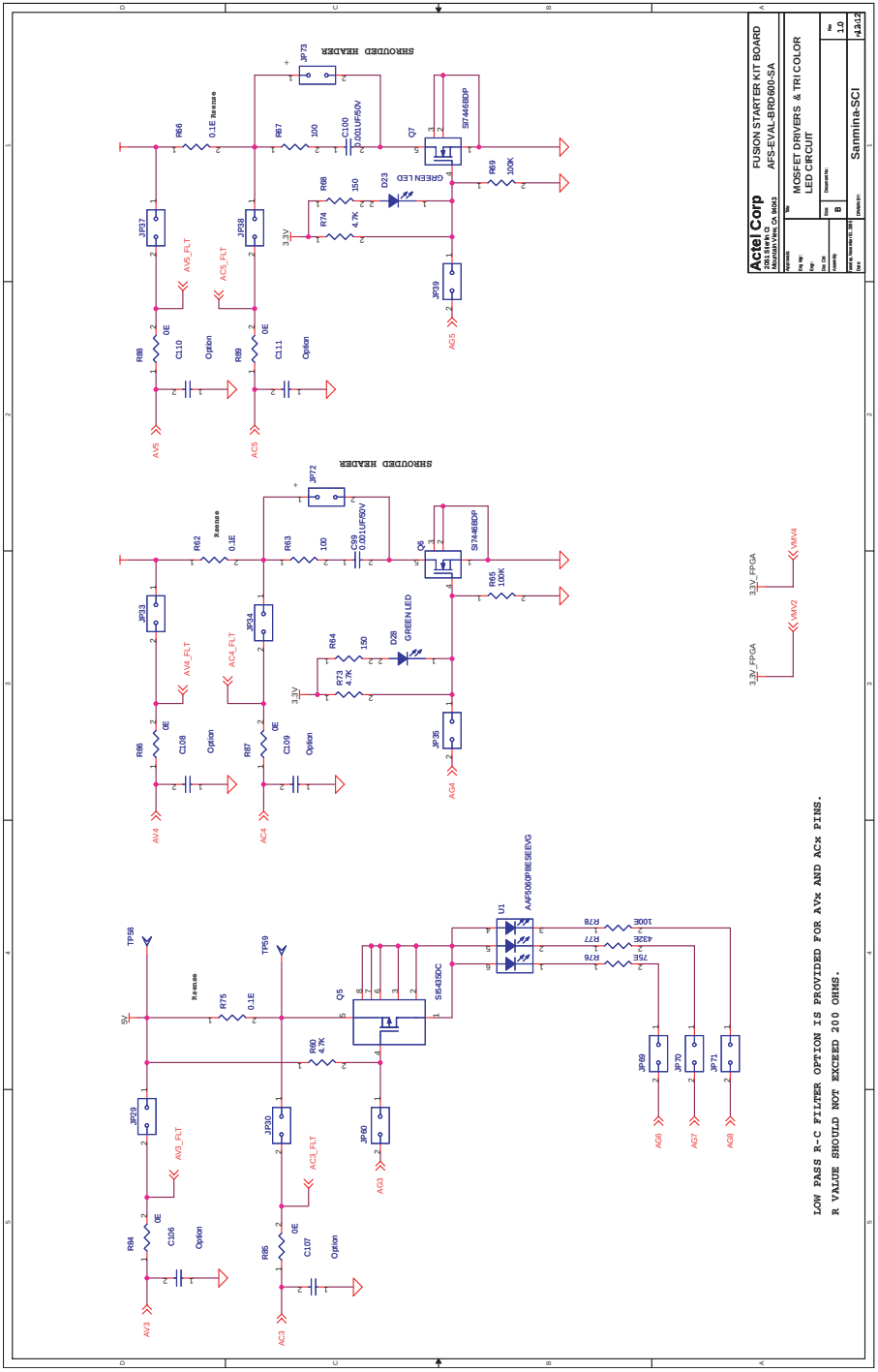

Figure B-14. MOSFET Drivers and Tricolor LED Circuit

C

Signal Layers

The Fusion Evaluation Board is a six-layer board, with the following layers of copper:

- Layer 1 – Top signal layer (see Figure C-1 on page 64)
- Layer 3 – Signal layer 3, for LVDS receive and other signals (see Figure C-2 on page 65)
- Layer 4 – Signal layer 4, for LVDS transmit and other signals (see Figure C-3 on page 66)
- Layer 6 – Bottom signal layer (see Figure C-4 on page 67 and Figure C-5 on page 68)

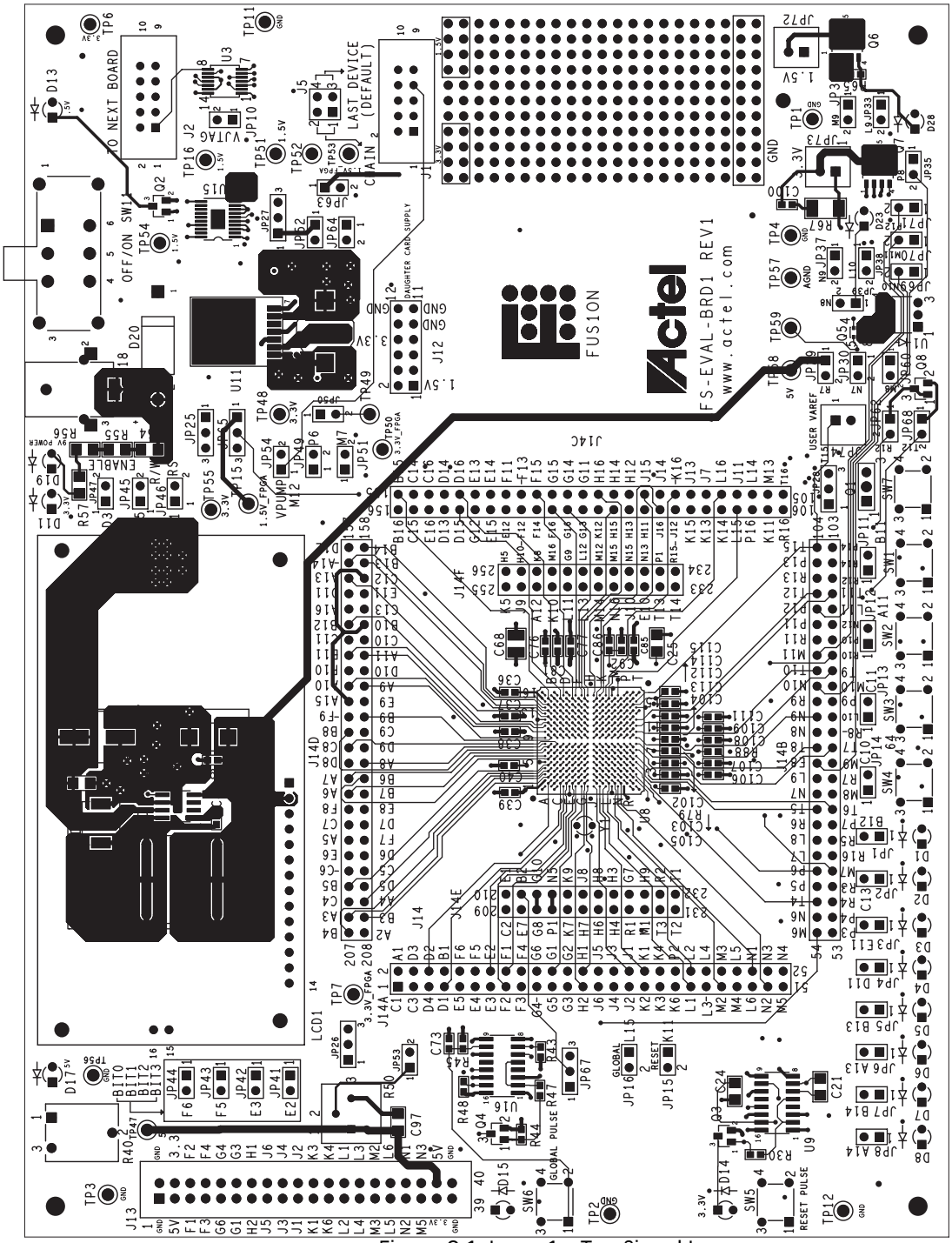

Figure C-1. Layer 1 – Top Signal Layer

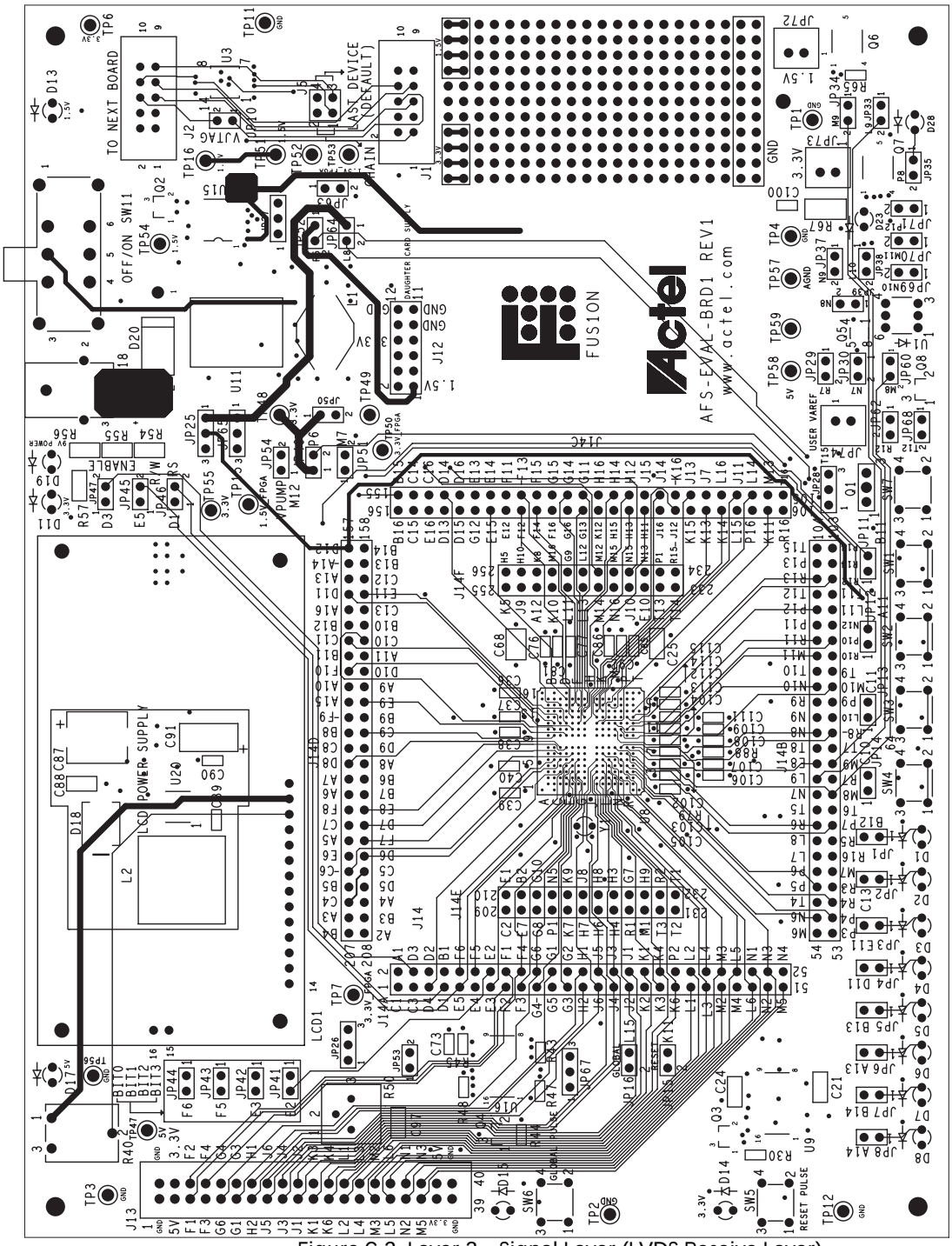

Figure C-2. Layer 3 – Signal Layer (LVDS Receive Layer)

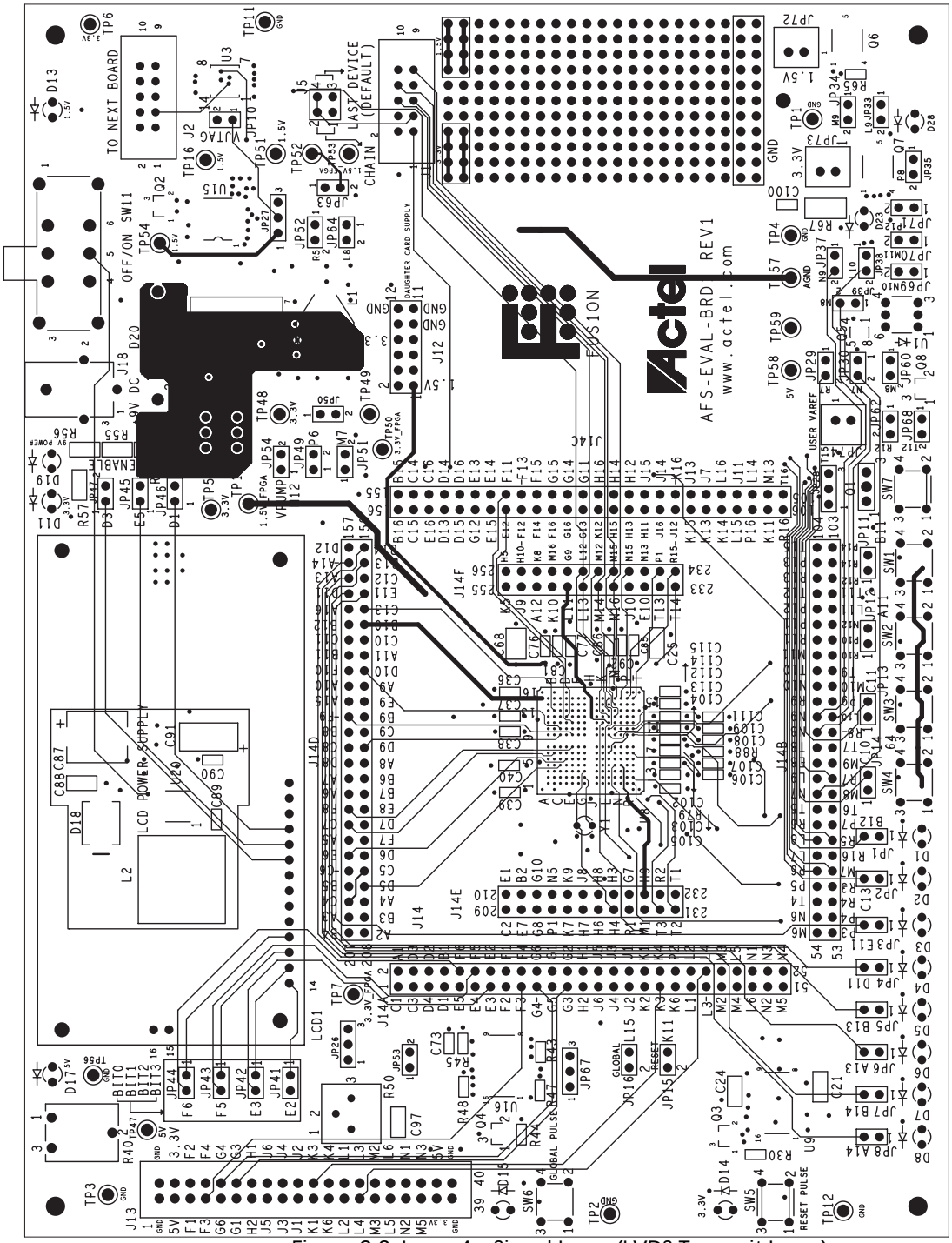

Figure C-3. Layer 4 – Signal Layer (LVDS Transmit Layer)

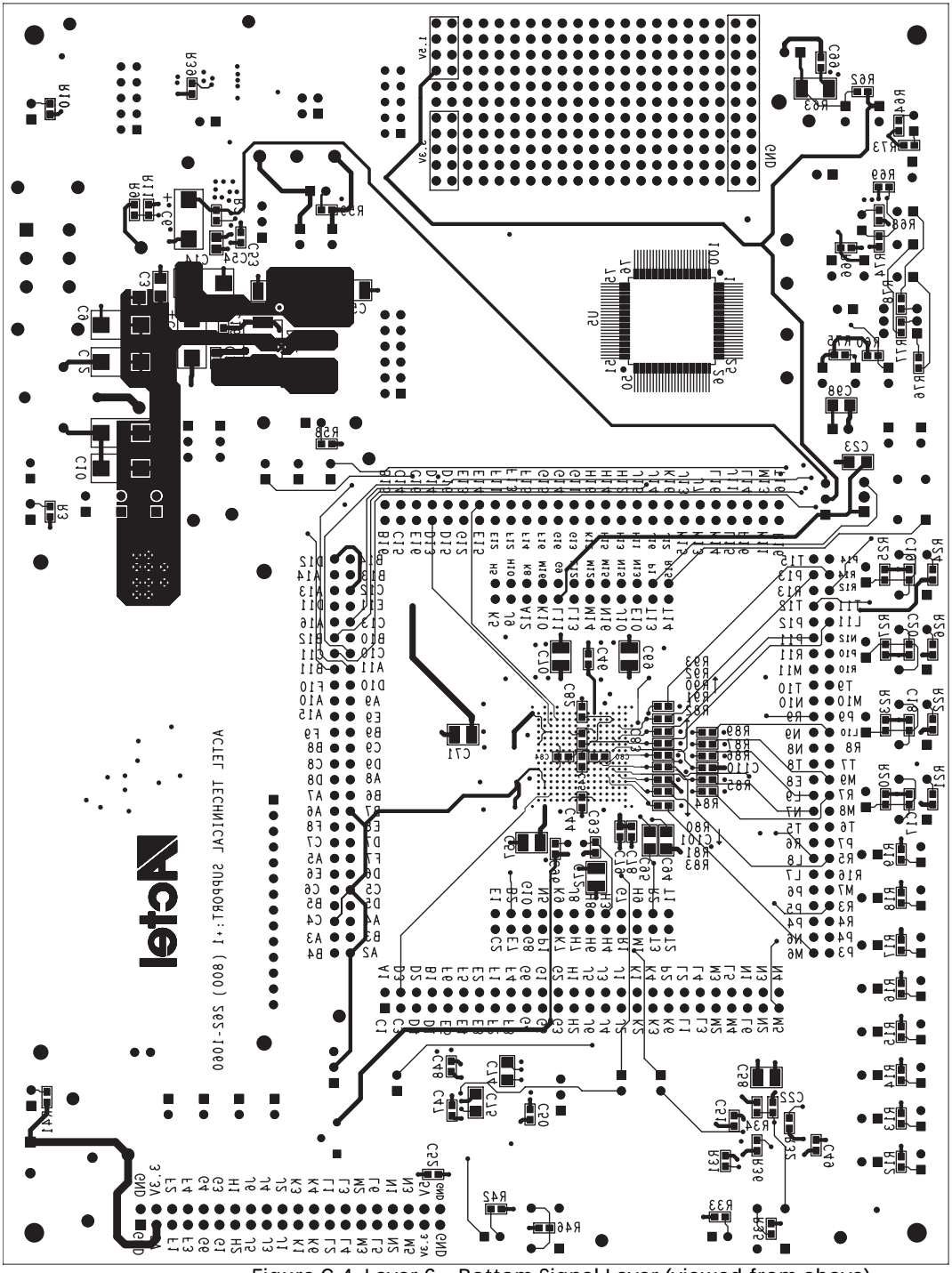

Figure C-4. Layer 6 – Bottom Signal Layer (viewed from above)

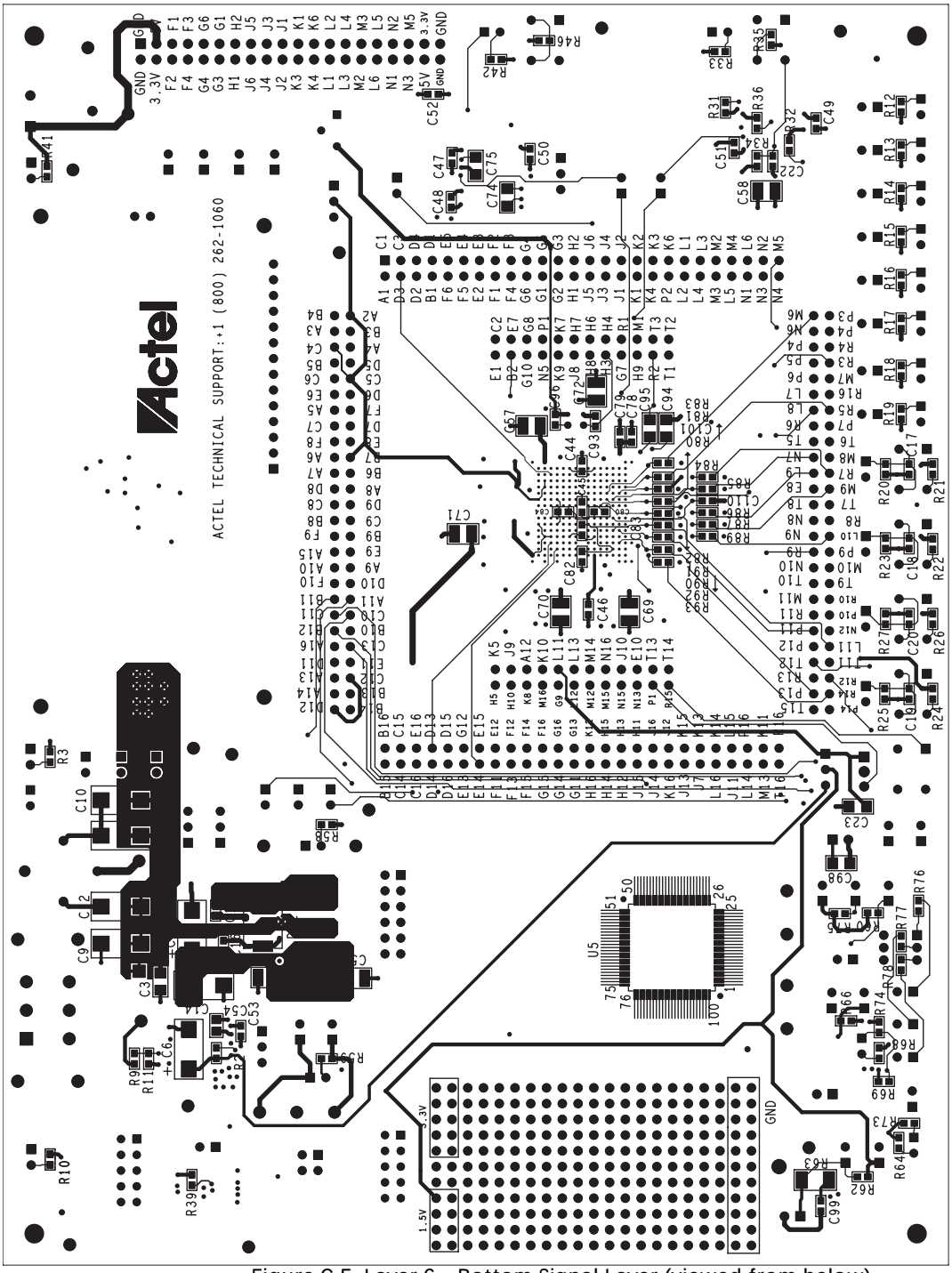

Figure C-5. Layer 6 – Bottom Signal Layer (viewed from below)

D

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650.318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/contact/offices/index.html.

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