Live at Power-Up

The Time it Takes an FPGA to Power Up has a Significant Impact on Effective System Design and the Total System Cost

Key Actel Benefits

- Level 0, Best in Class, Live at Power-Up (LAPU) Support
- Operational Before Power-Up
- Orders of Magnitude Faster Power-On than Competitors
- Short System Initialization Time
- Reduction of System Power-Up Components
- Effective and Robust System Design
- Reduced Total Cost of Ownership

Applications that require short initialization time cannot wait for device configuration upon power-up. Actel Flash and antifuse FPGAs are the only FPGA device technology to support the best in class, Level 0, live at power-up (LAPU) classification and are orders of magnitude faster to power-on than their nearest competitors.

Unlike SRAM-based FPGAs, Actel devices do not require reloading when system power is restored; glitches and brownouts in system power will not corrupt the Actel device configuration. As a result, there is no need for a configuration PROM, a power sequencing device, brownout detection, reset controller, and clock generator devices in the printed circuit board (PCB) design.

Actel nonvolatile Level 0 LAPU FPGAs speed initialization of system components and execute critical tasks up to 4,000 times sooner than SRAM or Hybrid FPGAs, and before the processor powers up and initializes. Critical tasks include setup and configuration of memory blocks, clock generation, synthesis and distribution, and bus activity management. The live at power-up capability of Actel nonvolatile devices greatly simplifies total system design and reduces total system cost. Using live at power-up Actel FPGAs instead of SRAM or Hybrid FPGAs often eliminates the need for Complex Programmable Logic Devices (CPLDs), clock generation devices, and external PLLs.

Programmable Logic Technologies

Programmable logic devices require configuration to initialize the device and operate according to the customer application.

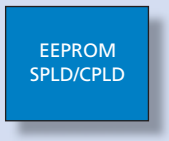
Technologies currently used in programmable logic devices differ in the way the device is configured when power is applied. Programmable logic devices, based on nonvolatile memory technologies, such as Flash and antifuse, store their configuration in the logic gates. This eliminates the need to download the configuration, making these devices readily available for operation in a similar way to standard semiconductor devices (ASIC/ASSPs).

Other technologies, such as the volatile SRAM-based programmable logic devices, wake up in an unknown state and require the download of configuration from an external nonvolatile memory device on each power-up cycle. Hybrid SRAM devices have SRAM FPGA architecture and nonvolatile configuration memory on-chip. These FPGAs must be loaded internally on each power-up cycle. Only after the device is loaded with the configuration can it start operating according to the customer application. After each power-down or brownout, the device loses its configuration and needs to be loaded again in the next power-up cycle.

Nonvolatile Technologies (Flash, Antifuse, EEPROM)

Configuration bits are embedded in the device, and there is no need to configure the device on power-up

EEPROOM
SPLD/CPLDs – EEPROM

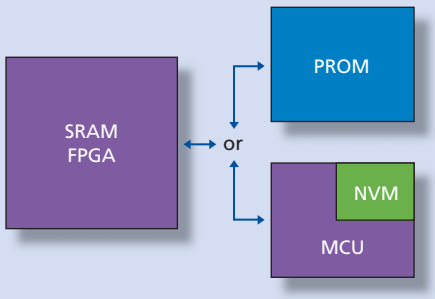


Flash/Antifuse
Nonvolatile Memory (NVM) FPGAs

SRAM Technology

Programmed on every system power-up using external memory

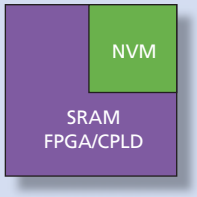
SRAM
SRAM FPGAs with boot (PROM or MCU) – These Level 2 devices are typically 3 or 4 orders of magnitude slower than Level 0 Actel FPGAs.



Hybrid SRAM and Nonvolatile Technology

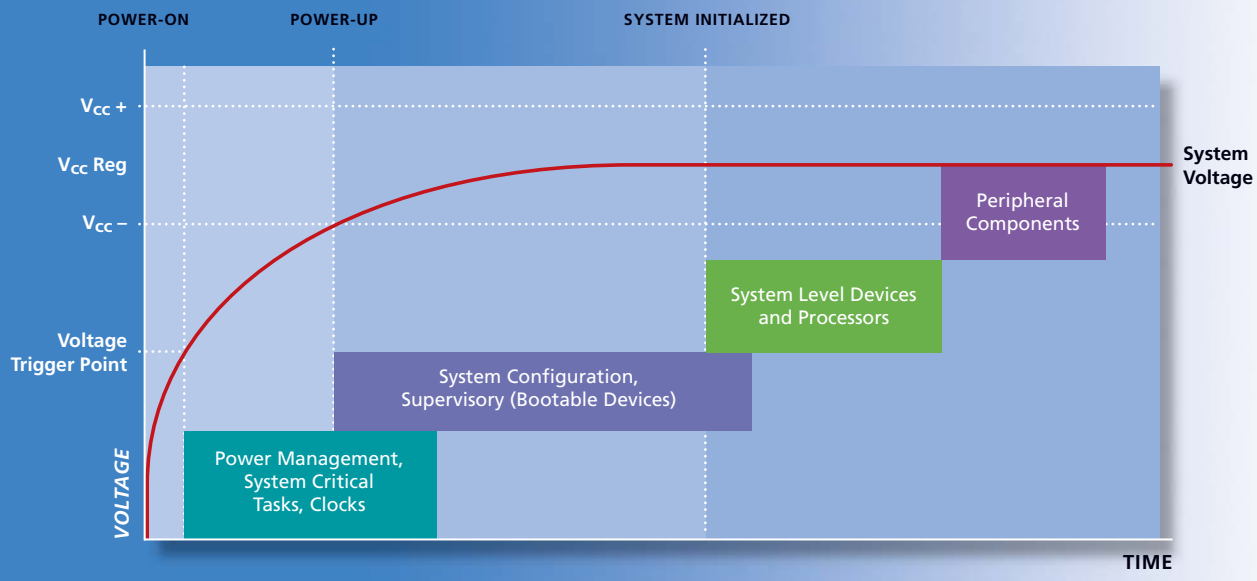
Programmed on every system power-up from internal nonvolatile memory (NVM) block

SRAM
Hybrid FPGAs/CPLDs – SRAM FPGA fabric loaded from on-chip NVM. These Level 1 devices are typically 2 orders of magnitude slower than Level 0 Actel FPGAs.



Power-Up Device Classification

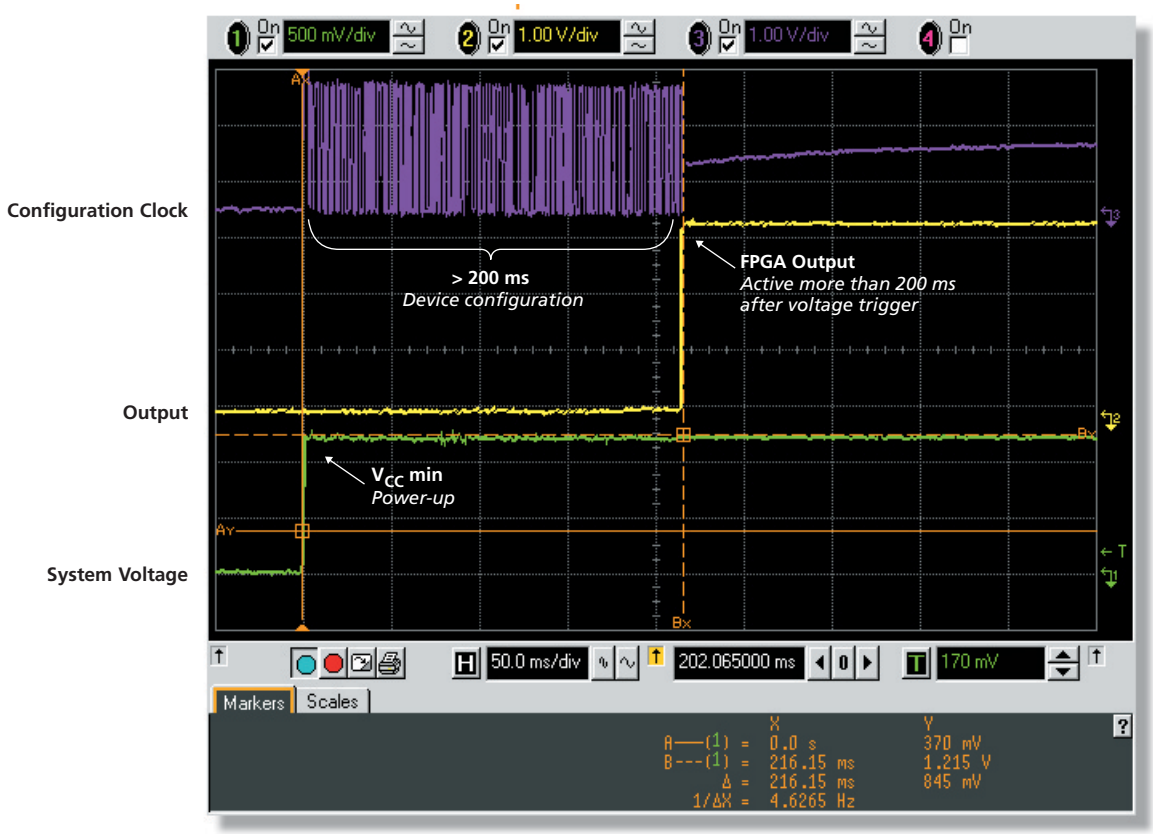
Typical system power-up sequence and device operation in each stage with a single "critical" supply voltage



	POWER-ON	POWER-UP	SYSTEM INITIALIZED
Level	0	1	2
Level Description	Live at power-up	Live after power-up	Live after system initialization
Activity	Regulates critical tasks for system environment setup. Provides clocks and critical logic functions during power ramp-up until system is powered up	System configuration and initialization, supervisory, and monitoring tasks. Set up memories and interfaces for microprocessors access	Processor initialization (boot) after environment setup. Periphery component setup least critical to system operation
Device that Can Be Used at this Level	• NVM FPGAs (Flash and antifuse) • Some CPLDs • ASICs • Some ASSPs	• Hybrid CPLDs/FPGAs (SRAM plus NVM) • Some ASSPs	• SRAM-based FPGAs loaded from boot PROM or from microcontroller/processor • Processor

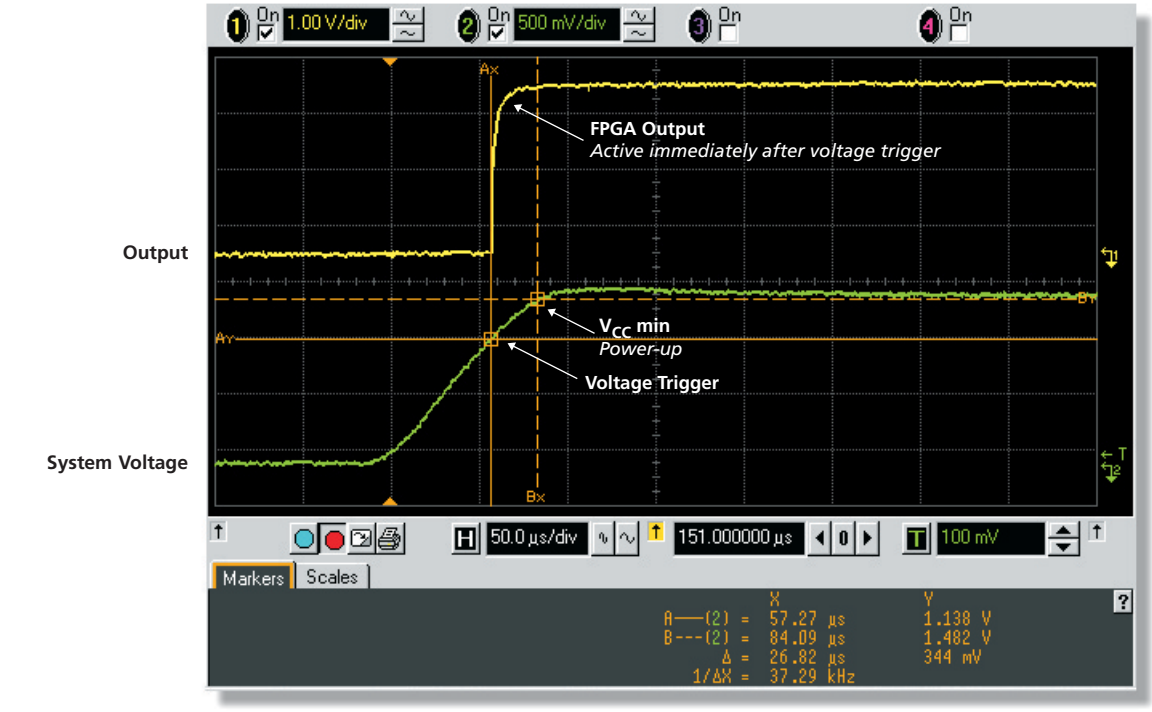
SRAM FPGA Power-Up Behavior

Operational hundreds of milliseconds after power-up – Meets Level 2 LAPU classification



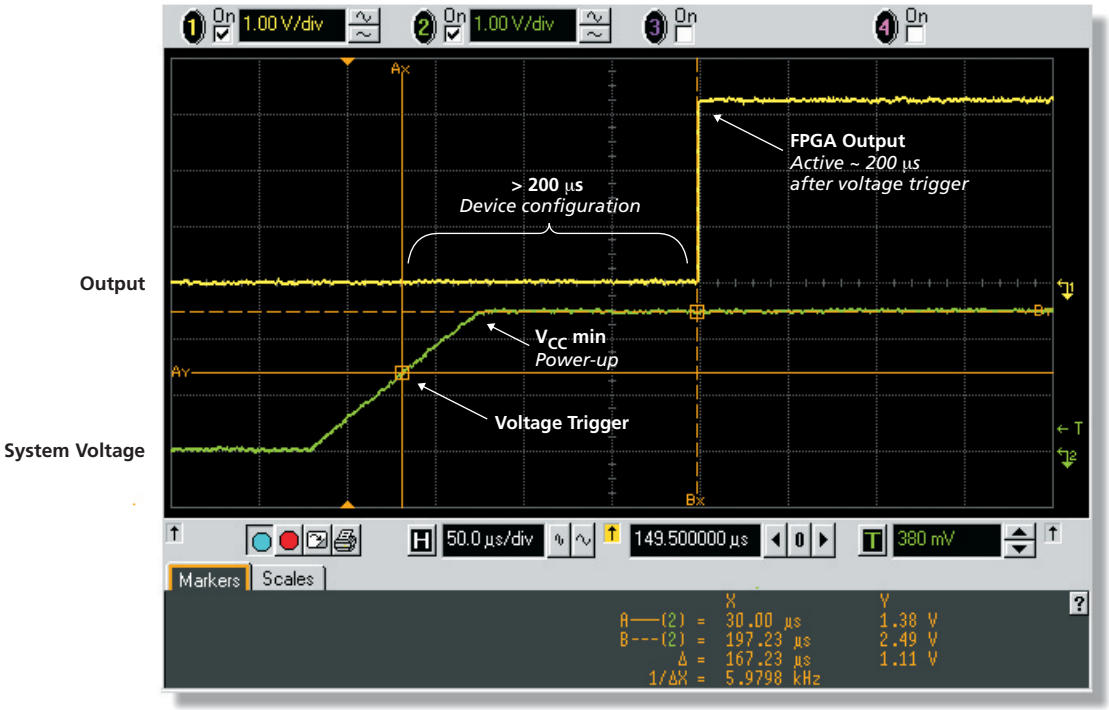
Nonvolatile Antifuse FPGA Power-Up Behavior

Operational before power-up – Meets Level 0 LAPU classification



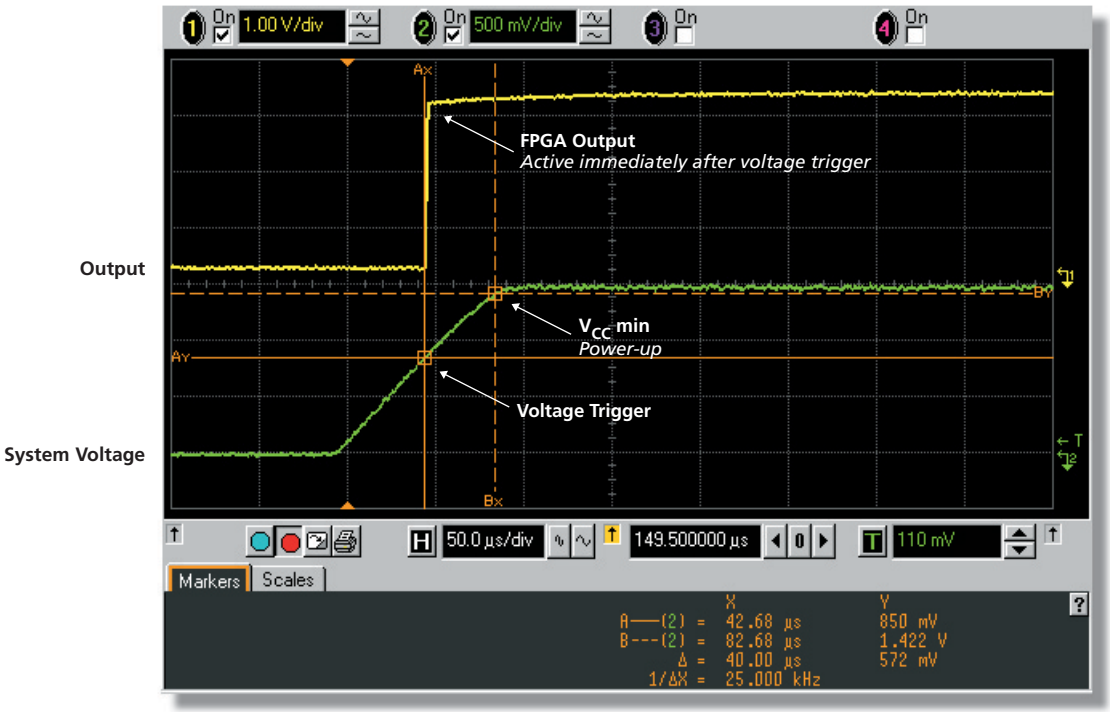
Hybrid (SRAM plus NVM) FPGA Power-Up Behavior

Active hundreds of microseconds after power-up – Meets Level 1 LAPU classification



Nonvolatile ProASIC3/E Flash FPGA Power-Up Behavior

Operational before power-up – Meets Level 0 LAPU classification



Actel nonvolatile devices are the only FPGAs that comply with Level 0 LAPU classification, while SRAM FPGAs meet only Level 2, and Hybrid (SRAM plus NVM) FPGAs meet Level 1. This SRAM and Hybrid FPGA deficiency leads to complex design requirements, additional components on-board, more design time, and increased overhead. Often these devices' inability to operate immediately at power-up prevents them from being used in applications where system initialization time is critical. Actel FPGAs address system design requirements and can be used in applications requiring short system initialization time.

Actel Level 0 LAPU devices assist in system start-up tasks, system configuration, and supervision during voltage ramp-up. With an Actel device on your board, you do not need additional live at power-up circuitry and the device is ready when you most need it, at power-up.

For more information regarding **Actel Flash and Antifuse FPGAs Supporting Level 0 Live at Power-Up (LAPU) Classification**, please contact your local **Actel** sales representative.

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