DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in the Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-2.

Table 3-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CC}	DC core supply voltage	–0.3 to 1.65	V
V_{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V_{PUMP}	Programming voltage	–0.3 to 3.75	V
V_{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V_{CCI}	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V_{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage Temperature	–65 to +150	°C
T_J [2]	Junction Temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-3 on page 3-2.*
2. *For Flash programming and retention maximum limits refer to Table 3-4 on page 3-2 and for recommended operating limits refer to Table 3-2 on page 3-2.*

Table 3-2 • **Recommended Operating Conditions**

Symbol	Parameter		Commercial	Industrial	Units
T_A, T_J	Ambient and Junction temperature		0 to +70	–40 to +85	°C
V_{CC}	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
V_{JTAG}	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
V_{PUMP}	Programming voltage	Programming Mode	3.0 to 3.6	3.0 to 3.6	V
		Operation[3]	0 to 3.6	0 to 3.6	V
V_{CCPLL}	Analog power supply (PLL)		1.4 to 1.6	1.4 to 1.6	V
V_{CCI} and VMV	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS/BLVDS/M-LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 3-13 on page 3-15. VMV and V_{CCI} should be at the same voltage within a given I/O bank.*
2. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
3. *V_{PUMP} can be left floating during normal operation (not programming mode).*

Table 3-3 • **Flash Programming Limits - Retention, Storage and Operating Temperature[1]**

Product Grade	Programming Cycles	Program Retention (Biased/Unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	110
Industrial	500	20 years	110	110

Notes:

1. *This is a stress rating only, functional operation at any other condition other than those indicates is not implied.*
2. *These limits apply for program/data retention only. Refer to tables 3-1 and 3-2 for device operating conditions and absolute limits.*

Table 3-4 • **Overshoot and Undershoot Limits (as measured on quiet I/Os)[1]**

V_{CCI} and VMV	Average V_{CCI}-GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot)[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one cycle out of six clock cycles (estimated SSO density over cycles). If the overshoot/undershoot occurs at 1 out of 2 cycles, then the maximum overshoot/undershoot has to be reduced by 0.15 V.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC3E device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power-up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 3-1.

There are five regions to consider during power-up.

ProASIC3E I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points (Figure 3-1).
2. $V_{CCI} > V_{CC}$ - 0.75 V (Typical).
3. Chip is in the operating mode.

V_{CCI} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation.

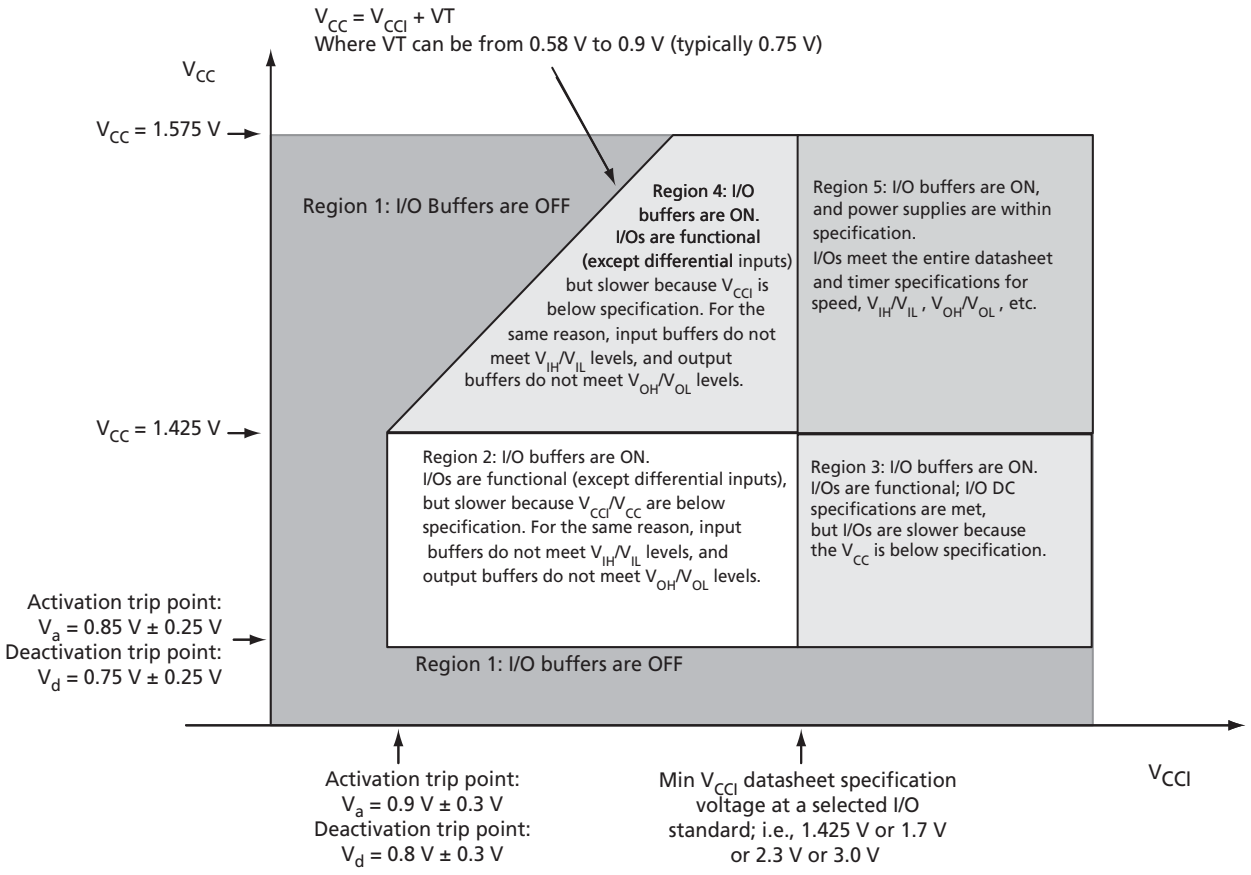

Figure 3-1 • **I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 3-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A \qquad \textit{EQ 3-1}$$

Where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 3-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 3-2 shows a sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{13.6\text{°C/W}} = 5.88\ \text{W} \qquad \textit{EQ 3-2}$$

Table 3-5 • **Package Thermal Resistivities**

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./min.	500 ft./min.	
Plastic Quad Flat Package (PQFP)	208	8.0	26.1	22.5	20.8	C/W
Plastic Quad Flat Package (PQFP) with embedded heat spreader	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.8	26.6	22.8	21.5	C/W
	484	3.2	20.5	17.0	15.9	C/W
	676	3.2	16.4	13.0	12.0	C/W
	896	2.4	13.6	10.4	9.4	C/W

Temperature and Voltage Derating Factors

Table 3-6 • **Temperature and Voltage Derating Factors for Timing Delays (Normalized to T_J = 70°C, V_{CC} = 1.425 V)**

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.87	0.93	0.95	1.00	1.02	1.05
1.500	0.83	0.88	0.90	0.95	0.96	0.99
1.575	0.80	0.84	0.87	0.91	0.93	0.96

Calculating Power Dissipation

Quiescent Supply Current

Table 3-7 • **Quiescent Supply Current Characteristics**

	A3PE600	A3PE1500	A3PE3000
Typical (25°C)	5 mA	12 mA	25 mA
Maximum (Commercial)	30 mA	70 mA	150 mA
Maximum (Industrial)	45 mA	105 mA	225 mA

Notes:

1. *I_{DD} Includes V_{CC}, V_{PUMP}, V_{CCI}, and VMV currents. Values do not include I/O static contribution, which is shown in Table 3-8 and Table 3-9 on page 3-6.*
2. *–F speed grade devices may experience higher standby I_{DD} of up to five times the standard I_{DD} and higher I/O leakage.*

Power per I/O Pin

Table 3-8 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings**

	VMV (V)	Static Power P_{DC2} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	17.39
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	25.51
2.5 V LVCMOS	2.5	–	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.16
1.8 V LVCMOS	1.8	–	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.80
1.5 V LVCMOS (JESD8-11)	1.5	–	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	2.00
3.3 V PCI	3.3	–	18.82
3.3 V PCI – Schmitt trigger	3.3	–	20.12
3.3 V PCI-X	3.3	–	18.82
3.3 V PCI-X – Schmitt trigger	3.3	–	20.12
Voltage-Referenced			
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL +	3.3	2.81	4.14
2.5 V GTL +	2.5	2.57	3.71
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26
Differential			
LVDS/BLVDS/M-LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*
2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 3-9 • **Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings[1]**

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC3} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL/LVCMOS	35	3.3	–	474.70
2.5 V LVCMOS	35	2.5	–	270.73
1.8 V LVCMOS	35	1.8	–	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.55
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
Voltage-Referenced				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential				
LVDS/BLVDS/M-LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	168.02

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC3} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CC} and V_{CCI}.*

Power Consumption of Various Internal Resources

Table 3-10 • **Different Components Contributing to the Dynamic Power Consumption in ProASIC3E Devices**

Parameter	Definition	Device-Specific Dynamic Contributions (µW/MHz)		
		A3PE600	A3PE1500	A3PE3000
P_{AC1}	Clock contribution of a Global Rib	12.77	16.21	19.7
P_{AC2}	Clock contribution of a Global Spine	1.85	3.06	4.16
P_{AC3}	Clock contribution of a VersaTile row	0.88		
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.12		
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.07		
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.29		
P_{AC7}	Contribution of a VersaTile used as a combinatorial module	0.29		
P_{AC8}	Average contribution of a routing net	0.70		
P_{AC9}	Contribution of an I/O input pin (standard dependent)	See Table 3-8 on page 3-5.		
P_{AC10}	Contribution of an I/O output pin (standard dependent)	See Table 3-9 on page 3-6		
P_{AC11}	Average contribution of a RAM block during a read operation	25.00		
P_{AC12}	Average contribution of a RAM block during a write operation	30.00		
P_{AC13}	First contribution of a PLL	4.00		
P_{AC14}	Second contribution of a PLL	2.00		

Note: **For a different output load, drive strength, or slew rate, Actel recommends using the Actel power calculator or SmartPower in Actel Libero IDE software.*

Power Calculation Methodology

The section below describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 3-11 on page 3-10
- Enable rates of output buffers—guidelines are provided for typical applications in Table 3-12 on page 3-10
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 3-12 on page 3-10. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = P_{DC1} + N_{INPUTS} * P_{DC2} + N_{OUTPUTS} * P_{DC3}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{AC4}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in Table 3-11 on page 3-10.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 3-11 on page 3-10.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

P_{AC1}, P_{AC2}, P_{AC3}, and P_{AC4} are device dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1/2 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-11 on page 3-10.

F_{CLK} is the global clock signal frequency.

Combinational Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1/2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-11 on page 3-10.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1/2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-11 on page 3-10.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2/2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-11 on page 3-10.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2/2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-11 on page 3-10.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 3-12 on page 3-10.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 3-12 on page 3-10.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 3-12 on page 3-10.

PLL/CCC contribution—P_{PLL}

$P_{PLL} = P_{AC13} * F_{CLKIN} + \Sigma P_{AC14} * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT}[1] is the output clock frequency.

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift-register is 100% as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - The average toggle rate is = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 3-11 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 3-12 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

User I/O Characteristics

Timing Model

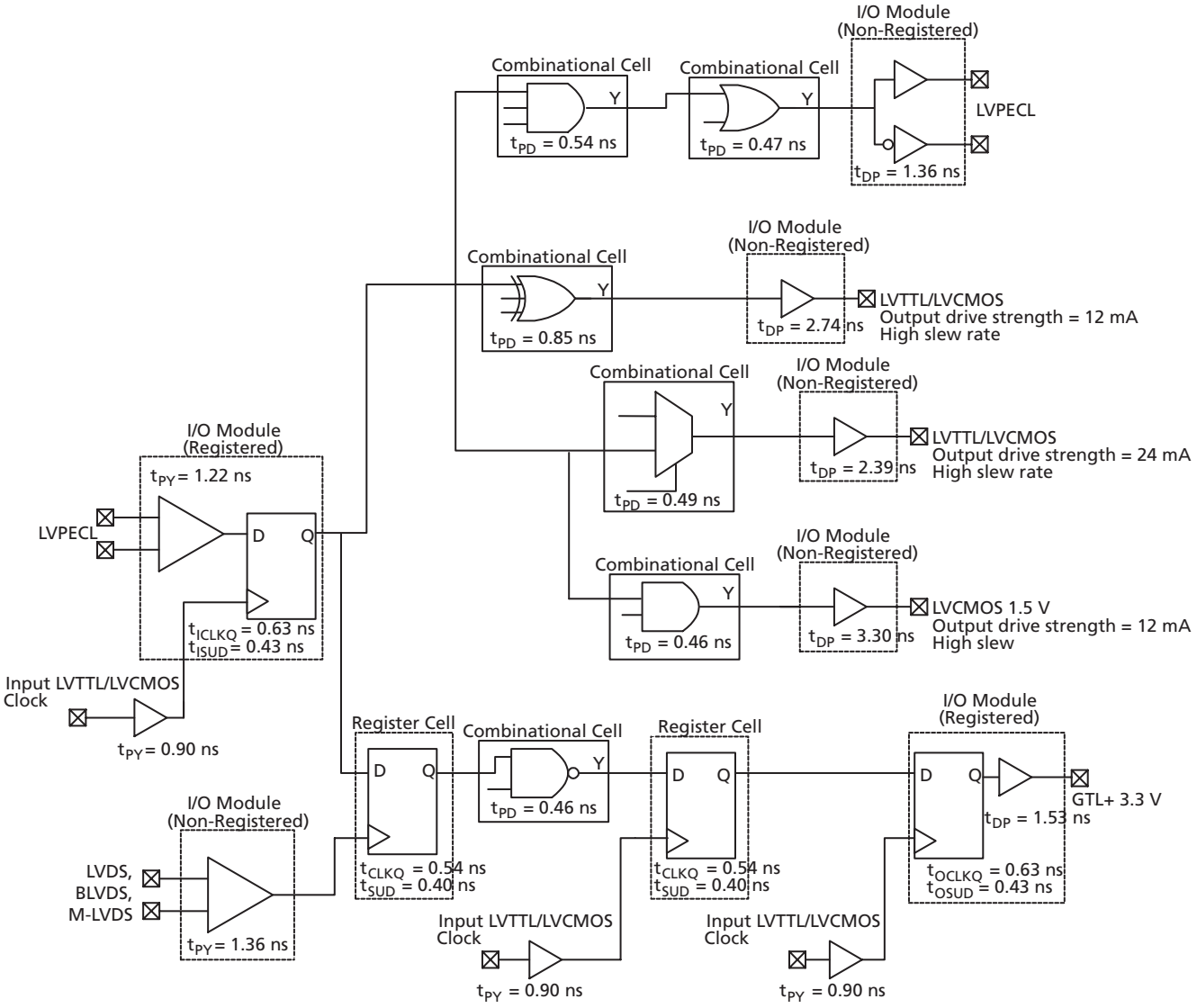

Figure 3-2 • **Timing Model**
Operating Conditions: –2 Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case V_{CC} = 1.425 V

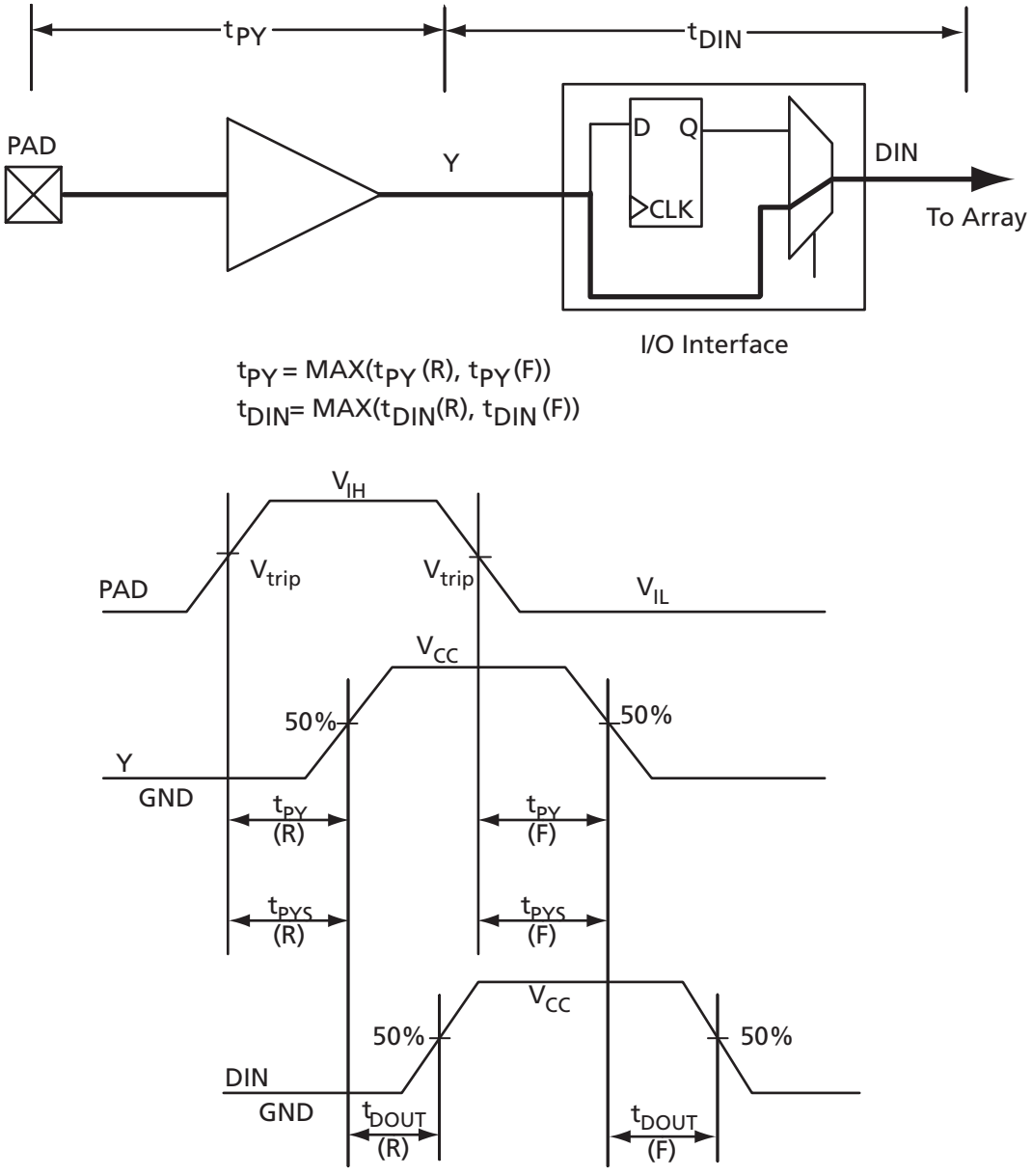

Figure 3-3 • **Input Buffer Timing Model and Delays (example)**

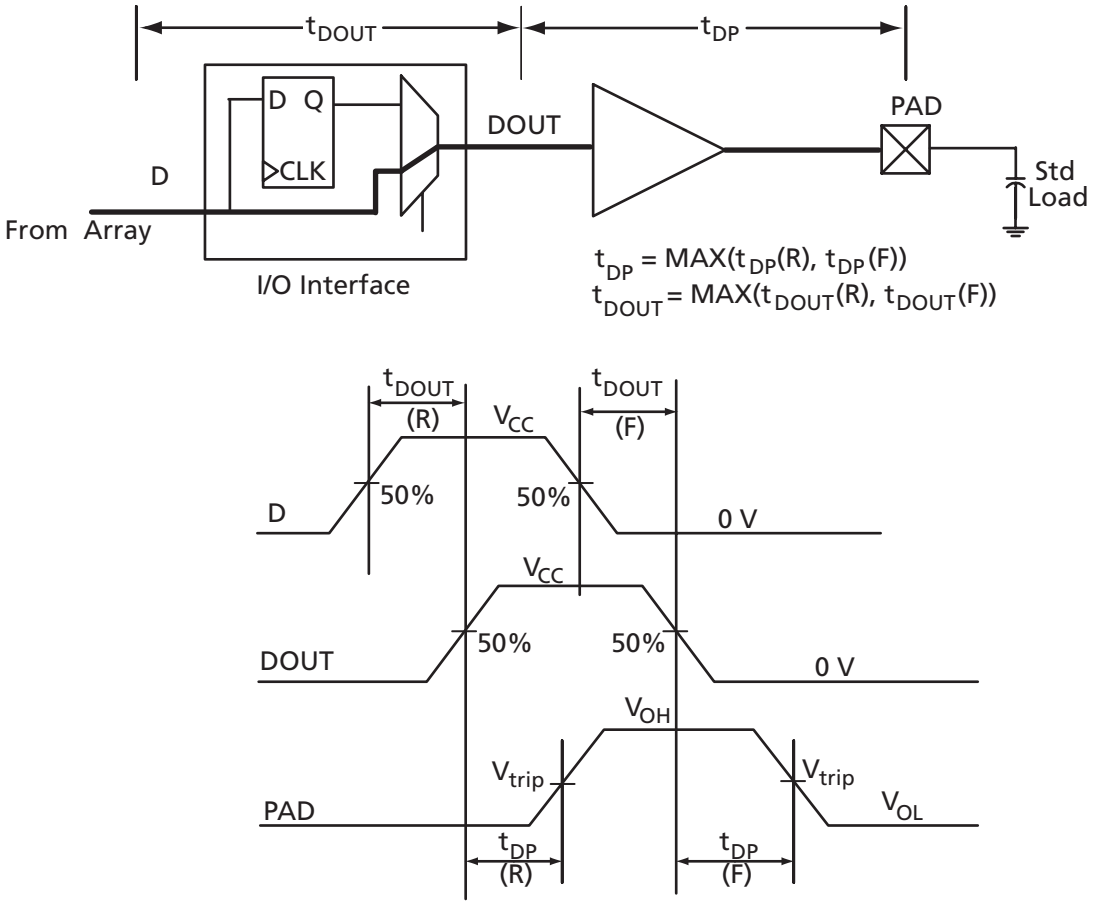

Figure 3-4 • **Output Buffer Model and Delays (example)**

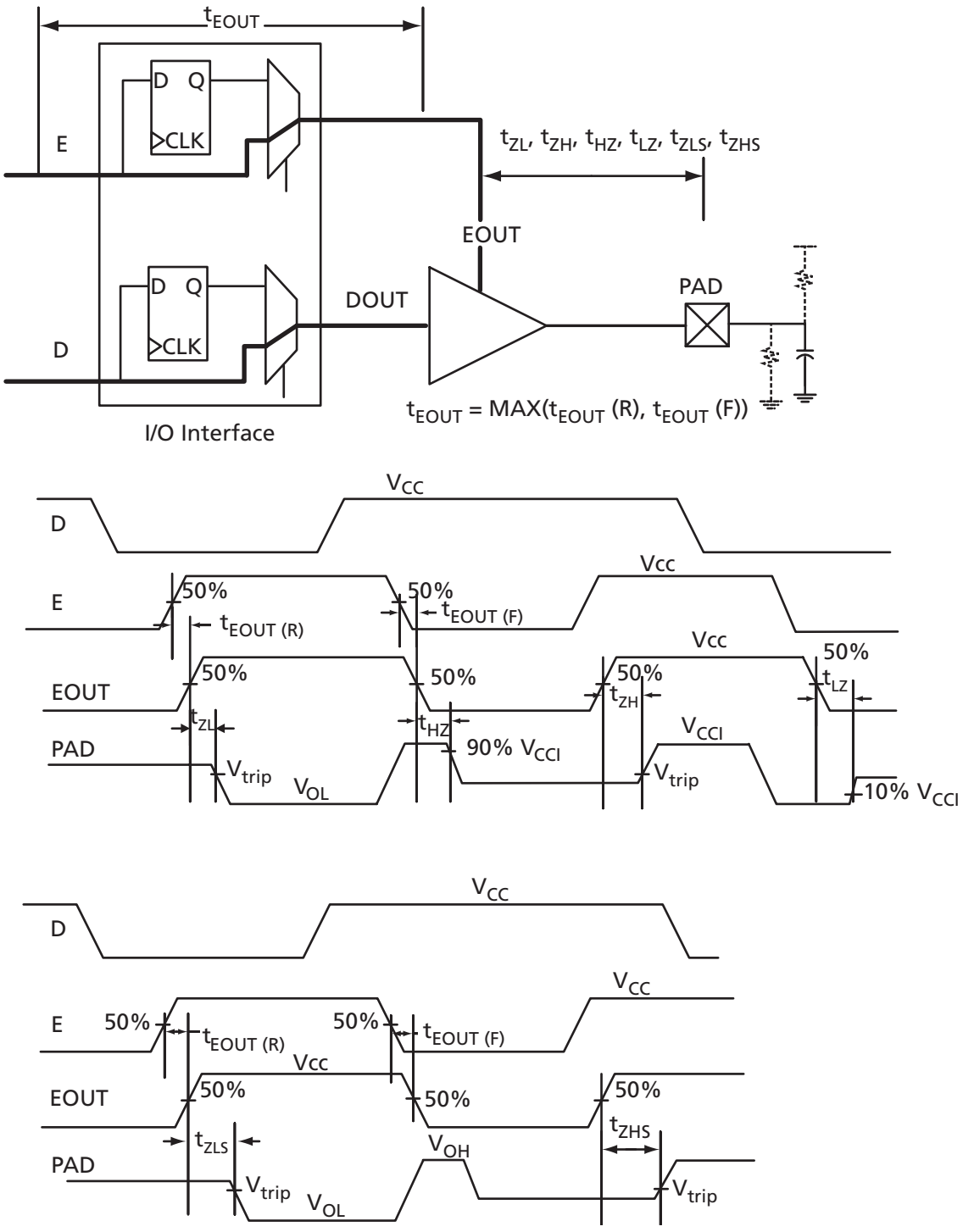

Figure 3-5 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 3-13 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions**

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.30 V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	25 mA[2]	High	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25
2.5 V GTL	25 mA[2]	High	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25
3.3 V GTL+	35 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	51	51
2.5 V GTL+	33 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	40	40
HSTL (I)	8 mA	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI} – 0.4	8	8
HSTL (II)	15 mA[2]	High	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI} – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.54	V_{CCI} – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.35	V_{CCI} – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*

Table 3-14 • **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

	Commercial[1]		Industrial[2]	
	I_{IL}	I_{IH}	I_{IL}	I_{IH}
DC I/O Standards	**µA**	**µA**	**µA**	**µA**
3.3 V LVTTL/3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range ($0°C < T_J < 70°C$)*
2. *Industrial range ($–40°C < T_J < 85°C$)*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 3-15 • **Summary of AC Measuring Points**

Standard	Input Reference Voltage (V_{REF_TYP})	Board Termination Voltage (V_{TT_REF})	Measuring Trip Point (V_{trip})
3.3 V LVTTL/3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * V_{CCI} (RR) 0.615 * V_{CCI} (FF))
3.3 V PCI-X	–	–	0.285 * V_{CCI} (RR) 0.615 * V_{CCI} (FF)
3.3 V GTL	0.8 V	1.2 V	V_{REF}
2.5 V GTL	0.8 V	1.2 V	V_{REF}
3.3 V GTL+	1.0 V	1.5 V	V_{REF}
2.5 V GTL+	1.0 V	1.5 V	V_{REF}
HSTL (I)	0.75 V	0.75 V	V_{REF}
HSTL (II)	0.75 V	0.75 V	V_{REF}
SSTL2 (I)	1.25 V	1.25 V	V_{REF}
SSTL2 (II)	1.25 V	1.25 V	V_{REF}
SSTL3 (I)	1.5 V	1.485 V	V_{REF}
SSTL3 (II)	1.5 V	1.485 V	V_{REF}
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 3-16 • **I/O AC Parameter Definitions**

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt Trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt Trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—high to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to high
t_{LZ}	Enable to Pad delay through the Output Buffer—low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to high
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to low

Table 3-17 • **Summary of I/O Timing Characteristics – Software Default Settings –2 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
2.5 V LVCMOS	12 mA	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
1.8 V LVCMOS	12 mA	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
1.5 V LVCMOS	12 mA	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
3.3 V PCI	Per PCI spec	High	10	25 [2]	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 [2]	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V GTL	25 mA	High	10	25	0.45	1.55	0.03	2.19	–	0.32	1.52	1.55	–	–	3.19	3.22	ns
2.5 V GTL	25 mA	High	10	25	0.45	1.59	0.03	1.83	–	0.32	1.61	1.59	–	–	3.28	3.26	ns
3.3 V GTL+	35 mA	High	10	25	0.45	1.53	0.03	1.19	–	0.32	1.56	1.53	–	–	3.23	3.20	ns
2.5 V GTL+	33 mA	High	10	25	0.45	1.65	0.03	1.13	–	0.32	1.68	1.57	–	–	3.35	3.24	ns
HSTL (I)	8 mA	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	–	–	4.09	4.02	ns
HSTL (II)	15 mA	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	–	–	3.97	3.70	ns
SSTL2 (I)	15 mA	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	–	–	3.29	3.05	ns
SSTL2 (II)	18 mA	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	–	–	3.32	2.99	ns
SSTL3 (I)	14 mA	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	–	–	3.42	3.04	ns
SSTL3 (II)	21 mA	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	–	–	3.24	2.92	ns
LVDS/BLVDS/ M-LVDS	24 mA	High	–	–	0.49	1.57	0.03	1.36	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.49	1.60	0.03	1.22	–	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-35 for connectivity. This resistor is not required during normal operation.*

Detailed I/O DC Characteristics

Table 3-18 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 3-19 • **I/O Output Buffer Maximum Resistances[1]**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	25 mA	11	–
2.5 V GTL	25 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 3-19 • **I/O Output Buffer Maximum Resistances[1] (Continued)**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
HSTL (II)	15 mA	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Table 3-20 • **I/O Weak Pull-Up/Pull-Down Resistances**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] ($\Omega$)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] ($\Omega$)	
V_{CCI}	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{WEAK\ PULL\text{-}DOWN\text{-}MIN}$
2. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{WEAK\ PULL\text{-}UP\text{-}MIN}$

Table 3-21 • **I/O Short Currents I_{OSH}/I_{OSL}**

	Drive Strength	I_{OSH} (mA)*	I_{OSL} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55

Note: **T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 3-22 • **Short Current Event Duration Before Failure**

Temperature	Time Before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

Table 3-23 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (Typ) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (Typ)
3.3 V LVTTL/LVCMOS / PCI / PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 3-24 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**[1]

Input Buffer	Input Rise/Fall Time (Min.)	Input Rise/Fall Time (Max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns [2]	20 years (110°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed schmitt hysteresis	20 years (110°C)
HSTL/SSTL/GTL	No requirement	10 ns [2]	10 years (100°C)
LVDS/BLVDS/M-LVDS/LVPECL	No requirement	10 ns [2]	10 years (100°C)

Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

Table 3-25 • **Minimum and Maximum DC Input and Output Levels**

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

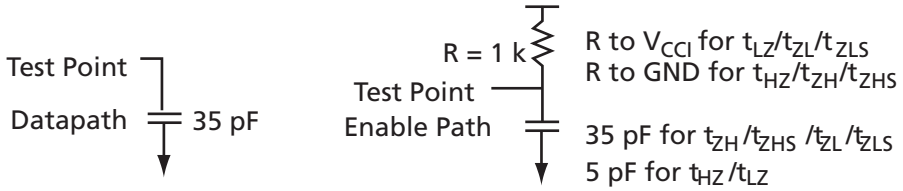

Figure 3-6 • **AC Loading**

Table 3-26 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-27 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 m A	–F	0.79	13.22	0.05	1.44	1.88	0.51	13.47	10.87	3.23	2.93	16.16	13.56	ns
	Std.	0.66	11.01	0.04	1.20	1.57	0.43	11.21	9.05	2.69	2.44	13.45	11.29	ns
	–1	0.56	9.36	0.04	1.02	1.33	0.36	9.54	7.70	2.29	2.08	11.44	9.60	ns
	–2	0.49	8.22	0.03	0.90	1.17	0.32	8.37	6.76	2.01	1.82	10.04	8.43	ns
8 m A	–F	0.79	9.45	0.05	1.44	1.88	0.51	9.62	7.74	3.65	3.68	12.31	10.42	ns
	Std.	0.66	7.86	0.04	1.20	1.57	0.43	8.01	6.44	3.04	3.06	10.24	8.68	ns
	–1	0.56	6.69	0.04	1.02	1.33	0.36	6.81	5.48	2.58	2.61	8.71	7.38	ns
	–2	0.49	5.87	0.03	0.90	1.17	0.32	5.98	4.81	2.27	2.29	7.65	6.48	ns
12 mA	–F	0.79	7.24	0.05	1.44	1.88	0.51	7.37	6.03	3.93	4.17	10.06	8.72	ns
	Std.	0.66	6.03	0.04	1.20	1.57	0.43	6.14	5.02	3.28	3.47	8.37	7.26	ns
	–1	0.56	5.13	0.04	1.02	1.33	0.36	5.22	4.27	2.79	2.95	7.12	6.17	ns
	–2	0.49	4.50	0.03	0.90	1.17	0.32	4.58	3.75	2.45	2.59	6.25	5.42	ns
16 mA	–F	0.79	6.75	0.05	1.44	1.88	0.51	6.87	5.68	3.99	4.30	9.56	8.36	ns
	Std.	0.66	5.62	0.04	1.20	1.57	0.43	5.72	4.72	3.32	3.58	7.96	6.96	ns
	–1	0.56	4.78	0.04	1.02	1.33	0.36	4.87	4.02	2.83	3.04	6.77	5.92	ns
	–2	0.49	4.20	0.03	0.90	1.17	0.32	4.27	3.53	2.48	2.67	5.94	5.20	ns
24 mA	–F	0.79	6.30	0.05	1.44	1.88	0.51	6.42	5.64	4.07	4.76	9.10	8.32	ns
	Std.	0.66	5.24	0.04	1.20	1.57	0.43	5.34	4.69	3.39	3.96	7.58	6.93	ns
	–1	0.56	4.46	0.04	1.02	1.33	0.36	4.54	3.99	2.88	3.37	6.44	5.89	ns
	–2	0.49	3.92	0.03	0.90	1.17	0.32	3.99	3.50	2.53	2.96	5.66	5.17	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-28 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	9.47	0.05	1.44	1.88	0.51	9.64	8.05	3.23	3.11	12.33	10.74	ns
	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	–1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	–2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
8 mA	–F	0.79	6.10	0.05	1.44	1.88	0.51	6.21	4.98	3.66	3.86	8.90	7.66	ns
	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	–1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	–2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12 mA	–F	0.79	4.41	0.05	1.44	1.88	0.51	4.49	3.45	3.93	4.34	7.17	6.13	ns
	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	–1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	–2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16 mA	–F	0.79	4.16	0.05	1.44	1.88	0.51	4.24	3.13	4.00	4.47	6.92	5.82	ns
	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	–1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	–2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24 mA	–F	0.79	3.85	0.05	1.44	1.88	0.51	3.92	2.59	4.07	4.96	6.61	5.28	ns
	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	–1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	–2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 2.5 V applications. It uses a 5-V-tolerant input buffer and push-pull output buffer.

Table 3-29 • **Minimum and Maximum DC Input and Output Levels**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

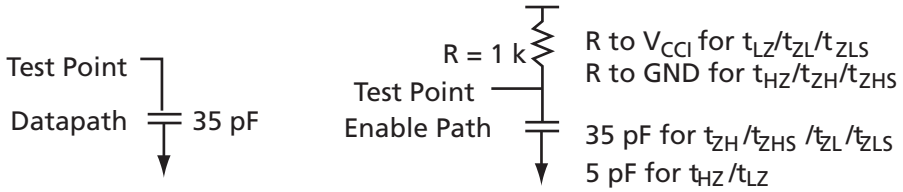

Figure 3-7 • **AC Loading**

Table 3-30 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-31 • **2.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	14.42	0.05	1.82	1.99	0.51	14.69	13.95	3.26	2.64	17.37	16.63	ns
	Std.	0.66	12.00	0.04	1.51	1.66	0.43	12.23	11.61	2.72	2.20	14.46	13.85	ns
	–1	0.56	10.21	0.04	1.29	1.41	0.36	10.40	9.88	2.31	1.87	12.30	11.78	ns
	–2	0.49	8.96	0.03	1.13	1.24	0.32	9.13	8.67	2.03	1.64	10.80	10.34	ns
8 mA	–F	0.79	10.49	0.05	1.82	1.99	0.51	10.68	9.62	3.73	3.52	13.37	12.31	ns
	Std.	0.66	8.73	0.04	1.51	1.66	0.43	8.89	8.01	3.10	2.93	11.13	10.25	ns
	–1	0.56	7.43	0.04	1.29	1.41	0.36	7.57	6.82	2.64	2.49	9.47	8.72	ns
	–2	0.49	6.52	0.03	1.13	1.24	0.32	6.64	5.98	2.32	2.19	8.31	7.65	ns
12 mA	–F	0.79	8.14	0.05	1.82	1.99	0.51	8.29	7.34	4.04	4.08	10.97	10.02	ns
	Std.	0.66	6.77	0.04	1.51	1.66	0.43	6.90	6.11	3.37	3.39	9.14	8.34	ns
	–1	0.56	5.76	0.04	1.29	1.41	0.36	5.87	5.20	2.86	2.89	7.77	7.10	ns
	–2	0.49	5.06	0.03	1.13	1.24	0.32	5.15	4.56	2.51	2.53	6.82	6.23	ns
16 mA	–F	0.79	7.58	0.05	1.82	1.99	0.51	7.72	6.88	4.11	4.23	10.40	9.57	ns
	Std.	0.66	6.31	0.04	1.51	1.66	0.43	6.42	5.73	3.42	3.52	8.66	7.96	ns
	–1	0.56	5.37	0.04	1.29	1.41	0.36	5.46	4.87	2.91	3.00	7.37	6.77	ns
	–2	0.49	4.71	0.03	1.13	1.24	0.32	4.80	4.28	2.56	2.63	6.47	5.95	ns
24 mA	–F	0.79	7.13	0.05	1.82	1.99	0.51	7.26	6.85	4.20	4.80	9.94	9.54	ns
	Std.	0.66	5.93	0.04	1.51	1.66	0.43	6.04	5.70	3.49	4.00	8.28	7.94	ns
	–1	0.56	5.05	0.04	1.29	1.41	0.36	5.14	4.85	2.97	3.40	7.04	6.75	ns
	–2	0.49	4.43	0.03	1.13	1.24	0.32	4.51	4.26	2.61	2.99	6.18	5.93	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-32 • **2.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	–F	0.79	10.59	0.05	1.82	1.99	0.51	9.77	10.59	3.26	2.75	12.45	13.28	ns
	Std.	0.66	8.82	0.04	1.51	1.66	0.43	8.13	8.82	2.72	2.29	10.37	11.05	ns
	–1	0.56	7.50	0.04	1.29	1.41	0.36	6.92	7.50	2.31	1.95	8.82	9.40	ns
	–2	0.49	6.58	0.03	1.13	1.24	0.32	6.07	6.58	2.03	1.71	7.74	8.25	ns
8 mA	–F	0.79	6.33	0.05	1.82	1.99	0.51	6.33	6.33	3.73	3.64	9.02	9.02	ns
	Std.	0.66	5.27	0.04	1.51	1.66	0.43	5.27	5.27	3.10	3.03	7.50	7.51	ns
	–1	0.56	4.48	0.04	1.29	1.41	0.36	4.48	4.48	2.64	2.58	6.38	6.38	ns
	–2	0.49	3.94	0.03	1.13	1.24	0.32	3.93	3.94	2.32	2.26	5.60	5.61	ns
12 mA	–F	0.79	4.50	0.05	1.82	1.99	0.51	4.58	4.19	4.04	4.20	7.27	6.88	ns
	Std.	0.66	3.74	0.04	1.51	1.66	0.43	3.81	3.49	3.37	3.49	6.05	5.73	ns
	–1	0.56	3.18	0.04	1.29	1.41	0.36	3.24	2.97	2.86	2.97	5.15	4.87	ns
	–2	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
16 mA	–F	0.79	4.24	0.05	1.82	1.99	0.51	4.32	3.75	4.11	4.35	7.00	6.43	ns
	Std.	0.66	3.53	0.04	1.51	1.66	0.43	3.59	3.12	3.42	3.62	5.83	5.35	ns
	–1	0.56	3.00	0.04	1.29	1.41	0.36	3.06	2.65	2.91	3.08	4.96	4.55	ns
	–2	0.49	2.63	0.03	1.13	1.24	0.32	2.68	2.33	2.56	2.71	4.35	4.00	ns
24 mA	–F	0.79	3.92	0.05	1.82	1.99	0.51	3.99	2.98	4.20	4.93	6.68	5.67	ns
	Std.	0.66	3.26	0.04	1.51	1.66	0.43	3.32	2.48	3.49	4.11	5.56	4.72	ns
	–1	0.56	2.77	0.04	1.29	1.41	0.36	2.83	2.11	2.97	3.49	4.73	4.01	ns
	–2	0.49	2.44	0.03	1.13	1.24	0.32	2.48	1.85	2.61	3.07	4.15	3.52	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.8 V applications. It uses 1.8 V input buffer and push-pull output buffer.

Table 3-33 • **Minimum and Maximum DC Input and Output Levels**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	16	16	74	91	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

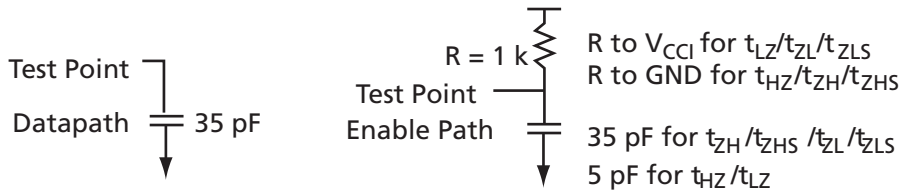

Figure 3-8 • **AC Loading**

Table 3-34 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-35 • **1.8 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.7 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	19.03	0.05	1.74	2.29	0.51	18.80	19.03	3.34	1.90	21.49	21.71	ns
	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	–1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	–2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4 mA	–F	0.79	13.68	0.05	1.74	2.29	0.51	13.94	12.92	3.91	3.33	16.62	15.61	ns
	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	–1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	–2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
6 mA	–F	0.79	10.78	0.05	1.74	2.29	0.51	10.98	9.73	4.29	4.03	13.66	12.41	ns
	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	–1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	–2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
8 mA	–F	0.79	10.03	0.05	1.74	2.29	0.51	10.22	9.11	4.37	4.23	12.90	11.80	ns
	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	–1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	–2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
12 mA	–F	0.79	9.54	0.05	1.74	2.29	0.51	9.72	9.08	4.50	4.93	12.40	11.77	ns
	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns
16 mA	–F	0.79	9.54	0.05	1.74	2.29	0.51	9.72	9.08	4.50	4.93	12.40	11.77	ns
	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-36 • **1.8 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.7 V

Drive Strength (mA)	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	14.54	0.05	1.74	2.29	0.51	11.52	14.54	3.34	1.97	14.21	17.23	ns
	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	–1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	–2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	–F	0.79	8.47	0.05	1.74	2.29	0.51	7.45	8.47	3.90	3.44	10.14	11.16	ns
	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	–1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	–2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
6 mA	–F	0.79	5.43	0.05	1.74	2.29	0.51	5.36	5.43	4.29	4.17	8.05	8.12	ns
	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	–1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	–2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
8 mA	–F	0.79	4.95	0.05	1.74	2.29	0.51	5.04	4.80	4.36	4.35	7.73	7.48	ns
	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	–1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	–2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
12 mA	–F	0.79	4.56	0.05	1.74	2.29	0.51	4.64	3.71	4.48	5.09	7.33	6.40	ns
	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
16 mA	–F	0.79	4.56	0.05	1.74	2.29	0.51	4.64	3.71	4.48	5.09	7.33	6.40	ns
	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.5 V applications. It uses 1.5 V input buffer and push-pull output buffer.

Table 3-37 • **Minimum and Maximum DC Input and Output Levels**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	16	13	10	10
4 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	33	25	10	10
6 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	6	6	39	32	10	10
8 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	8	8	55	66	10	10
12 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

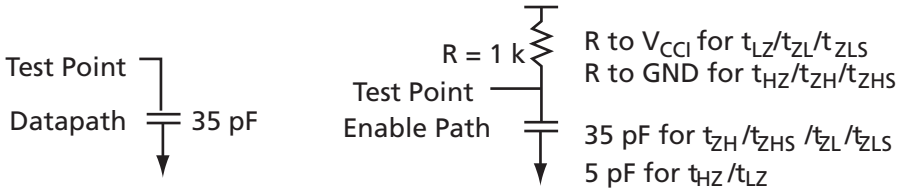

Figure 3-9 • **AC Loading**

Table 3-38 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-39 • **1.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.4 V

Drive strength (mA)	Speed grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	16.95	0.05	2.04	2.58	0.51	17.26	15.78	4.09	3.22	19.95	18.47	ns
	Std.	0.66	14.11	0.04	1.70	2.14	0.43	14.37	13.14	3.40	2.68	16.61	15.37	ns
	–1	0.56	12.00	0.04	1.44	1.82	0.36	12.22	11.17	2.90	2.28	14.13	13.08	ns
	–2	0.49	10.54	0.03	1.27	1.60	0.32	10.73	9.81	2.54	2.00	12.40	11.48	ns
4 mA	–F	0.79	13.49	0.05	2.04	2.58	0.51	13.74	11.85	4.53	4.03	16.43	14.54	ns
	Std.	0.66	11.23	0.04	1.70	2.14	0.43	11.44	9.87	3.77	3.36	13.68	12.10	ns
	–1	0.56	9.55	0.04	1.44	1.82	0.36	9.73	8.39	3.21	2.86	11.63	10.29	ns
	–2	0.49	8.39	0.03	1.27	1.60	0.32	8.54	7.37	2.81	2.51	10.21	9.04	ns
6 mA	–F	0.79	12.56	0.05	2.04	2.58	0.51	12.79	11.10	4.62	4.26	15.48	13.79	ns
	Std.	0.66	10.45	0.04	1.70	2.14	0.43	10.65	9.24	3.84	3.55	12.88	11.48	ns
	–1	0.56	8.89	0.04	1.44	1.82	0.36	9.06	7.86	3.27	3.02	10.96	9.76	ns
	–2	0.49	7.81	0.03	1.27	1.60	0.32	7.95	6.90	2.87	2.65	9.62	8.57	ns
8 mA	–F	0.79	12.04	0.05	2.04	2.58	0.51	12.26	11.09	4.77	5.07	14.94	13.77	ns
	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns
12 mA	–F	0.79	12.04	0.05	2.04	2.58	0.51	12.26	11.09	4.77	5.07	14.94	13.77	ns
	Std.	0.66	10.02	0.04	1.70	2.14	0.43	10.20	9.23	3.97	4.22	12.44	11.47	ns
	–1	0.56	8.52	0.04	1.44	1.82	0.36	8.68	7.85	3.38	3.59	10.58	9.75	ns
	–2	0.49	7.48	0.03	1.27	1.60	0.32	7.62	6.89	2.97	3.15	9.29	8.56	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-40 • **1.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.4 V

Drive strength (mA)	Speed grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	–F	0.79	10.25	0.05	2.04	2.58	0.51	8.72	10.25	4.08	3.35	11.41	12.94	ns
	Std.	0.66	8.53	0.04	1.70	2.14	0.43	7.26	8.53	3.39	2.79	9.50	10.77	ns
	–1	0.56	7.26	0.04	1.44	1.82	0.36	6.18	7.26	2.89	2.37	8.08	9.16	ns
	–2	0.49	6.37	0.03	1.27	1.60	0.32	5.42	6.37	2.53	2.08	7.09	8.04	ns
4 mA	–F	0.79	6.50	0.05	2.04	2.58	0.51	6.27	6.50	4.51	4.18	8.95	9.19	ns
	Std.	0.66	5.41	0.04	1.70	2.14	0.43	5.22	5.41	3.75	3.48	7.45	7.65	ns
	–1	0.56	4.60	0.04	1.44	1.82	0.36	4.44	4.60	3.19	2.96	6.34	6.50	ns
	–2	0.49	4.04	0.03	1.27	1.60	0.32	3.89	4.04	2.80	2.60	5.56	5.71	ns
6 mA	–F	0.79	5.77	0.05	2.04	2.58	0.51	5.88	5.70	4.60	4.41	8.56	8.39	ns
	Std.	0.66	4.80	0.04	1.70	2.14	0.43	4.89	4.75	3.83	3.67	7.13	6.98	ns
	–1	0.56	4.09	0.04	1.44	1.82	0.36	4.16	4.04	3.26	3.12	6.06	5.94	ns
	–2	0.49	3.59	0.03	1.27	1.60	0.32	3.65	3.54	2.86	2.74	5.32	5.21	ns
8 mA	–F	0.79	5.31	0.05	2.04	2.58	0.51	5.41	4.35	4.76	5.25	8.09	7.04	ns
	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	–1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	–2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
12 mA	–F	0.79	5.31	0.05	2.04	2.58	0.51	5.41	4.35	4.76	5.25	8.09	7.04	ns
	Std.	0.66	4.42	0.04	1.70	2.14	0.43	4.50	3.62	3.96	4.37	6.74	5.86	ns
	–1	0.56	3.76	0.04	1.44	1.82	0.36	3.83	3.08	3.37	3.72	5.73	4.98	ns
	–2	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 3-41 • **Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in Figure 3-10.

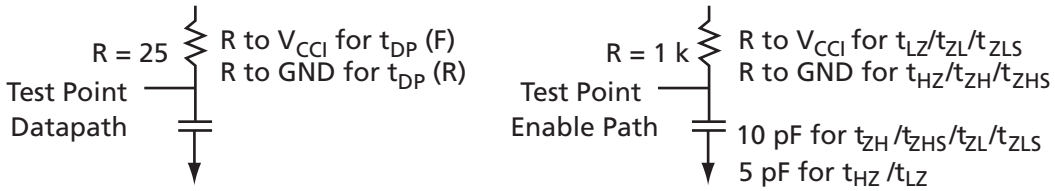

Figure 3-10 • **AC Loading**

AC loading are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 3-42.

Table 3-42 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	C_{LOAD} (pF)
0	3.3	0.285 * V_{CCI} for $t_{DP(R)}$ 0.615 * V_{CCI} for $t_{DP(F)}$	–	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-43 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	3.37	0.05	1.26	2.01	0.51	3.43	2.40	3.93	4.34	6.12	5.08	ns
Std.	0.66	2.81	0.04	1.05	1.67	0.43	2.86	2.00	3.28	3.61	5.09	4.23	ns
–1	0.56	2.39	0.04	0.89	1.42	0.36	2.43	1.70	2.79	3.07	4.33	3.60	ns
–2	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Voltage Referenced I/O Characteristics

3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 3-44 • **Minimum and Maximum DC Input and Output Levels**

3.3 V GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA[1]	Max, mA[1]	µA[2]	µA[2]
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

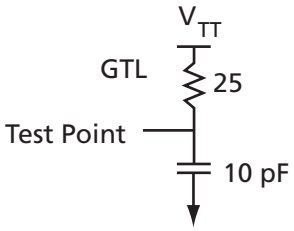

Figure 3-11 • **AC Loading**

Table 3-45 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-46 • **3.3 V GTL**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	2.49	0.05	3.52	0.51	2.45	2.49			5.13	5.18	ns
Std.	0.60	2.08	0.04	2.93	0.43	2.04	2.08			4.27	4.31	ns
–1	0.51	1.77	0.04	2.50	0.36	1.73	1.77			3.63	3.67	ns
–2	0.45	1.55	0.03	2.19	0.32	1.52	1.55			3.19	3.22	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 3-47 • **Minimum and Maximum DC Input and Output Levels**

2.5 GTL	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
25 mA[3]	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	–	25	25	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

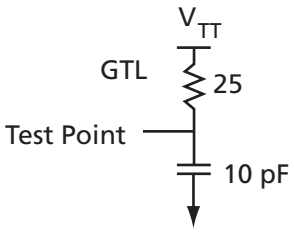

Figure 3-12 • **AC Loading**

Table 3-48 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.05	V_{REF} + 0.05	0.8	0.8	1.2	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-49 • **2.5 V GTL**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V V_{REF} = 0.8 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	2.56	0.05	2.95	0.51	2.60	2.56			5.28	5.24	ns
Std.	0.60	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
–1	0.51	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
–2	0.45	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open drain output buffer. The V_{CCI} pin should be connected to 3.3 V.

Table 3-50 • **Minimum and Maximum DC Input and Output Levels**

3.3 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
35 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	35	35	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

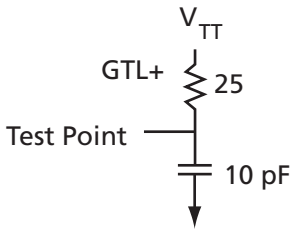

Figure 3-13 • **AC Loading**

Table 3-51 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-52 • **3.3 V GTL+**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V, V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	2.47	0.05	1.91	0.51	2.51	2.47			5.20	5.15	ns
Std.	0.60	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
–1	0.51	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
–2	0.45	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open drain output buffer. The V_{CCI} pin should be connected to 2.5 V.

Table 3-53 • **Minimum and Maximum DC Input and Output Levels**

2.5 V GTL+	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
33 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	–	33	33	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

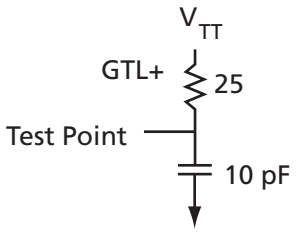

Figure 3-14 • **AC Loading**

Table 3-54 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	1.0	1.0	1.5	10

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-55 • **2.5 V GTL+**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V, V_{REF} = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.72	2.65	0.05	1.82	0.51	2.70	2.52			5.38	5.21	ns
Std.	0.60	2.21	0.04	1.51	0.43	2.25	2.10			4.48	4.34	ns
–1	0.51	1.88	0.04	1.29	0.36	1.91	1.79			3.81	3.69	ns
–2	0.45	1.65	0.03	1.13	0.32	1.68	1.57			3.35	3.24	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-56 • **Minimum and Maximum DC Input and Output Levels**

HSTL Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
8 mA	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI}-0.4	8	8	39	32	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

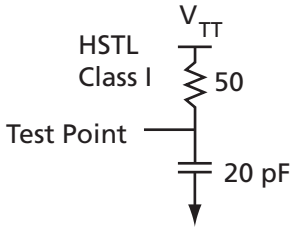

Figure 3-15 • **AC Loading**

Table 3-57 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-58 • **HSTL Class I**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.4 V, V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	3.82	0.05	2.55	0.51	3.89	3.78			6.58	6.46	ns
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
–1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
–2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-59 • **Minimum and Maximum DC Input and Output Levels**

HSTL Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
15 mA[3]	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCI}-0.4	15	15	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Output drive strength is below JEDEC specification.*

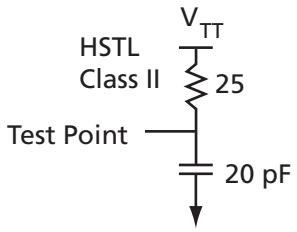

Figure 3-16 • **AC Loading**

Table 3-60 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.1	V_{REF} + 0.1	0.75	0.75	0.75	20

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-61 • **HSTL Class II**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 1.4 V, V_{REF} = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	3.63	0.05	2.55	0.51	3.70	3.26			6.39	5.95	ns
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
–1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
–2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-62 • **Minimum and Maximum DC Input and Output Levels**

SSTL2 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
15 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.54	V_{CCI} - 0.62	15	15	87	83	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

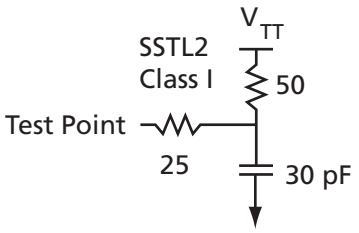

Figure 3-17 • **AC Loading**

Table 3-63 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.25	1.25	1.25	30

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-64 • **SSTL 2 Class I**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V, V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	2.56	0.05	1.60	0.51	2.60	2.22			5.29	4.90	ns
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-65 • **Minimum and Maximum DC Input and Output Levels**

SSTL2 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
18 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.35	V_{CCI} – 0.43	18	18	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

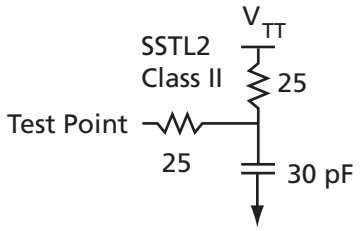

Figure 3-18 • **AC Loading**

Table 3-66 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.25	1.25	1.25	30

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-67 • **SSTL 2 Class II**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V, V_{REF} = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	2.60	0.05	1.60	0.51	2.65	2.13			5.34	4.81	ns
Std.	0.66	2.17	0.04	1.33	0.43	2.21	1.77			4.44	4.01	ns
–1	0.56	1.84	0.04	1.14	0.36	1.88	1.51			3.78	3.41	ns
–2	0.49	1.62	0.03	1.00	0.32	1.65	1.32			3.32	2.99	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

SSTL3 Class I

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-68 • **Minimum and Maximum DC Input and Output Levels**

SSTL3 Class I	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
14 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCI} – 1.1	14	14	54	51	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

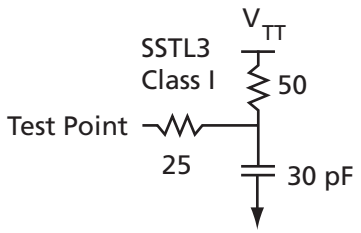

Figure 3-19 • **AC Loading**

Table 3-69 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-70 • **SSTL3 Class I**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V, V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	2.77	0.05	1.50	0.51	2.82	2.21			5.51	4.89	ns
Std.	0.66	2.31	0.04	1.25	0.43	2.35	1.84			4.59	4.07	ns
–1	0.56	1.96	0.04	1.06	0.36	2.00	1.56			3.90	3.46	ns
–2	0.49	1.72	0.03	0.93	0.32	1.75	1.37			3.42	3.04	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 3-71 • **Minimum and Maximum DC Input and Output Levels**

SSTL3 Class II	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
21 mA	–0.3	V_{REF} – 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCI} – 0.9	21	21	109	103	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

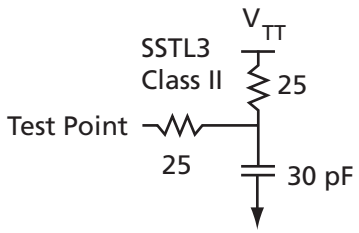

Figure 3-20 • **AC Loading**

Table 3-72 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)	V_{TT} (Typ) (V)	C_{LOAD} (pF)
V_{REF} – 0.2	V_{REF} + 0.2	1.5	1.5	1.485	30

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-73 • **SSTL3- Class II**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V, V_{REF} = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
–F	0.79	2.48	0.05	1.50	0.51	2.53	2.01			5.21	4.69	ns
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
–1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
–2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by the Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit is carried through two signal lines; so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 3-21. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation, because the output standard specifications are different.

Along with the LVDS I/O, ProASIC3E also will support BusLVDS structure and Multi-Drop LVDS (M-LVDS) configuration (up to 40 nodes).

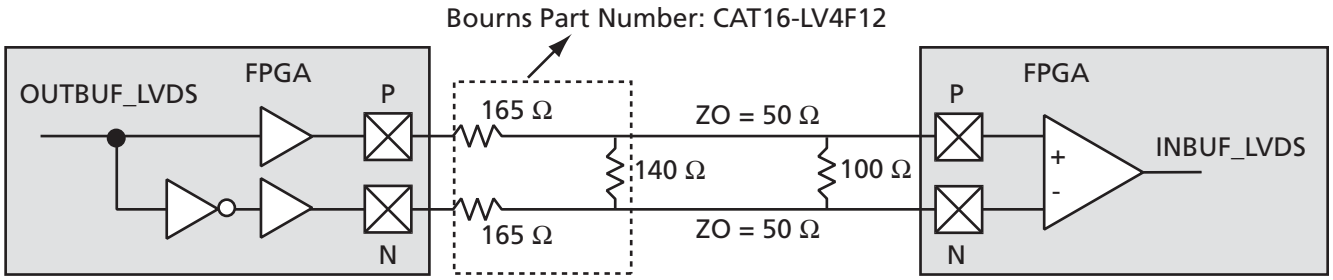

Figure 3-21 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 3-74 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage	2.375	2.5	2.625	V
V_{OL}	Output Low Voltage	0.9	1.075	1.25	V
V_{OH}	Output High Voltage	1.25	1.425	1.6	V
V_I	Input Voltage	0	–	2.925	V
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage	100	350	–	mV

Notes:

1. *+/- 5%*
2. *Differential input voltage = +/-350mV*

Table 3-75 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)
1.075	1.325	Cross point	–

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-76 • **LVDS**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
–F	0.79	2.25	0.05	2.18	ns
Std.	0.66	1.87	0.04	1.82	ns
–1	0.56	1.59	0.04	1.55	ns
–2	0.49	1.40	0.03	1.36	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

BLVDS/M-LVDS

Bus LVDS (BLVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers and transceivers. Actel LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The driver requires series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve upto 200 MHz with a maximum of 20 loads. A sample application is given in Figure 3-22. The input and output buffer delays are available in the LVDS section in Table 3-76.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and a Z_{stub} = 50 Ω (~1.5").

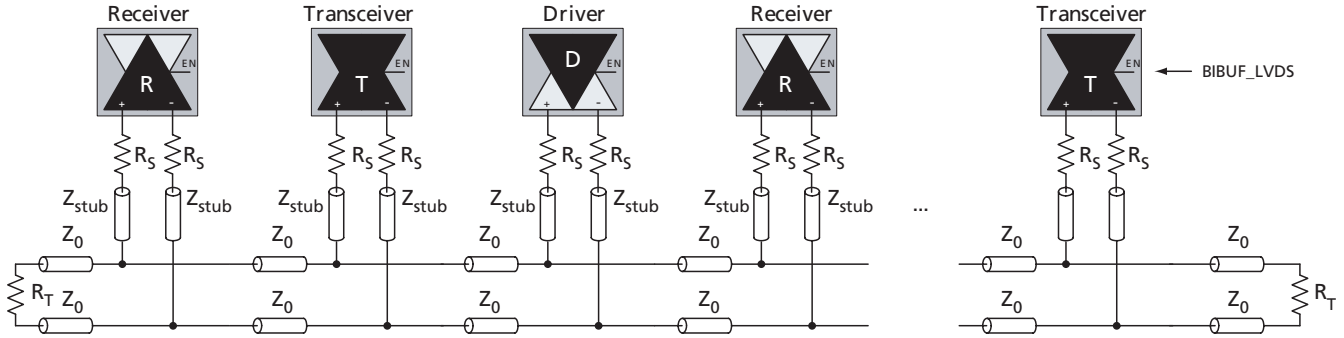

Figure 3-22 • **BLVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 3-23. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation, because the output standard specifications are different.

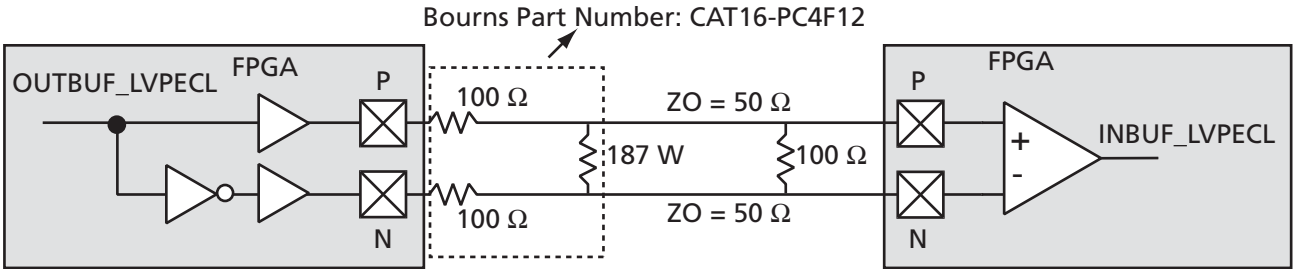

Figure 3-23 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 3-77 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input Low, Input High voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 3-78 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (Typ) (V)
1.64	1.94	Cross point	–

Note: **Measuring point = V_{trip}. See Table 3-15 on page 3-17 for a complete table of trip points.*

Timing Characteristics

Table 3-79 • **LVPECL**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
–F	0.79	2.19	0.05	1.96	ns
Std.	0.66	1.83	0.04	1.63	ns
–1	0.56	1.55	0.04	1.39	ns
–2	0.49	1.36	0.03	1.22	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

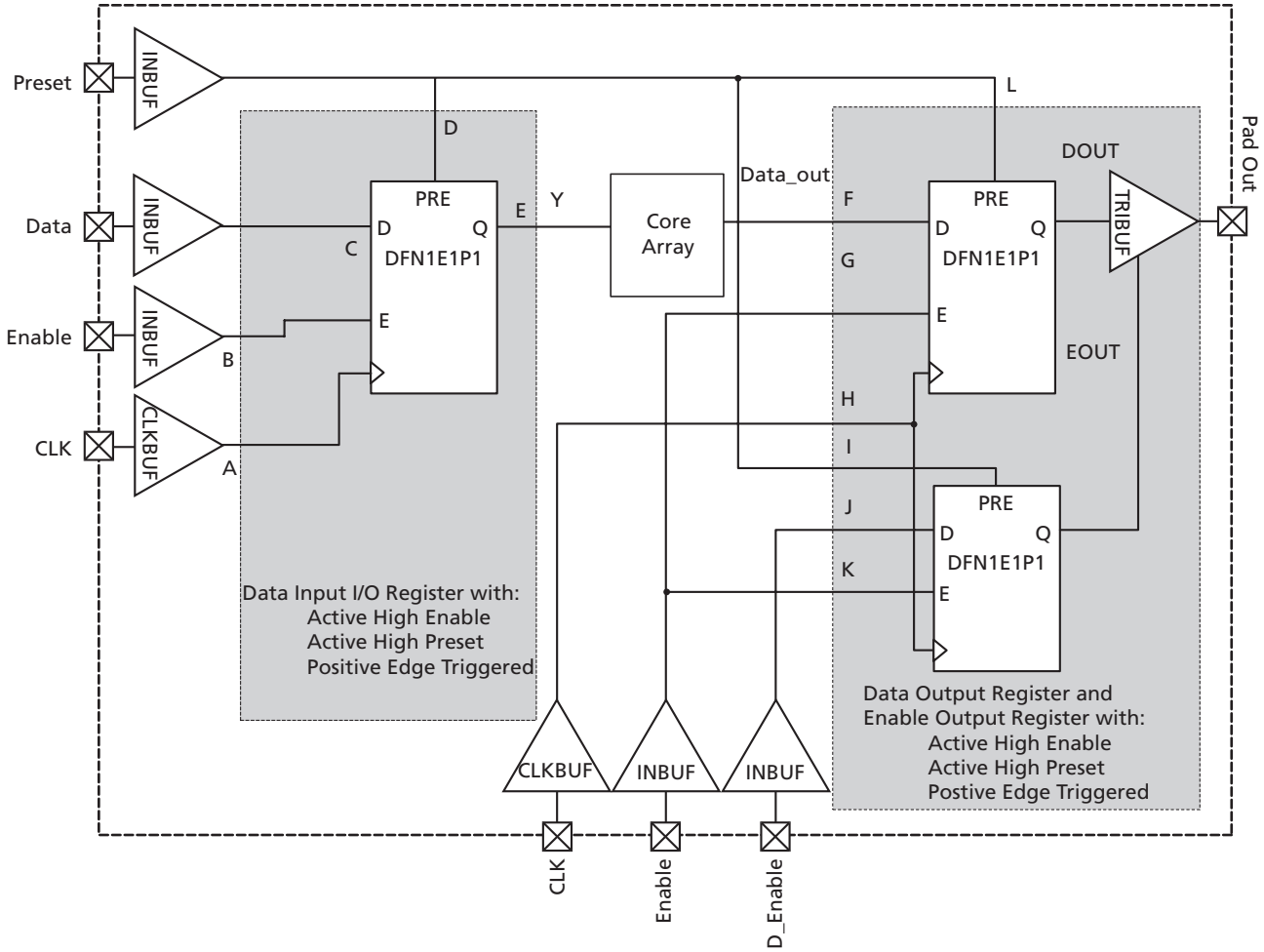

Figure 3-24 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 3-80 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup time for the Output Data Register	F, H
t_{OHD}	Data Hold time for the Output Data Register	F, H
t_{OSUE}	Enable Setup time for the Output Data Register	G, H
t_{OHE}	Enable Hold time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset removal time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup time for the Output Enable Register	J, H
t_{OEHD}	Data Hold time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup time for the Input Data Register	C, A
t_{IHD}	Data Hold time for the Input Data Register	C, A
t_{ISUE}	Enable Setup time for the Input Data Register	B, A
t_{IHE}	Enable Hold time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery time for the Input Data Register	D, A

Note: **See Figure 3-24 on page 3-49 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

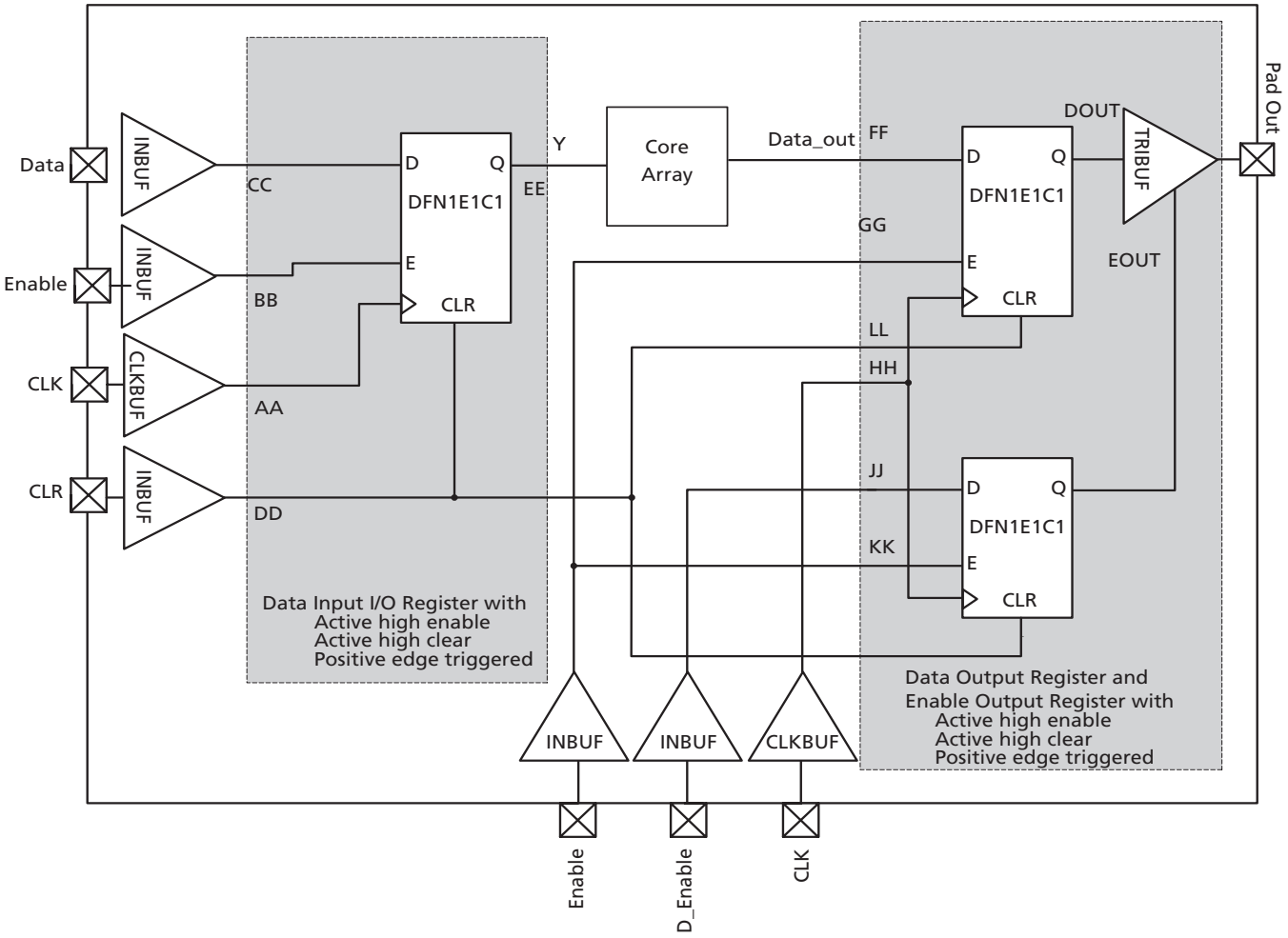

Figure 3-25 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 3-81 • **Parameter Definition and Measuring Nodes**

Parameter name	Parameter Definition	Measuring Nodes (From, To)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup time for the Output Data Register	FF, HH
t_{OHD}	Data Hold time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup time for the Input Data Register	CC, AA
t_{IHD}	Data Hold time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery time for the Input Data Register	DD, AA

Note: **See Figure 3-25 on page 3-51 for more information.*

Input Register

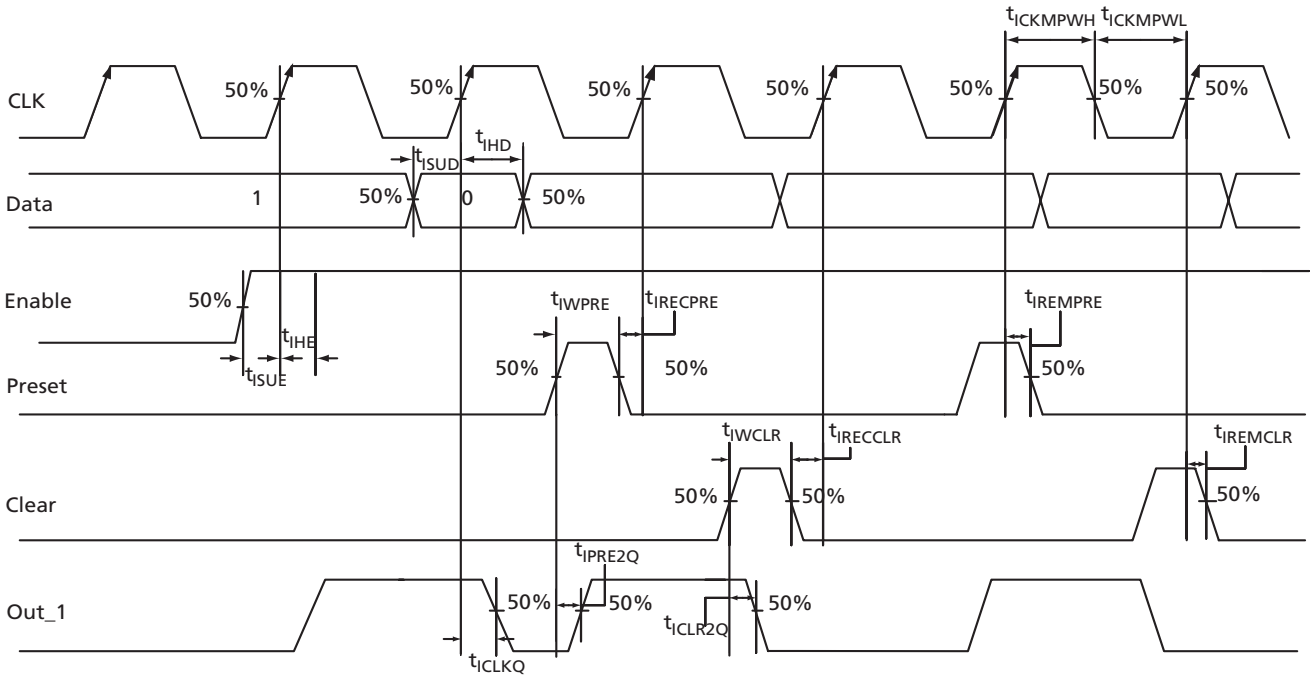

Figure 3-26 • **Input Register Timing Diagram**

Timing Characteristics

Table 3-82 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.63	0.71	0.84	1.01	ns
t_{ISUD}	Data Setup time for the Input Data Register	0.43	0.49	0.57	0.69	ns
t_{IHD}	Data Hold time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup time for the Input Data Register	0.43	0.49	0.57	0.69	ns
t_{IHE}	Enable Hold time for the Input Data Register	0.00	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.63	0.71	0.84	1.01	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.51	0.60	0.72	ns
$t_{IREMCLR}$	Asynchronous Clear Removal time for the Input Data Register	0.00	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery time for the Input Data Register	0.22	0.25	0.30	0.36	ns
$t_{IREMPRE}$	Asynchronous Preset Removal time for the Input Data Register	0.00	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery time for the Input Data Register	0.22	0.25	0.30	0.36	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.28	0.33	0.40	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.28	0.33	0.40	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	0.58	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.41	0.46	0.54	0.65	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Output Register

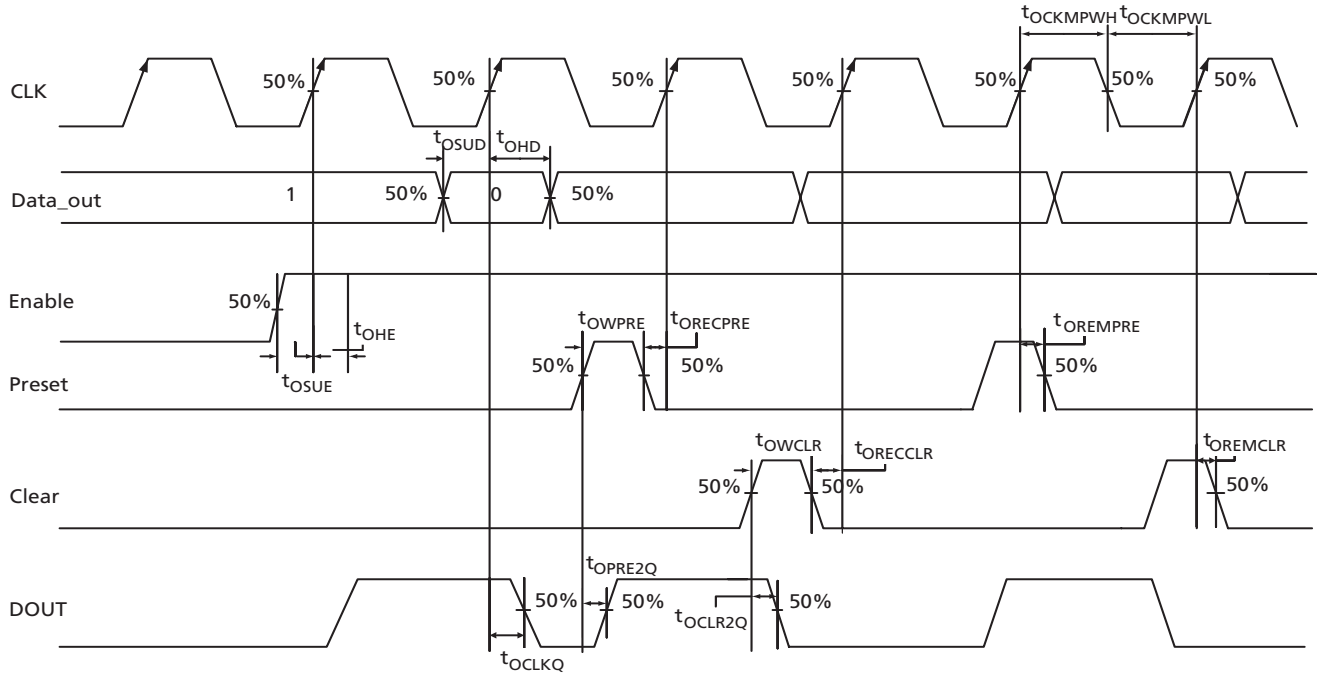

Figure 3-27 • **Output Register Timing Diagram**

Timing Characteristics

Table 3-83 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.63	0.71	0.84	1.01	ns
t_{OSUD}	Data Setup time for the Output Data Register	0.43	0.49	0.57	0.69	ns
t_{OHD}	Data Hold time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup time for the Output Data Register	0.43	0.49	0.57	0.69	ns
t_{OHE}	Enable Hold time for the Output Data Register	0.00	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.63	0.71	0.84	1.01	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.45	0.51	0.60	0.72	ns
$t_{OREMCLR}$	Asynchronous Clear Removal time for the Output Data Register	0.00	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery time for the Output Data Register	0.22	0.25	0.30	0.36	ns
$t_{OREMPRE}$	Asynchronous Preset Removal time for the Output Data Register	0.00	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery time for the Output Data Register	0.22	0.25	0.30	0.36	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.28	0.33	0.40	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.28	0.33	0.40	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	0.58	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.41	0.46	0.54	0.65	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Output Enable Register

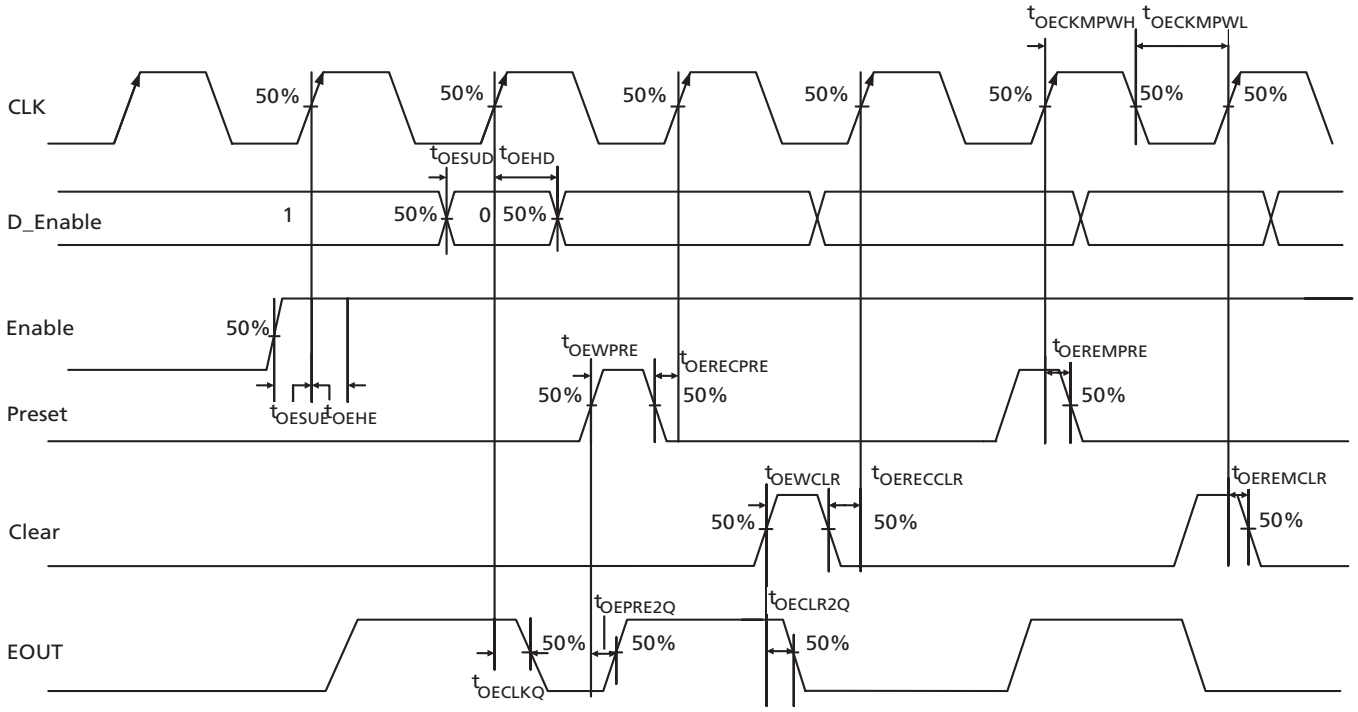

Figure 3-28 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 3-84 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.63	0.71	0.84	1.01	ns
t_{OESUD}	Data Setup time for the Output Enable Register	0.43	0.49	0.57	0.69	ns
t_{OEHD}	Data Hold time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
t_{OESUE}	Enable Setup time for the Output Enable Register	0.43	0.49	0.57	0.69	ns
t_{OEHE}	Enable Hold time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.63	0.71	0.84	1.01	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.45	0.51	0.60	0.72	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery time for the Output Enable Register	0.22	0.25	0.30	0.36	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal time for the Output Enable Register	0.00	0.00	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery time for the Output Enable Register	0.22	0.25	0.30	0.36	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.28	0.33	0.40	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.28	0.33	0.40	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	0.58	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.41	0.46	0.54	0.65	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

DDR Module Specifications

Input DDR Module

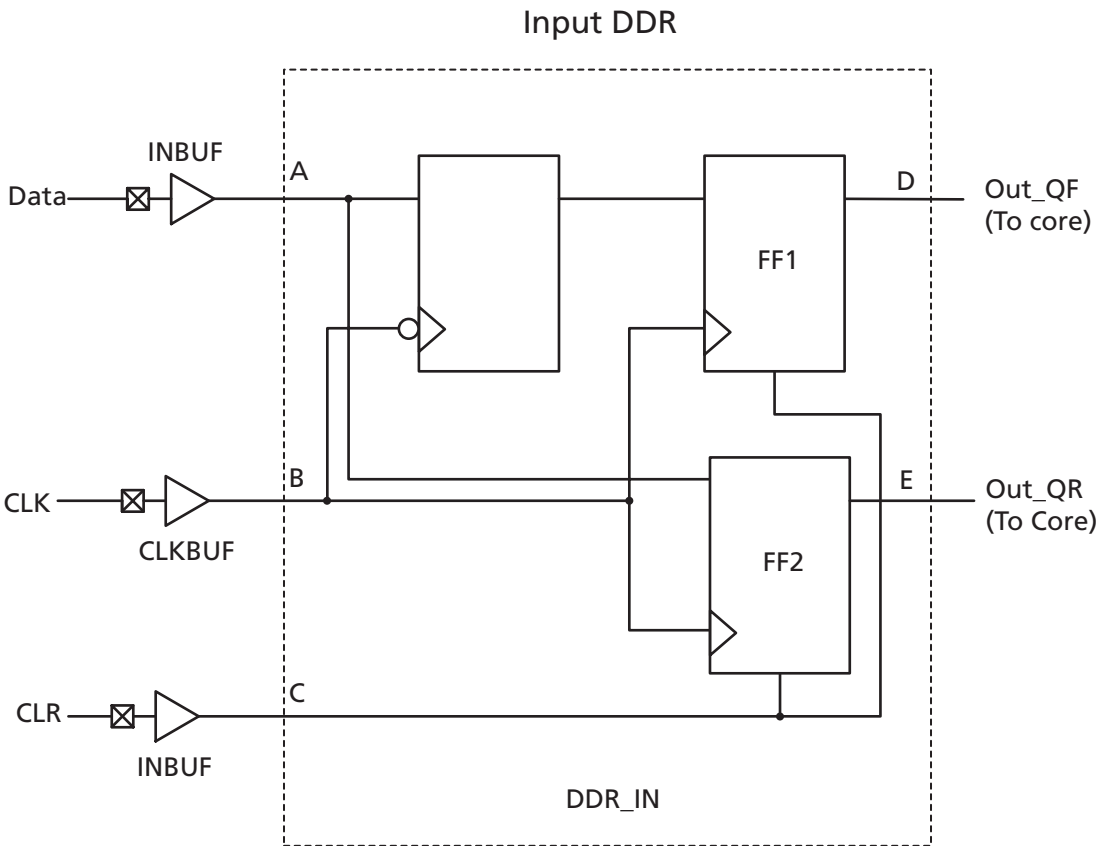

Figure 3-29 • **Input DDR Timing Model**

Table 3-85 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup time of DDR input	A, B
t_{DDRIHD}	Data Hold time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

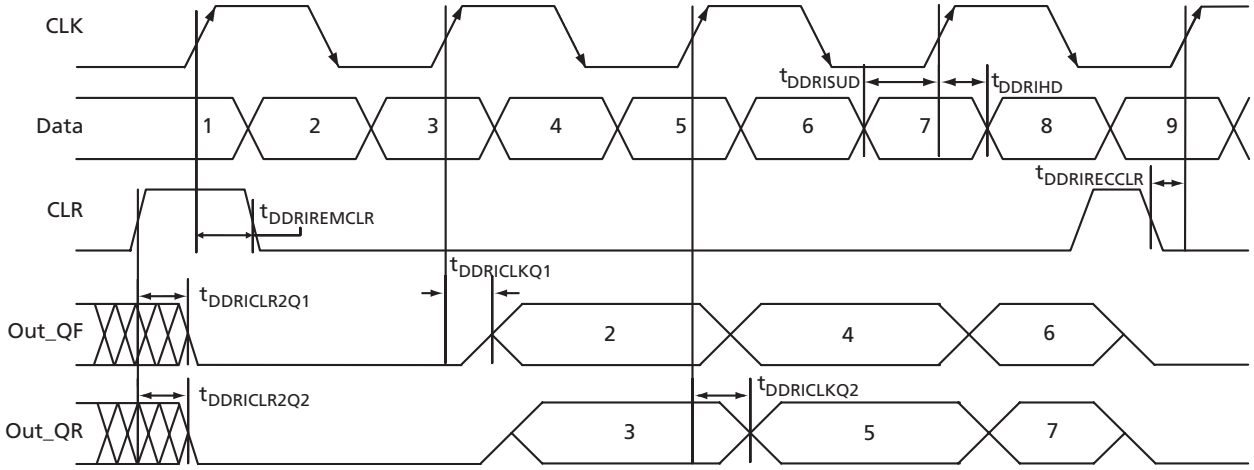

Figure 3-30 • **Input DDR Timing Diagram**

Timing Characteristics

Table 3-86 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.63	0.71	0.84	1.01	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.63	0.71	0.84	1.01	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.53	0.61	0.71	0.86	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear to Out Out_QR for Input DDR	0.57	0.65	0.76	0.91	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.57	0.65	0.76	0.91	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.22	0.25	0.30	0.36	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR					ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR					ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR					ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR					MHz

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Output DDR

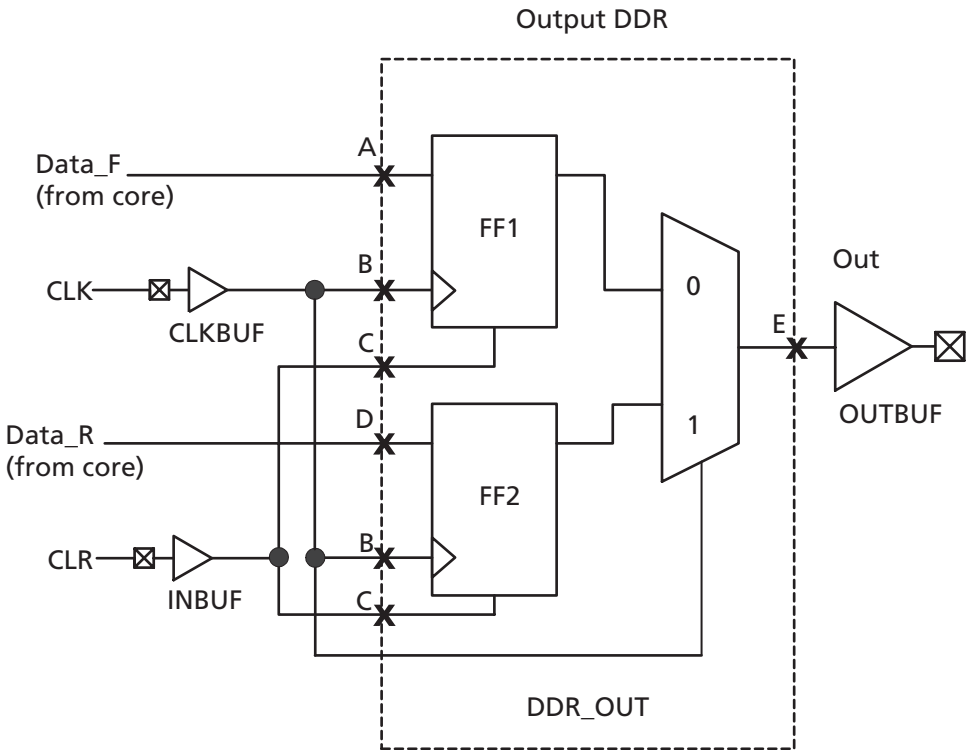

Figure 3-31 • **Output DDR Timing Model**

Table 3-87 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

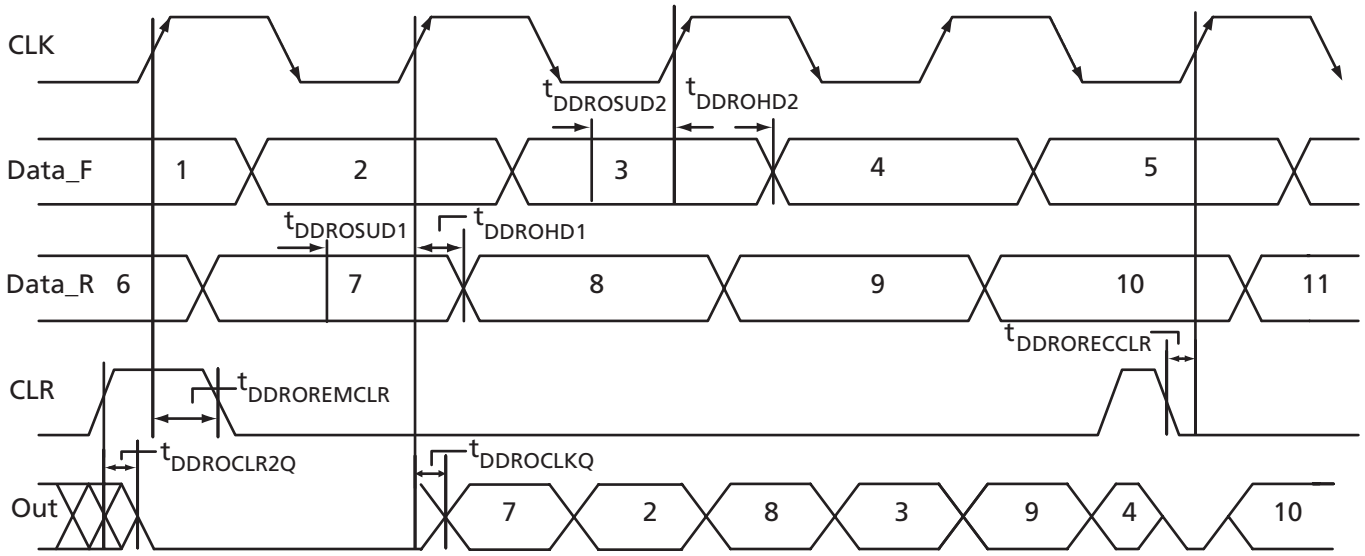

Figure 3-32 • **Output DDR Timing Diagram**

Timing Characteristics

Table 3-88 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.63	0.71	0.84	1.01	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.43	0.49	0.57	0.69	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.43	0.49	0.57	0.69	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.57	0.65	0.76	0.91	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal time for Output DDR	0.00	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery time for Output DDR	0.22	0.25	0.30	0.36	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR					ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR					ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR					ns
F_{DDOMAX}	Maximum Frequency for the Output DDR					MHz

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3E library offers all combinations of LUT-3 combinatorial functions. In this section timing characteristics are presented for a sample of the library. For more details, refer to the *ProASIC3/E Macro Library Guide*.

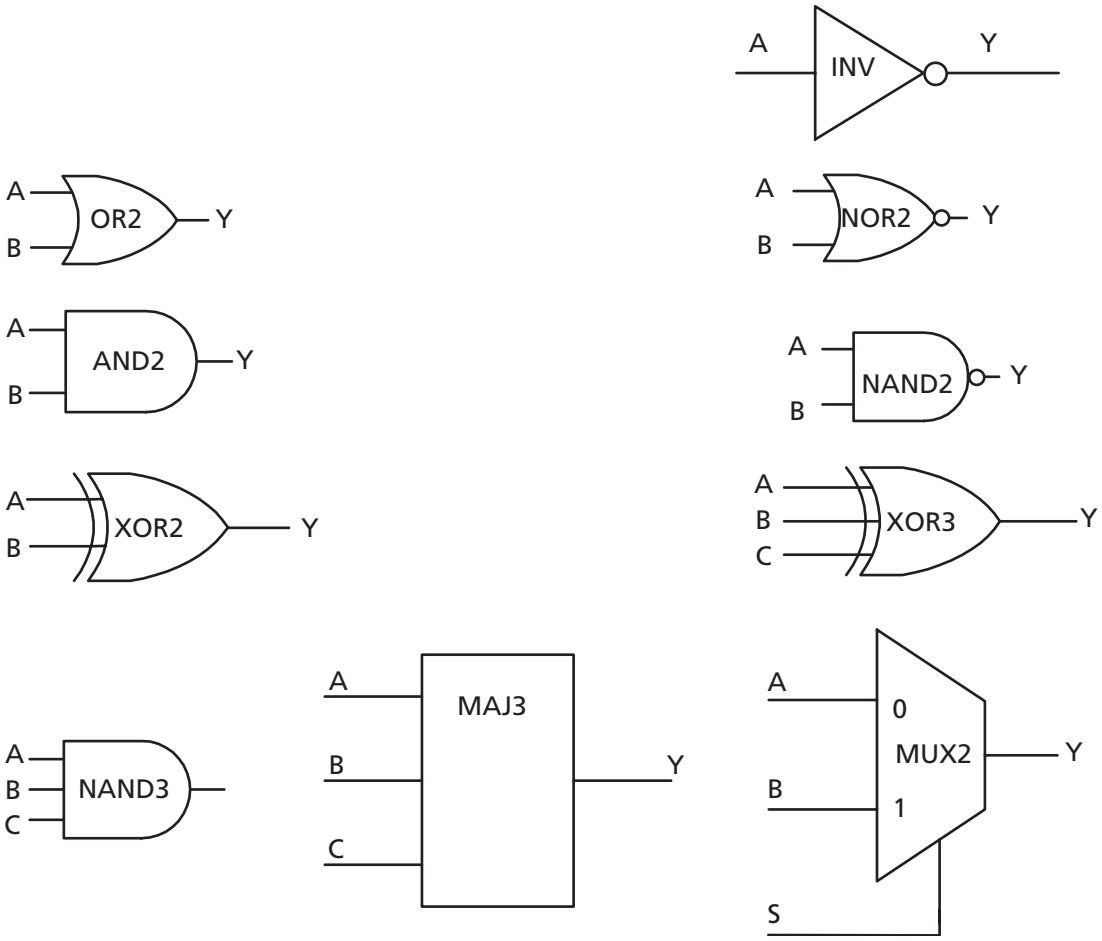

Figure 3-33 • **Sample of Combinatorial Cells**

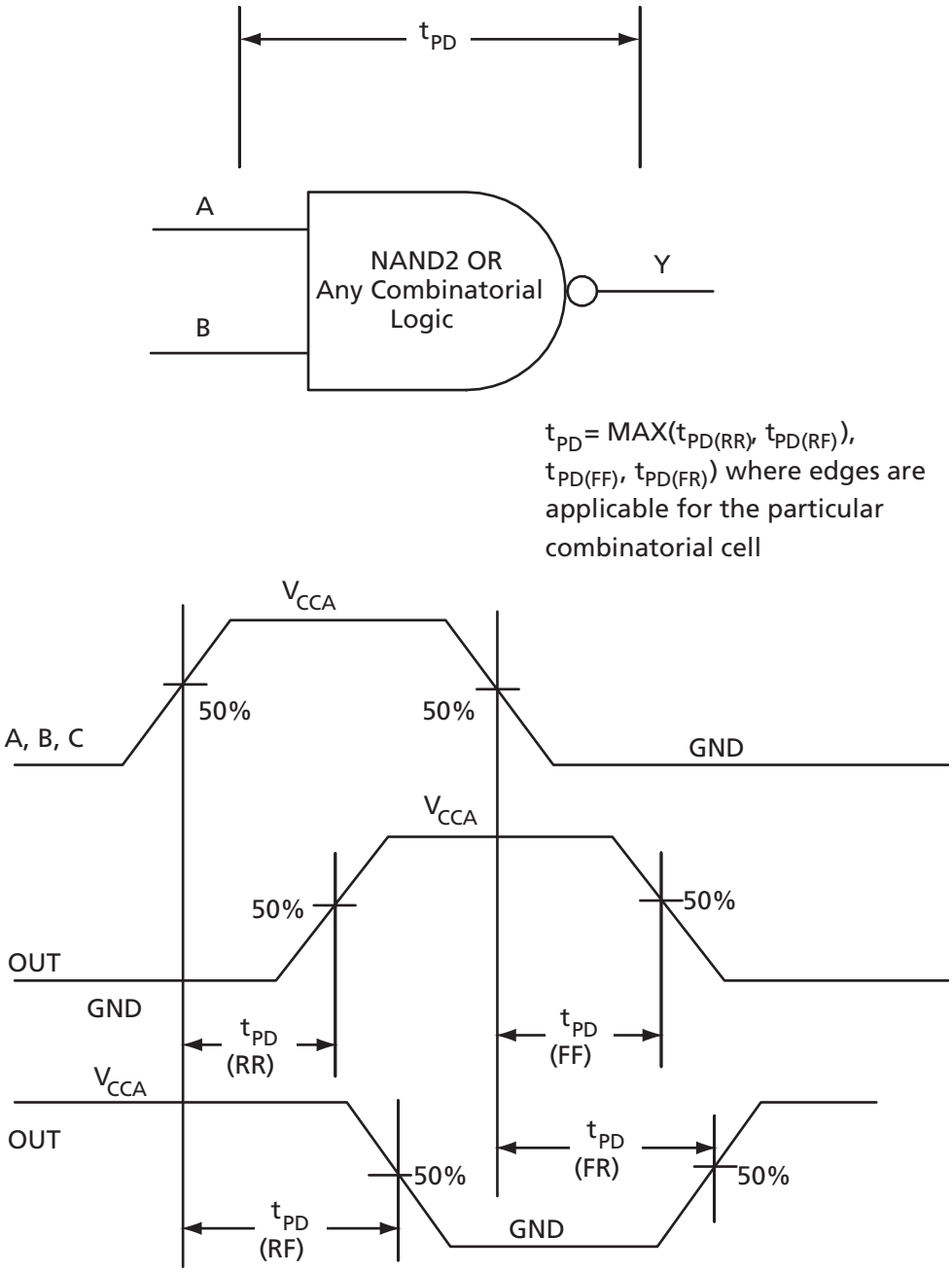

Figure 3-34 • **Timing Model and Waveforms**

Timing Characteristics

Table 3-89 • **Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	–F	Units
INV	Y = !A	t_{PD}	0.40	0.45	0.53	0.64	ns
AND2	Y = A · B	t_{PD}	0.46	0.52	0.62	0.74	ns
NAND2	Y = !(A · B)	t_{PD}	0.46	0.52	0.62	0.74	ns
OR2	Y = A + B	t_{PD}	0.47	0.54	0.63	0.76	ns
NOR2	Y = !(A + B)	t_{PD}	0.47	0.54	0.63	0.76	ns
XOR2	Y = A ⊕ B	t_{PD}	0.72	0.82	0.96	1.15	ns
MAJ3	Y = MAJ (A , B, C)	t_{PD}	0.67	0.76	0.90	1.08	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.85	0.97	1.14	1.37	ns
MUX2	Y = A !S + B S	t_{PD}	0.49	0.56	0.65	0.79	ns
AND3	Y = A · B · C	t_{PD}	0.54	0.62	0.73	0.87	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

VersaTile Specifications as a Sequential Module

The ProASIC3E library offers a wide variety of sequential cells including flip-flops and latches. Each have a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *ProASIC3/E Macro Library Guide*.

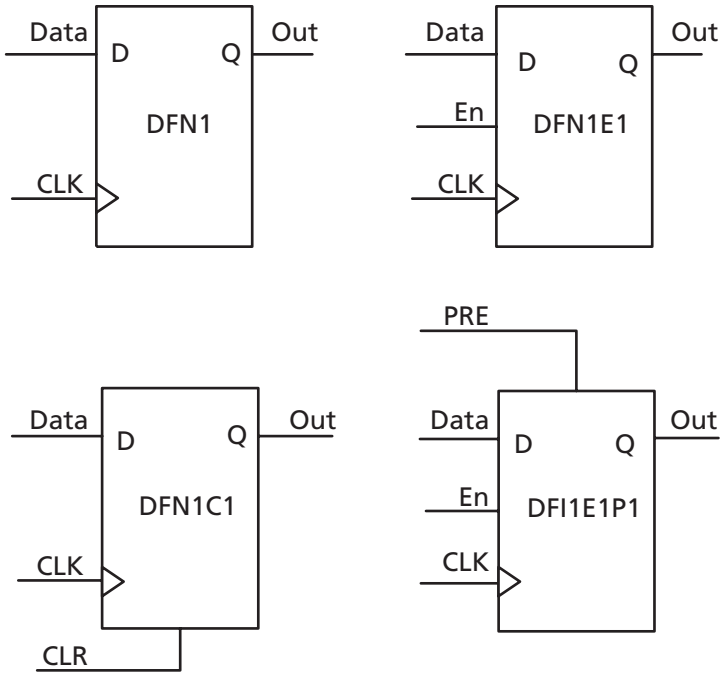

Figure 3-35 • **Sample of Sequential Cells**

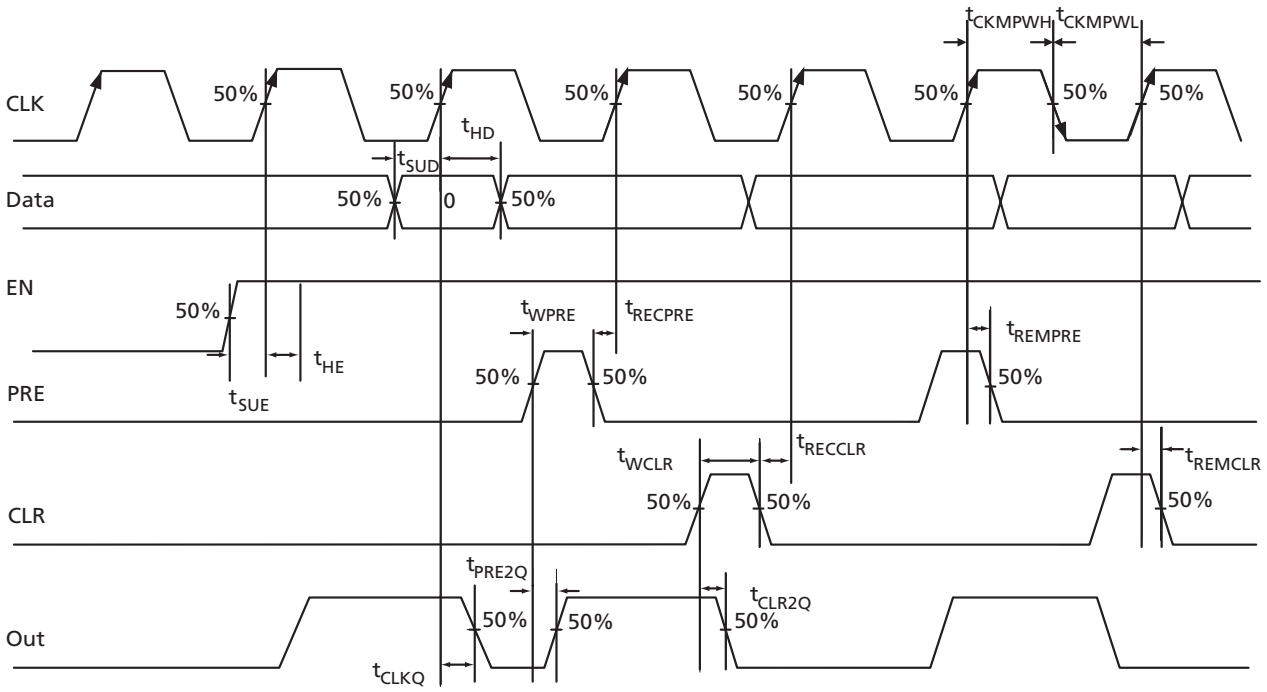

Figure 3-36 • **Timing Model and Waveforms**

Timing Characteristics

Table 3-90 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.54	0.61	0.72	0.86	ns
t_{SUD}	Data Setup time for the Core Register	0.40	0.46	0.54	0.65	ns
t_{HD}	Data Hold time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup time for the Core Register	0.43	0.49	0.57	0.69	ns
t_{HE}	Enable Hold time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	0.64	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	0.64	ns
t_{REMCLR}	Asynchronous Clear Removal time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery time for the Core Register	0.22	0.25	0.30	0.36	ns
t_{REMPRE}	Asynchronous Preset Removal time for the Core Register	0.00	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery time for the Core Register	0.22	0.25	0.30	0.36	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.25	0.28	0.33	0.40	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.25	0.28	0.33	0.40	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.36	0.41	0.48	0.58	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.41	0.46	0.54	0.65	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Global Resource Characteristics

A3PE600 Clock Tree Topology

Clock delays are device-specific. Figure 3-37 is an example of a global tree used for clock routing. The global tree presented in Figure 3-37 is driven by a CCC located on the west side of the A3PE600 device. It is used to drive all D-flip-flops in the device.

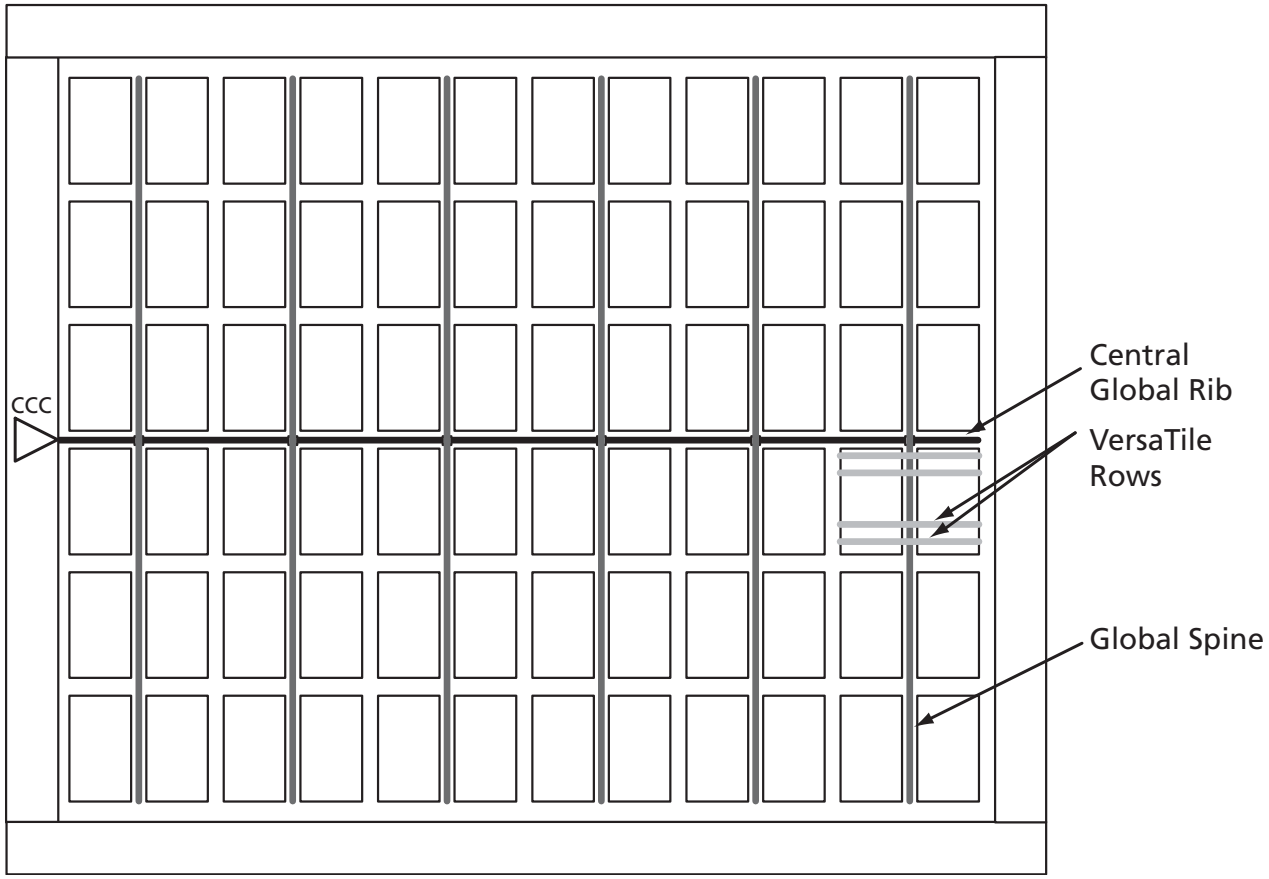

Figure 3-37 • **Example of Global Tree Use in an A3PE600 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard dependent and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, please refer to the "Clock Conditioning Circuits" section on page 2-13. Table 3-91, Table 3-92, and Table 3-93 on page 3-66 present minimum and maximum global clock delays within the device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 3-91 • **A3PE600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.83	1.04	0.94	1.18	1.11	1.39	1.33	1.67	ns
t_{RCKH}	Input High Delay for Global Clock	0.81	1.06	0.93	1.21	1.09	1.42	1.31	1.71	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.25		0.28		0.33		0.40	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-92 • **A3PE1500 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.07	1.29	1.22	1.47	1.43	1.72	1.72	2.07	ns
t_{RCKH}	Input High Delay for Global Clock	1.06	1.32	1.21	1.50	1.42	1.76	1.71	2.12	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34		0.41	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-93 • **A3PE3000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2		–1		Std.		–F		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.41	1.62	1.60	1.85	1.88	2.17	2.26	2.61	ns
t_{RCKH}	Input High Delay for Global Clock	1.40	1.66	1.59	1.89	1.87	2.22	2.25	2.66	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock									ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock									ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.35		0.41	ns
F_{RMAX}	Maximum Frequency for Global Clock									MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Embedded SRAM and FIFO Characteristics

SRAM

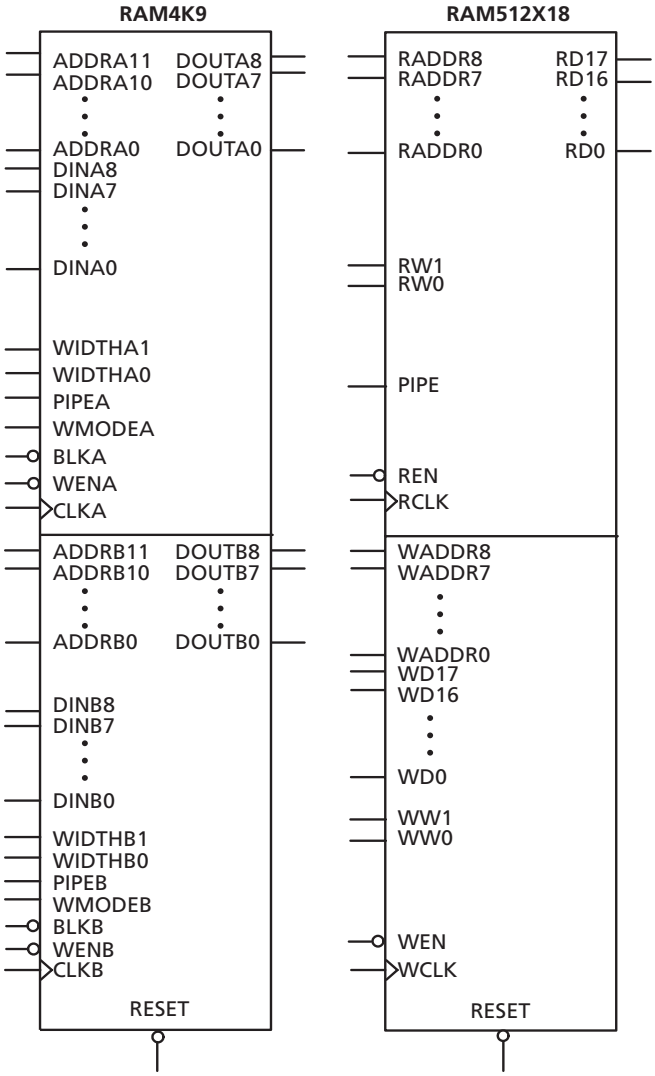

Figure 3-38 • **RAM Models**

Timing Waveforms

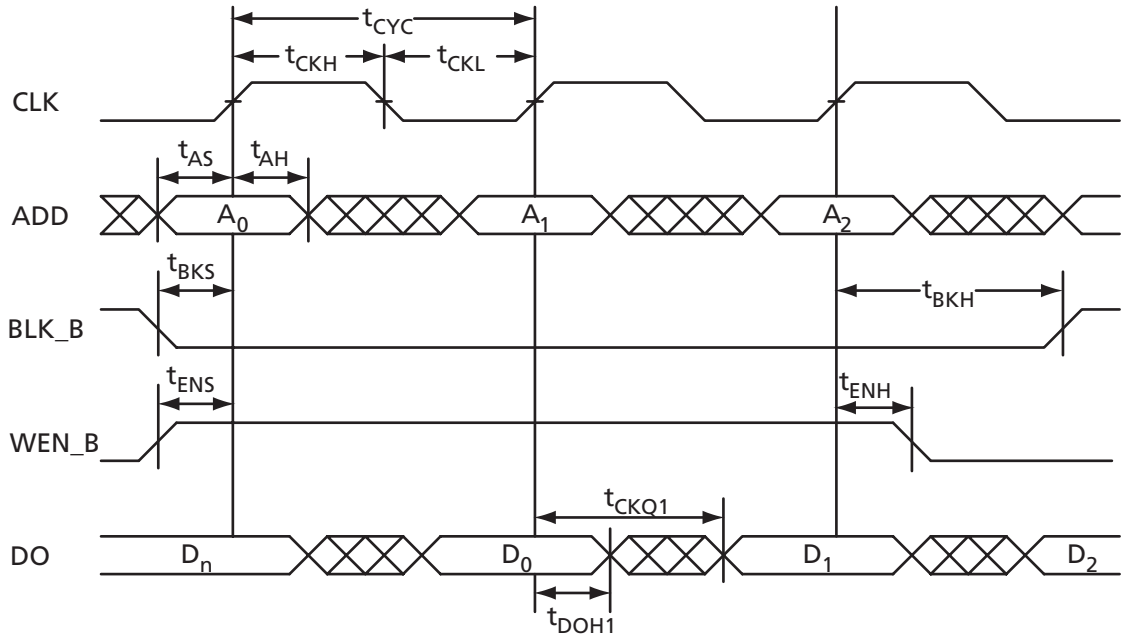

Figure 3-39 • **RAM Read for Pass-Through Output**

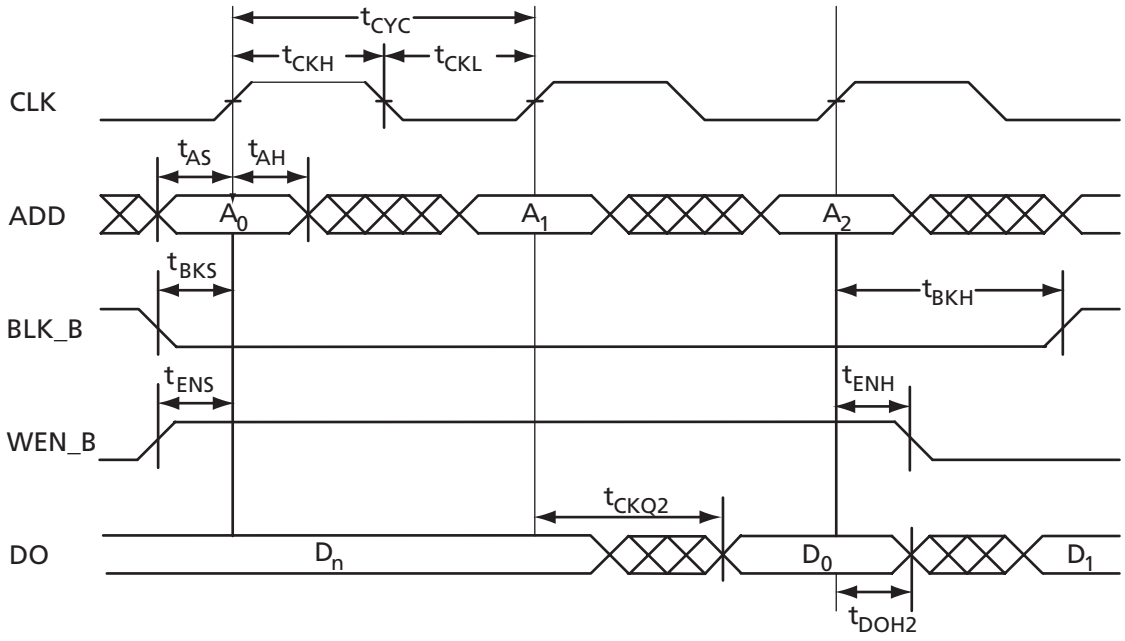

Figure 3-40 • **RAM Read for Pipelined Output**

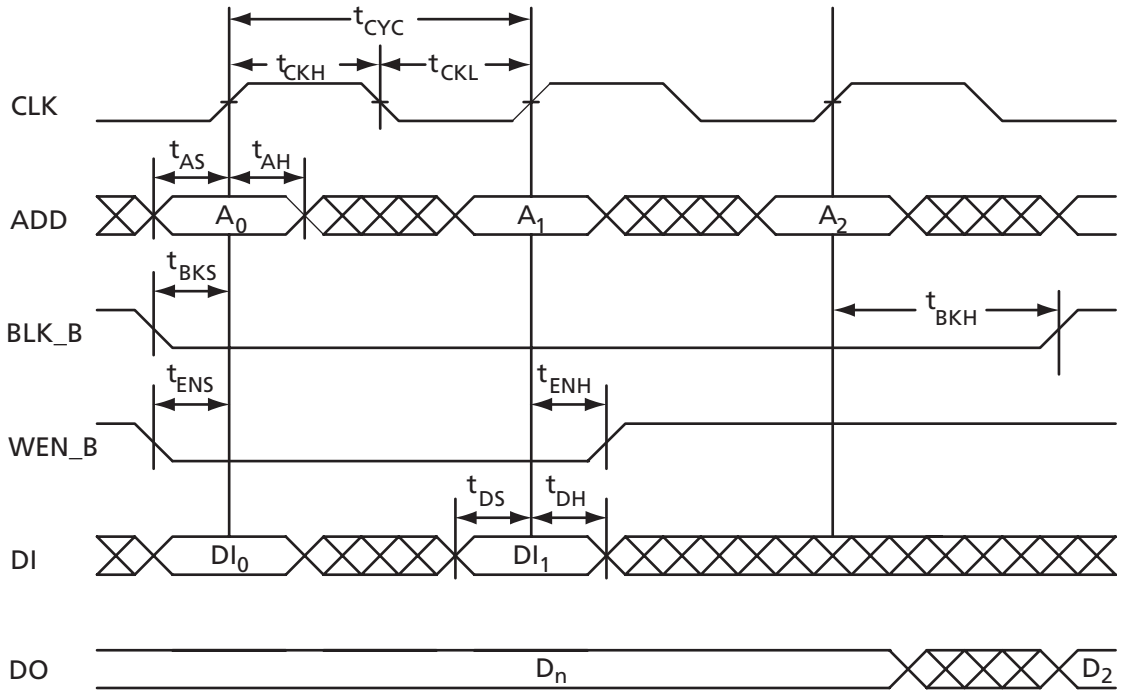

Figure 3-41 • **RAM Write, Output Retained (WMODE = 0)**

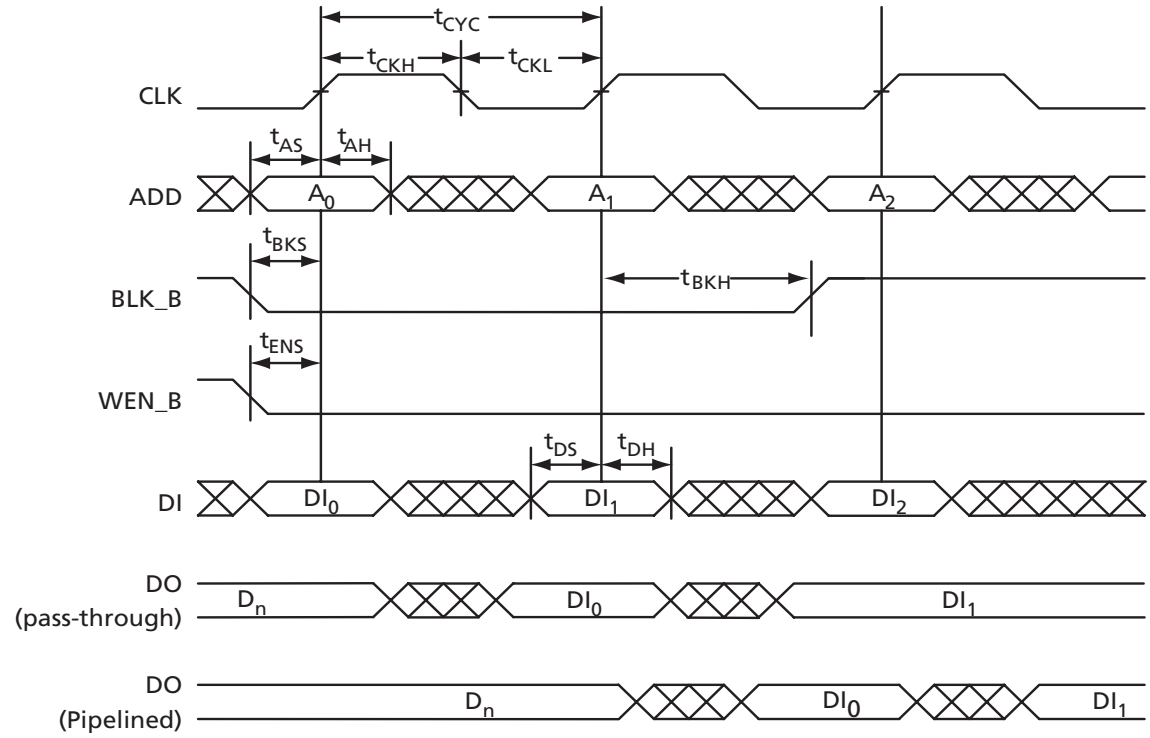

Figure 3-42 • **RAM Write, Output as Write Data (WMODE = 1)**

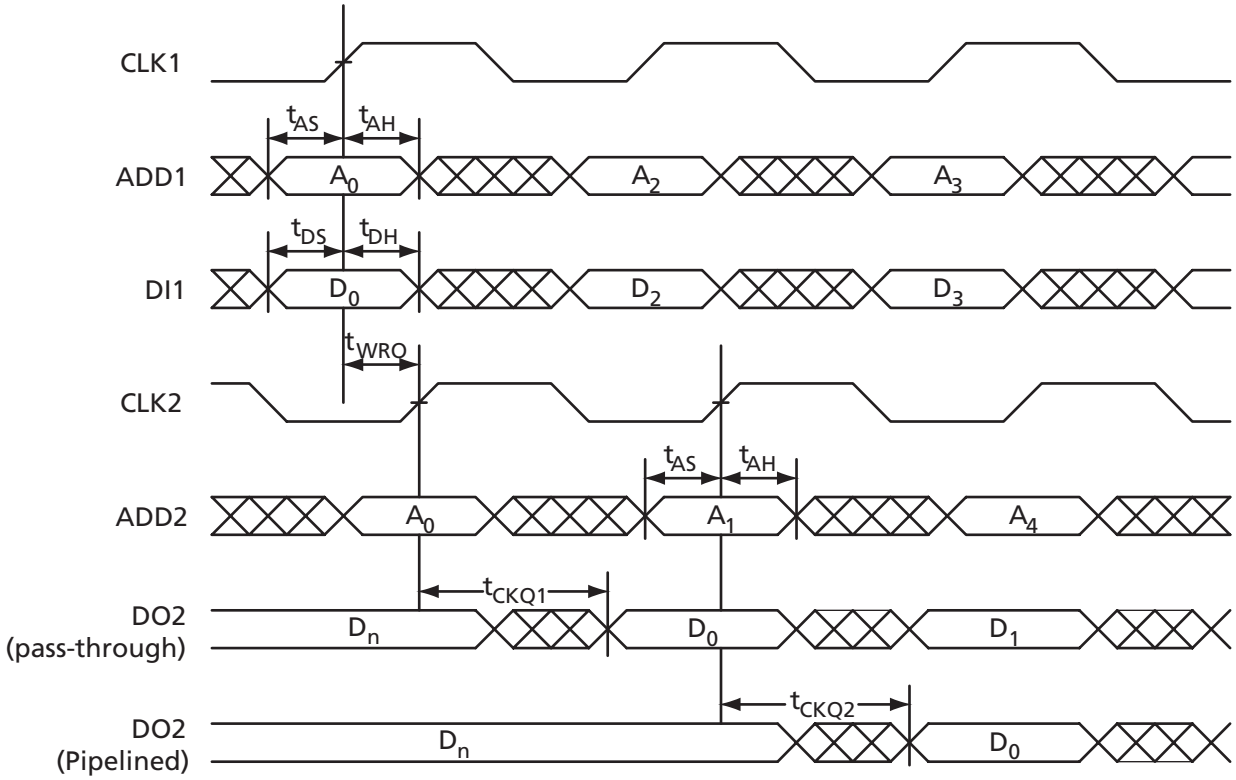

Figure 3-43 • **One Port Write/Other Port Read Same**

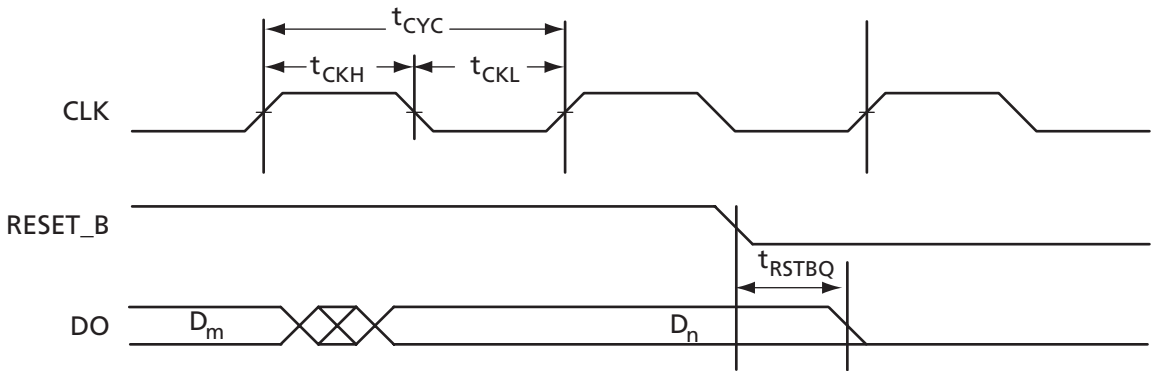

Figure 3-44 • **RAM Reset**

Timing Characteristics

Table 3-94 • **RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{AS}	Address Setup time	0.30	0.34	0.40	0.48	ns
t_{AH}	Address Hold time	0.00	0.00	0.00	0.00	ns
t_{ENS}	REN_B,WEN_B Setup time	0.20	0.22	0.26	0.32	ns
t_{ENH}	REN_B, WEN_B Hold time	0.03	0.03	0.04	0.05	ns
t_{BKS}	BLK_B Setup time	0.29	0.33	0.39	0.47	ns
t_{BKH}	BLK_B Hold time	0.00	0.00	0.00	0.00	ns
t_{DS}	Input data (DI) Setup time	0.24	0.27	0.32	0.38	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	1.58	1.80	2.11	2.54	ns
	Clock High to New Data Valid on DO (pass-through, WMODE = 1)	2.12	2.42	2.84	3.42	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	0.69	0.79	0.93	1.12	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (pass-through)	0.82	0.94	1.10	1.32	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.82	0.94	1.10	1.32	ns
$t_{REMRSTB}$	RESET_B Removal	0.31	0.35	0.41	0.49	ns
$t_{RECRSTB}$	RESET_B Recovery	1.38	1.56	1.84	2.21	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.20	0.23	0.27	0.33	ns
t_{CYC}	Clock Cycle time	1.96	2.22	2.61	3.14	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Table 3-95 • **RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{AS}	Address Setup time	0.30	0.34	0.40	0.48	ns
t_{AH}	Address Hold time	0.00	0.00	0.00	0.00	ns
t_{ENS}	REN_B,WEN_B Setup time	0.24	0.28	0.32	0.39	ns
t_{ENH}	REB_B, WEN_B Hold time	0.00	0.00	0.00	0.00	ns
t_{DS}	Input data (DI) Setup time	0.22	0.25	0.30	0.36	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	1.93	2.19	2.58	3.10	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	0.70	0.79	0.93	1.12	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (pass-through)	0.82	0.94	1.10	1.32	ns
	RESET_B Low to Data Out Low on DO (pipelined)	0.82	0.94	1.10	1.32	ns
$t_{REMRSTB}$	RESET_B Removal	0.31	0.35	0.41	0.49	ns
$t_{RECRSTB}$	RESET_B Recovery	1.38	1.56	1.84	2.21	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.20	0.23	0.27	0.33	ns
t_{CYC}	Clock Cycle time	1.96	2.22	2.61	3.14	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

FIFO

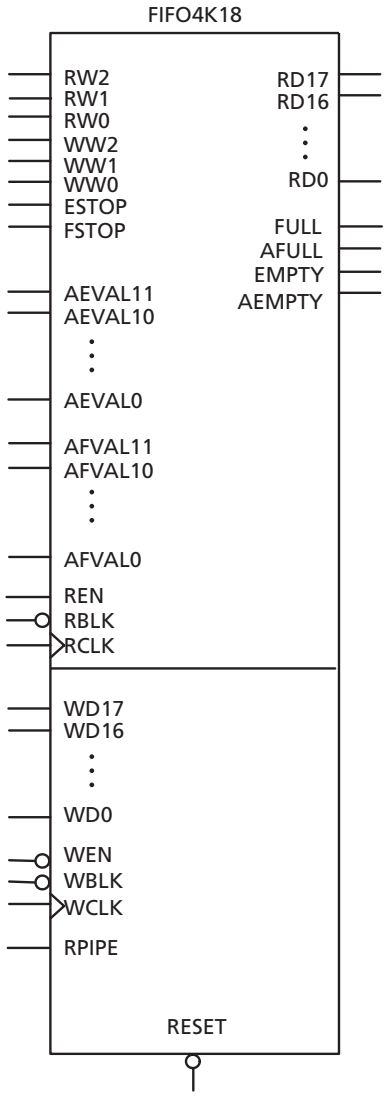

Figure 3-45 • **FIFO Model**

Timing Waveforms

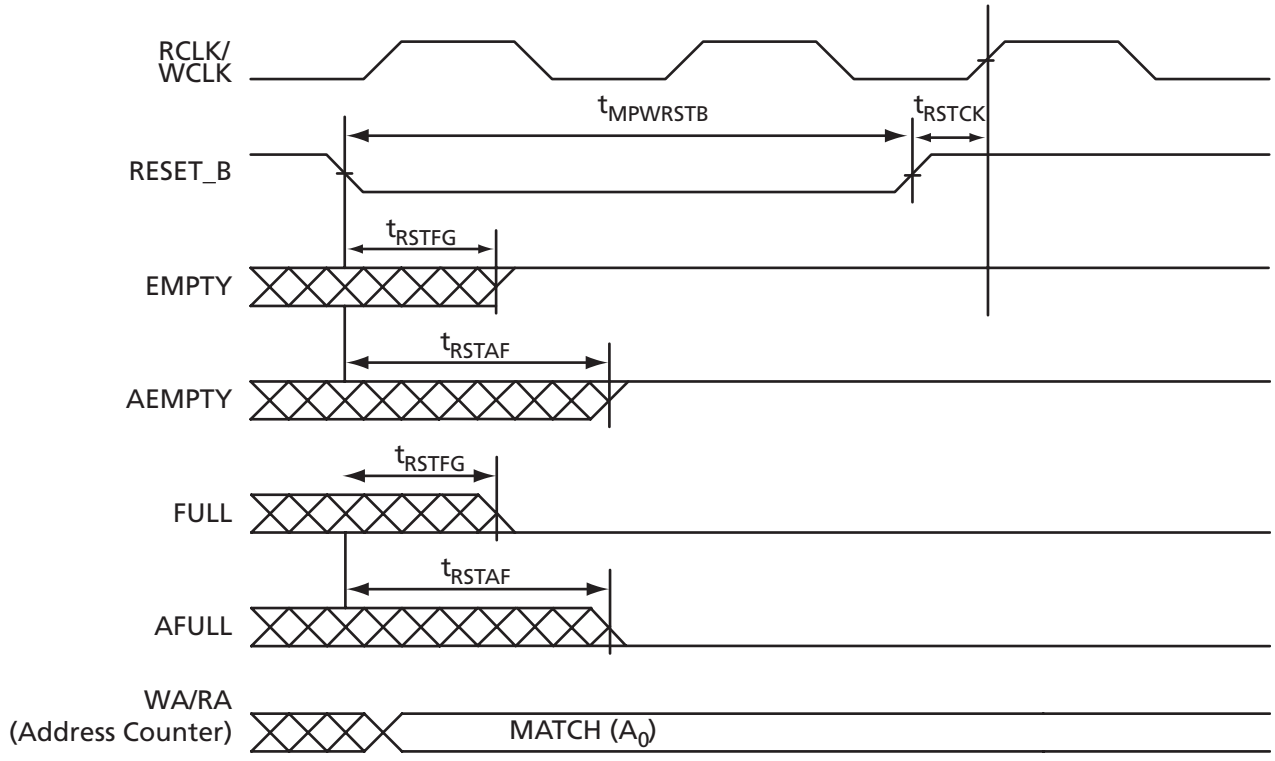

Figure 3-46 • **FIFO Reset**

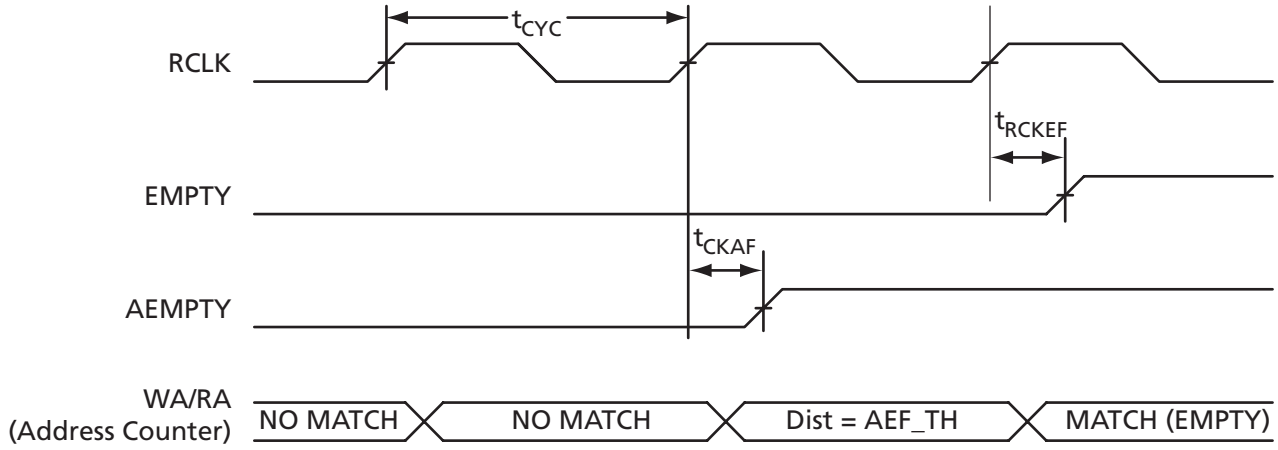

Figure 3-47 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

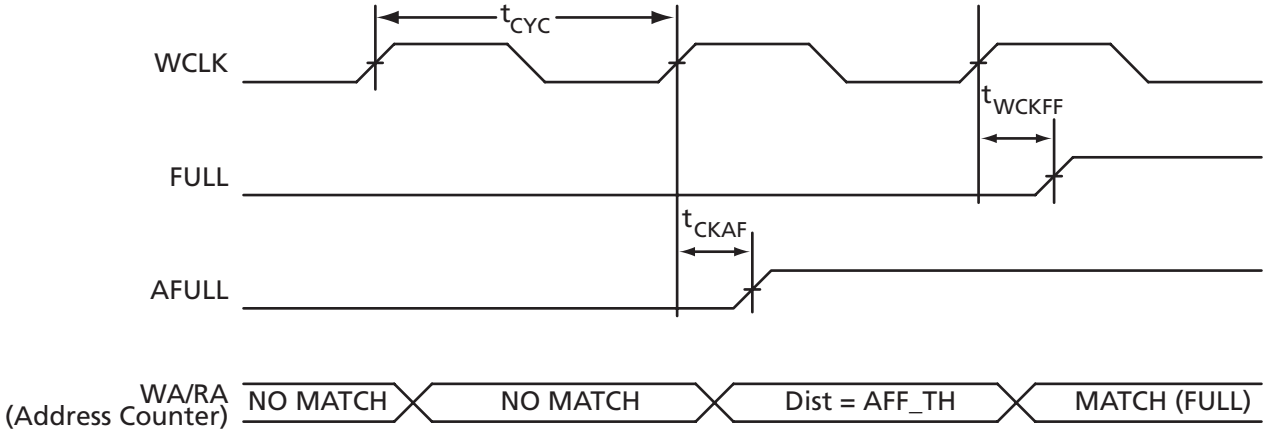

Figure 3-48 • **FIFO FULL Flag and AFULL Flag Assertion**

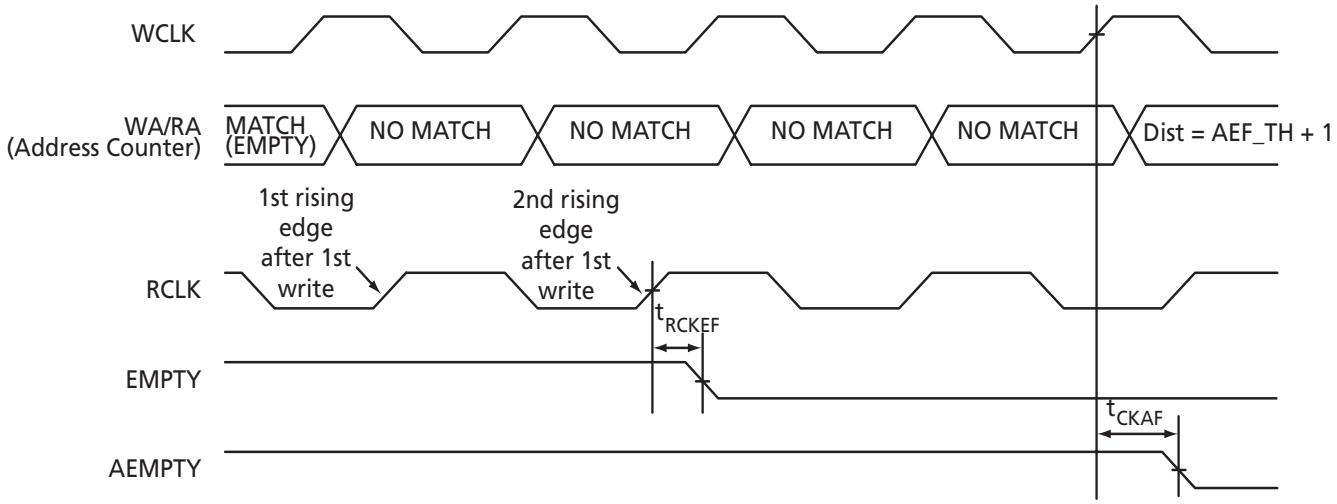

Figure 3-49 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

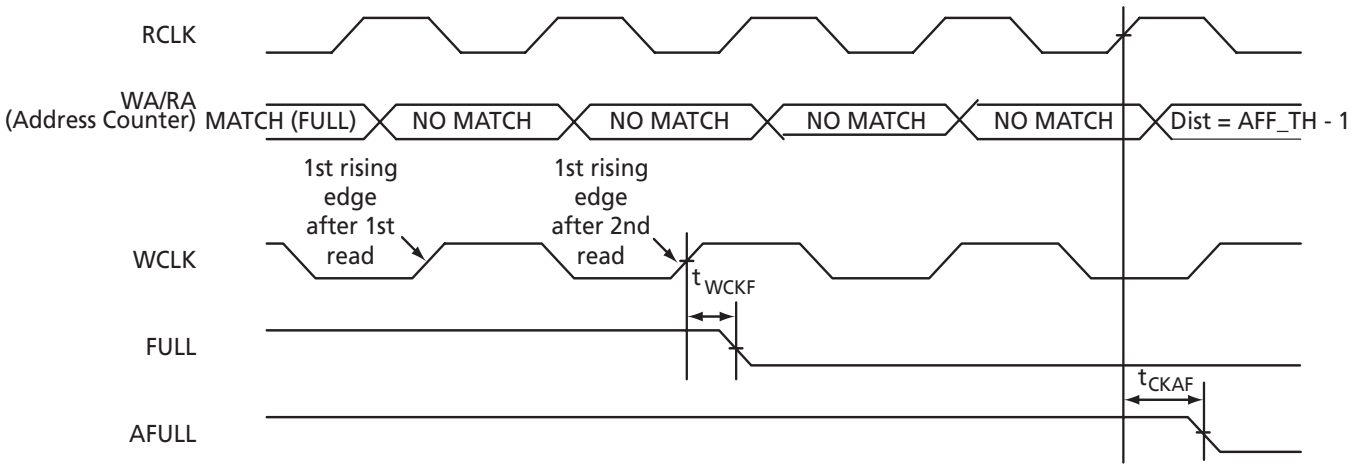

Figure 3-50 • **FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

Table 3-96 • **FIFO**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	–F	Units
t_{ENS}	REN_B,WEN_B Setup time	0.28	0.32	0.38	0.45	ns
t_{ENH}	REN_B, WEN_B Hold time	0.00	0.00	0.00	0.00	ns
t_{BKS}	BLK_B Setup time	0.25	0.29	0.34	0.40	ns
t_{BKH}	BLK_B Hold time	0.00	0.00	0.00	0.00	ns
t_{DS}	Input data (DI) Setup time	0.22	0.25	0.30	0.36	ns
t_{DH}	Input data (DI) Hold time	0.00	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on DO (pass-through)	2.12	2.42	2.84	3.42	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	0.69	0.79	0.93	1.12	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.53	1.74	2.05	2.46	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.45	1.65	1.94	2.33	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	3.50	3.99	4.69	5.63	ns
t_{RSTFG}	RESET_B Low to Empty/Full Flag valid	1.55	1.77	2.08	2.49	ns
t_{RSTAF}	RESET_B Low to Almost-Empty/Full Flag Valid	3.43	3.91	4.59	5.52	ns
t_{RSTBQ}	RESET_B Low to Data out Low on DO (pass-through)	0.82	0.94	1.10	1.32	ns
	RESET_B Low to Data out Low on DO (pipelined)	0.82	0.94	1.10	1.32	ns
$t_{REMRSTB}$	RESET_B Removal	0.30	0.34	0.40	0.48	ns
$t_{RECRSTB}$	RESET_B Recovery	1.35	1.53	1.80	2.17	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.20	0.23	0.27	0.32	ns
t_{CYC}	Clock Cycle time	1.94	2.20	2.59	3.11	ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*

Embedded FlashROM Characteristics

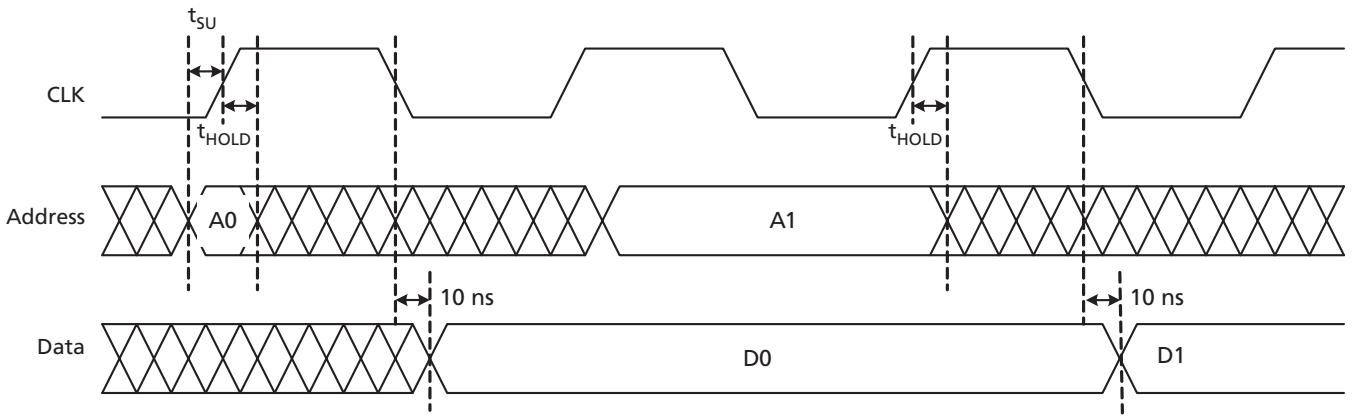

Figure 3-51 • **Timing Diagram**

Timing Characteristics

Table 3-97 • **Embedded FlashROM Access Time**

Parameter	Description	–2	–1	Std.	Units
t_{SU}	Address setup Time	TBD	TBD	TBD	ns
t_{HOLD}	Address Hold Time	TBD	TBD	TBD	ns
t_{CK2Q}	Clock to out	TBD	TBD	TBD	ns
F_{MAX}	Maximum Clock frequency	TBD	TBD	TBD	Mhz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected, refer to the I/O Timing characteristics for more details.

Timing Characteristics

Table 3-98 • **JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time				ns
t_{DIHD}	Test Data Input Hold Time				ns
t_{TMSSU}	Test Mode Select Setup Time				ns
t_{TMDHD}	Test Mode Select Hold Time				ns
t_{TCK2Q}	Clock to Q (Data Out)				ns
t_{RSTB2Q}	Reset to Q (Data Out)				ns
F_{TCKMAX}	TCK maximum frequency	20	20	20	MHz
$t_{TRSTREM}$	ResetB Removal time				ns
$t_{TRSTREC}$	ResetB Recovery time				ns
$t_{TRSTMPW}$	ResetB minimum pulse				ns

Note: *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-4 for derating values.*