Using Global Resources in Actel ProASIC3/E Devices

Introduction

Actel ProASIC3/E FPGA devices offer a powerful, low-delay VersaNet global network scheme and have extensive support for multiple clock domains. In addition to the Clock Conditioning Circuits (CCC) and Phase-Locked Loop (PLL), there is a comprehensive global clock distribution network called a VersaNet global network. Each VersaTile input and output port has access to these global networks. The VersaNet global networks can be used to distribute low-skew clock signals or high-fanout nets. In addition, these highly-segmented VersaNet global networks offer users the flexibility to create low-skew local networks using spines. This application note describes VersaNet global networks and discusses how to assign signals to these global networks and spines in a design flow. This application note covers the ProASIC3/E global architecture and uses of these global networks in designs.

ProASIC3/E Global Architecture

The following sub-sections give an overview of the ProASIC3/E VersaNet global network, the structure of the global network, and the clock aggregation feature that enables a design to have very low clock skew using spines.

VersaNet Global Network Distribution

One of the architectural benefits of ProASIC3/E is the set of powerful, low-delay VersaNet global networks. ProASIC3/E offers six chip global networks that are distributed from the center of the FPGA array. In addition, each ProASIC3/E device, except A3P030, has four quadrant global networks, each with three regional global network resources. These quadrant global networks can only drive a signal inside their own quadrant. In total, each core VersaTile has access to nine global network resources (six chip global networks and three quadrant global networks). Figure 1 on page 2 shows simplified ProASIC3/E architecture and Figure 2 on page 2 shows an overview of the VersaNet global networks.

The VersaNet global networks are segmented and consist of VersaNet global networks, spines, global ribs, and global multiplexers (MUXes), as shown in Figure 2 on page 2. The global networks are driven from the global rib at the center of the die or quadrant global networks at the north or south side of the die. The global network uses the MUX trees to access the spine, and the spine uses the clock ribs to access the VersaTile. You have access to the chip or quadrant global networks and the spines through the global MUXes. Access to the spine using the global MUXes is explained in the "Spine Architecture" section on page 3. This flexible structure allows you to have up to 252 internal/external clocks in the device.

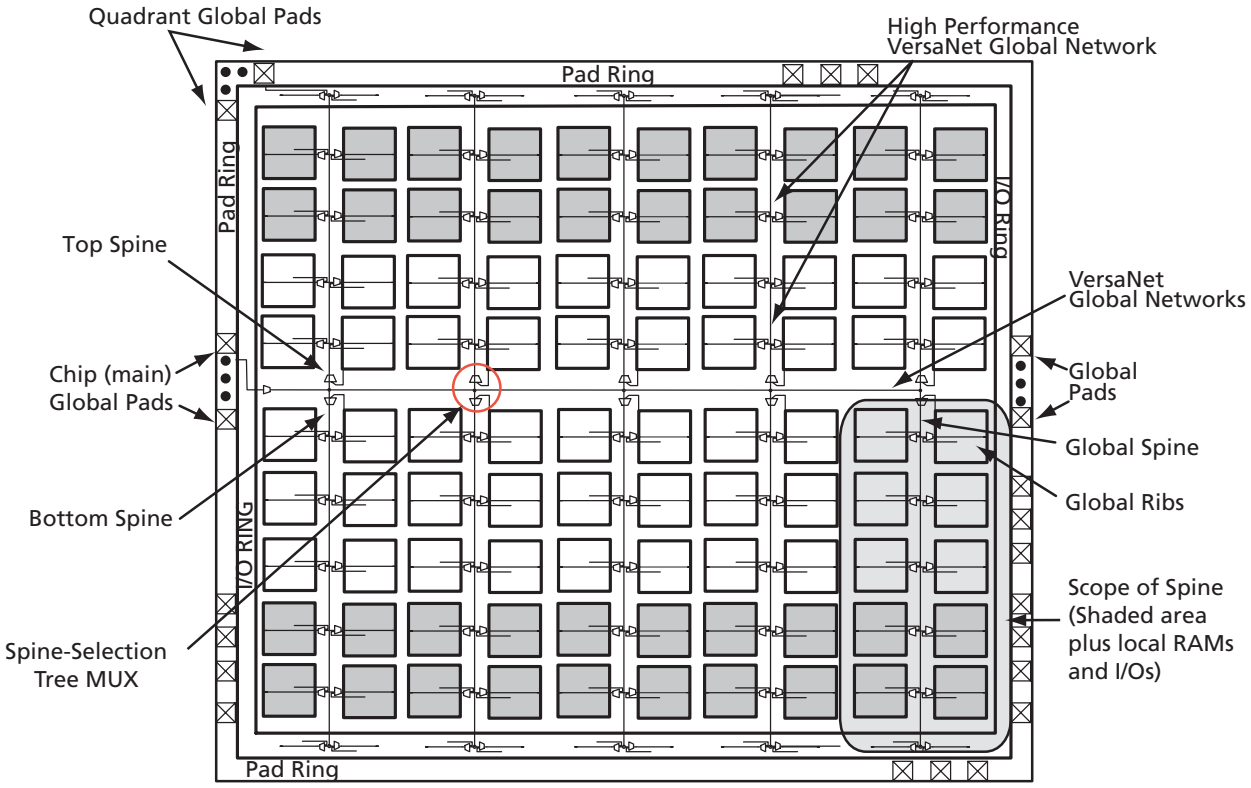


Figure 1 • **Overview of ProASIC3E VersaNet Global Network**

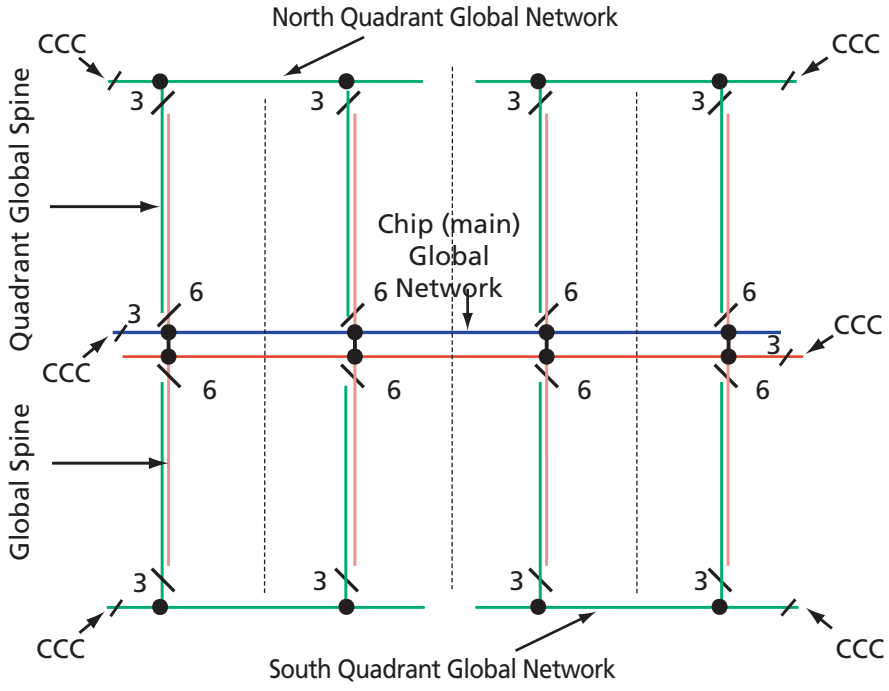


Figure 2 • **VersaNet Global Overview**

Spine Architecture

The ProASIC3/E architecture allows the VersaNet global networks to be segmented. Each of these networks contains spines (the vertical branches of the global network tree) and rows that can reach all the VersaTiles inside its region. Each spine covers a certain area of the ProASIC3/E device, called the "Scope of Spine" (shown in Figure 1 on page 2). In total, there are nine spines available (shown in Figure 2 on page 2) in each spine location/tree for all ProASIC3/E devices (except A3P030). In A3P030 there is no quadrant clock network, so there are only six spines in each spine tree. In other devices, the nine spines available in the spine tree come from global networks with two separate regions of scope: the quadrant global network, which has three spines, and the main global network, which has six spines. Global networks drive the chip spines from the center of the die and the north/south global network drives quadrant spines from the north or south side of the die. Access to the top quadrant spine regions is from the top of the die, and access to the bottom quadrant spine regions is from the bottom of the die (Figure 2 on page 2).

Each spine in a vertical column of a chip global network is further divided into two spine segments, one in the top half of the die and one in the bottom. Top and bottom spine segments radiating from the center of a device have the same height. However, just as in the ProASIC^{PLUS}® family, signals assigned only to the top and bottom spine cannot access the middle two rows of the die. The spines for quadrant clock networks do not cross the middle of the die and cannot access the middle two rows of the architecture. Table 1 lists the chip globals and spines in different ProASIC3/E devices. The A3PE3000 device has 28 spine trees and each spine tree has 9 spines; this flexible global network architecture enables users to map up to 252 different internal/external clocks in an A3PE3000 device.

Table 1 • **Global/Spines/Rows by Devices**

Die	Global Clock Networks	Quadrant Clock Networks	Clock Tree	Total Spines	VersaTiles in Each Top or Bottom Spine
A3P030	6	0	4	24	384
A3P060	6	4	4	36	384
A3P125	6	4	4	36	384
A3P250	6	4	8	72	768
A3P400	6	4	8	72	768
A3P600	6	4	12	108	1152
A3P1000	6	4	16	144	1536
A3PE600	6	4	12	108	1,120
A3PE1500	6	4	20	180	1,888
A3PE3000	6	4	28	252	2,656

The physical location of each spine is identified by the letter T (top) or B (bottom) and an accompanying number (Tn or Bn). The number n indicates the horizontal location of the spine; 1 refers to the first spine on the left side of the die. Since there are six chip spines in each spine tree, there are up to six spines available for each combination of T (or B) and n (for example, six T1 spines). Similarly, there are three quadrant spines available for each combination of T (or B) and n (for example, four T1 spines), as shown in Figure 2 on page 2. Table 2 on page 4 lists the spines for different ProASIC3/E devices.

Table 2 • **List of Spines in ProASIC3/E Devices**

Die	Spines
A3P030	B1:B2, T1:T2
A3P060	B1:B2, T1:T2
A3P125	B1:B2, T1:T2
A3P250	B1:B4, T1:T4
A3P400	B1:B4, T1:T4
A3P600	B1:B6, T1:T6
A3P1000	B1:B8, T1:T8
A3PE600	B1:B6, T1:T6
A3PE1500	B1:B10, T1:T10
A3PE3000	B1:B14, T1:T14

Spine Access

Spines are also called local clocks, and are accessed by the dedicated global MUX architecture. These MUXes define how a particular spine is driven. Refer to Figure 3 for the global MUX architecture. The MUXes for each chip global spine are located in the middle of the die. Access to the top and bottom chip global spine is available from the middle of the die. There is no control dependency between the top and bottom spines. If a top spine, T1, of a chip global network is assigned to a net, then B1 is not wasted and can be used by the global clock network. The signal assigned only to the top or bottom spine cannot access the middle two rows of the architecture. However, if a spine is using the top and bottom at the same time (T1 and B1, for instance), then the previous restriction is lifted.

The MUXes for each quadrant global spine are located in the north and south sides of the die. The access for the top and bottom quadrant global spine are available from the north and south sides of the die. Since the MUXes for quadrant spines are located in the north and south sides of the die, you should not try to drive T1 and B1 quadrant spines from the same signal.

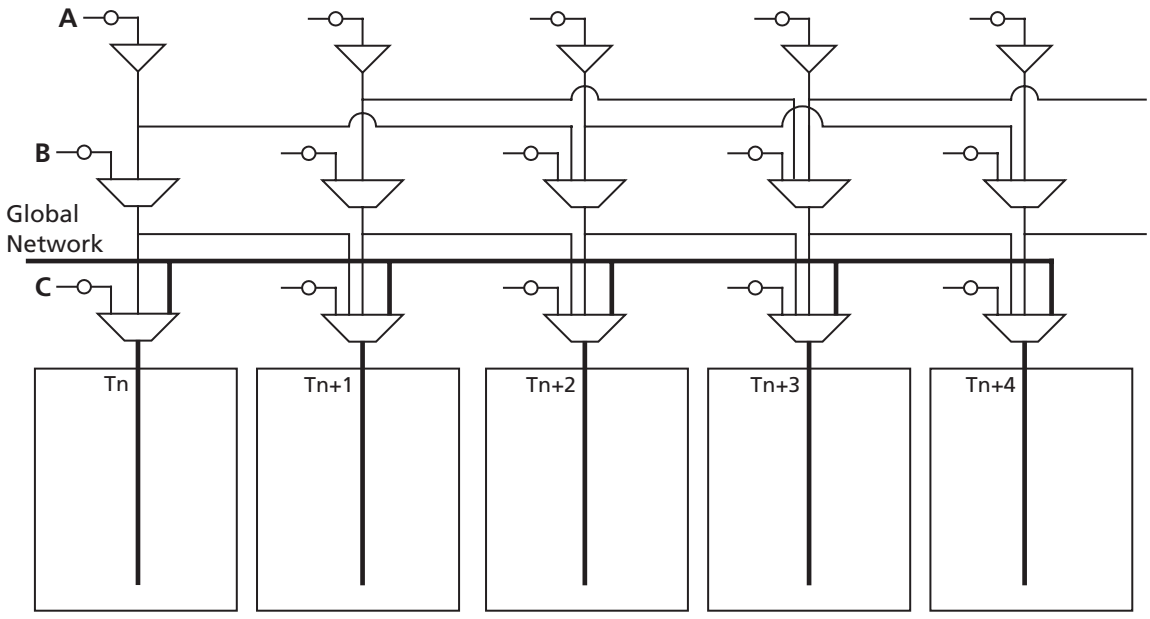


Figure 3 • **Chip Global Aggregation**

Clock Aggregation

ProASIC3/E has a clock aggregation feature that allows for multi-spine assignment using hardwired connections, without adding any extra skew. The MUX tree mentioned in the "Spine Access" section on page 4 provides the necessary flexibility to allow long lines, local resources, or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the center of the die, and also through local resources in the north and south side of the die, allowing I/Os to directly feed into the clock system. This clock aggregation feature allows a balanced clock tree, which improves the clock skew. The physical regions for clock aggregation are defined from left to right and shift by one spine. For chip global networks, there are three types of clock aggregation available, as shown in Figure 3 on page 4:

- Long lines that can drive up to four adjacent spines
- Long lines that can drive up to two adjacent spines
- Long lines that can drive one spine

There are three types of clock aggregation available for the quadrant spines, as shown in Figure 4:

- I/Os or local resources that can drive up to four adjacent spines
- I/Os or local resources that can drive up to two adjacent spines
- I/Os or local resources that can drive one spine
- As an example, A3PE600 devices have twelve spine locations: T1, T2, T3, T4, T5, T6, B1, B2, B3, B4, B5, and B6. Table 3 shows the clock aggregation you can have in A3PE600.

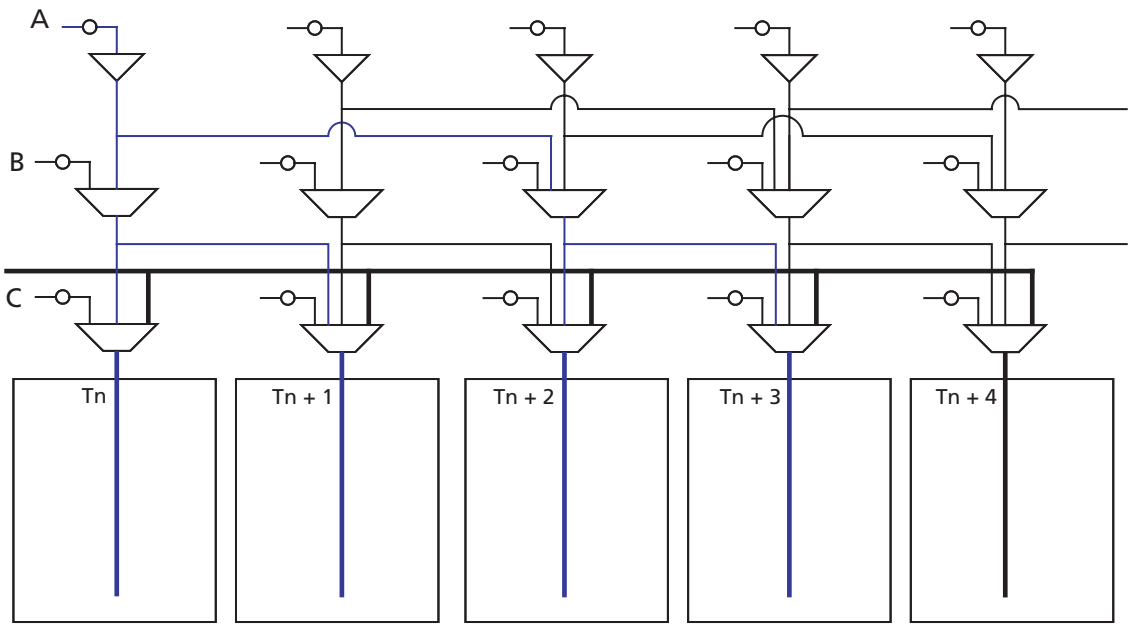


Figure 4 • **Four Spines Aggregation**

Table 3 • **Spine Aggregation in A3PE600**

Clock Aggregation	Spine
1 spine	T1, T2, T3, T4, T5, T6, B1, B2, B3, B4, B5, B6
2 spines	T1:T2, T2:T3, T3:T4, T4:T5, T5:T6, B1:B2, B2:B3, B3:B4, B4:B5, B5:B6
4 spines	B1:B4, B2:B5, B3:B6, T1:T4, T2:T5, T3:T6

The clock aggregation for the quadrant spines can cross over from the left to right quadrant, but not from top to bottom. The quadrant spine assignment T1:T4 is legal, but the quadrant spine assignment T1:B1 is not legal. Note that this clock aggregation is hardwired. You can always assign signals to spine T1 and B2 by instantiating a buffer, but this may add skew in the signal.

I/O Banks and Global I/Os

Naming of Global I/Os

In ProASIC3/E devices, the global I/Os have access to certain clock conditioning circuitry and have direct access to the global network. Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities to those of regular I/Os. Due to the comprehensive and flexible nature of the I/Os in ProASIC3/E devices, a naming scheme is used to show the details of the I/O. The global I/O uses the generic name, Gmn/IOuxwByVz. Refer to the *ProASIC3 Flash Family FPGAs* and *ProASIC3E Flash Family FPGAs* datasheets for more information.

Figure 5 on page 7 represents the global input pins connection to the northwest CCC or northwest quadrant global networks. It shows 9 global I/Os available for each CCC. Note these 9 I/Os may not be located in the same bank. Since each bank can have a different I/O standard, the user should pay attention to choose the correct global I/O for their design. There are 54 global pins available to access 18 global networks (except in the A3P030 device). For the single-ended and voltage-referenced I/O standard, you may use any of these three available I/Os to access the global network. For differential I/O standards such as LVDS and LVPECL, the I/O macro needs to be placed on GAA0x and GAA1x or similar locations. The unassigned global I/Os can be used as regular I/Os. Note that pin names starting with GF and GC are associated with the chip global networks, and GA, GB, GD, and GE are used for quadrant global networks.

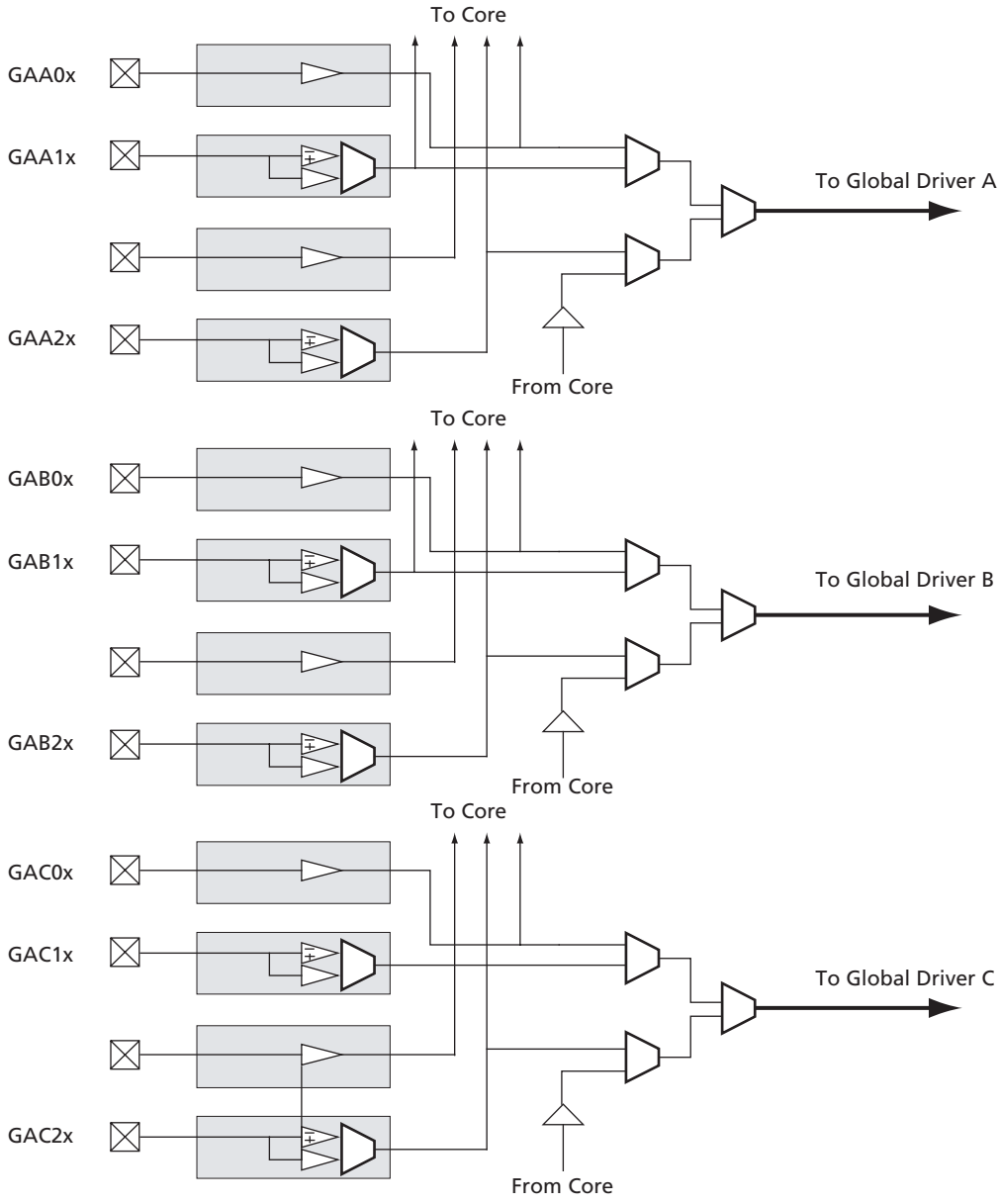


Figure 5 • **Global I/O Overview**

Unused Global I/O Configuration

The unused clock inputs behave similarly to the unused Pro I/Os. The Actel Designer software automatically configures the unused global pins as tristated outputs.

I/O Banks and Global I/O Standards

In ProASIC3/E devices, any I/O or internal logic can be used to drive the global network. However, only the global macro placed at the global pins will use the hardwired connection between the I/O and global network. Global signal (signal driving a global macro) assignment to I/O banks is no different from regular I/O assignment to I/O banks with the exception that you are limited to the pin placement location available. Only global signals compatible with both the V_{CCI} and V_{REF} standards can be assigned to the same bank.

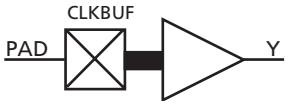
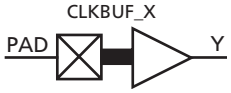
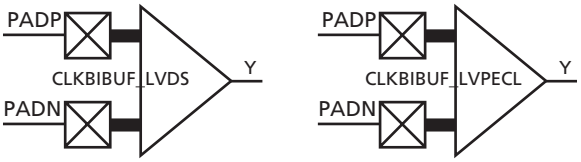
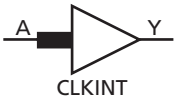
Design Recommendations

The following sections provide design flow recommendations for using a global network in ProASIC3/E design.

Global Macros and I/O Standards

ProASIC3/E devices have six chip global networks and four quadrant clock networks. However, the same clock macros are used for assigning signals to chip globals and quadrant globals. Depending on the clock macro placement or assignment in the Physical Design Constraint (PDC) file or MultiView Navigator (MVN), the signal will use the chip global network or quadrant network. Table 4 lists the clock macros available for ProASIC3/E devices. Refer to the *ProASIC3/E Macro Library Guide* for details.

Table 4 • **ProASIC3/E Clock Macros**

Macro Name	Description	Symbol
CLKBUF	Input macro for Clock Network	
CLKBUF_x	Input macro for Clock Network with specific I/O standard	
CLKBUF_LVDS/ LVPECL	LVDS or LVPECL input macro for Clock Network	
CLKINT	Internal clock interface	
CLKBIBUF	Bidirectional macro with input dedicated to routed Clock Network	

Use these available macros to assign a signal to the global network. In addition to these global macros, PLL and CLKDLY macros can also drive the global networks. Use I/O standard-specific clock macros (CLKBUF_x) to instantiate a specific I/O standard for the global signals. Table 5 shows the list of these I/O standard-specific macros. Note that if you use these I/O standard-specific clock macros, you cannot change the I/O standard later in the design stage. If you use the regular CLKBUF macro, you can use MVN or the PDC file in Designer to change the I/O standard. The default I/O standard for CLKBUF is LVTTL in the current Libero® Integrated Design Environment (IDE) and Designer software.

Table 5 • **I/O Standards within CLKBUF**

Name	Description
CLKBUF_LVCMOS5	LVCMOS Clock buffer with 5.0 CMOS voltage level
CLKBUF_LVCMOS33	LVCMOS Clock buffer with 3.3 CMOS voltage level
CLKBUF_LVCMOS25	LVCMOS Clock buffer with 2.5 CMOS voltage level[1]
CLKBUF_LVCMOS18	LVCMOS Clock buffer with 1.8 CMOS voltage level
CLKBUF_LVCMOS15	LVCMOS Clock buffer with 1.5 CMOS voltage level
CLKBUF_PCI	PCI Clock buffer
CLKBUF_PCIX	PCIX Clock buffer
CLKBUF_GTL25	GTL Clock buffer with 2.5 CMOS voltage level[1]
CLKBUF_GTL33	GTL Clock buffer with 3.3 CMOS voltage level[1]
CLKBUF_GTLP25	GTLP Clock buffer with 2.5 CMOS voltage level[1]
CLKBUF_GTLP33	GTLP Clock buffer with 3.3 CMOS voltage level[1]
CLKBUF_ HSTL _I	HSTL Class I Clock buffer[1]
CLKBUF_ HSTL _II	HSTL Class II Clock buffer[1]
CLKBUF_SSTL2_I	SSTL2 Class I Clock buffer[1]
CLKBUF_SSTL2_II	SSTL2 Class II Clock buffer[1]
CLKBUF_SSTL3_I	SSTL3 Class I Clock buffer[1]
CLKBUF_SSTL3_II	SSTL3 Class II Clock buffer[1]

Notes:

1. *Not supported in ProASIC3.*
2. *By default, the CLKBUF macro uses the 3.3 V LVTTL I/O technology.*

The current synthesis tool libraries only infer the CLKBUF or CLKINT macros in the netlist. All other global macros must be instantiated manually into your Hardware Description Language (HDL) code. The following is an example of CLKBUF_LVCMOS25 global macro instantiations that you can copy and paste into your code:

```
VHDL:

component clkbuf_lvcmos25
port (pad : in std_logic; y : out std_logic);
end component
begin
-- concurrent statements
u2 : clkbuf_lvcmos25 port map (pad =>  ext_clk, y => int_clk);
end


Verilog:

module design (_______);
input ______;
output _______;
clkbuf_lvcmos25 u2 (.y(int_clk), .pad(ext_clk);
endmodule
```

Using Global Macros in Synplicity®

The Synplify® synthesis tool automatically inserts global buffers for nets with high fanout during synthesis. By default, Synplicity puts six global macros (CLKBUF or CLKINT) in the netlist, including any global instantiation or PLL macro. Synplify always honors your global macro instantiation. If you have a PLL (only primary output is used) in the design, Synplilfy adds five more global buffers in the netlist. Synplify uses the following global counting rule to add global macros in the netlist:

1. CLKBUF: 1 global buffer
2. CLKINT: 1 global buffer
3. CLKDLY: 1 global buffer
4. PLL: 1 to 3 global buffers
   - GLA, GLB, GLC, YB, and YC are counted as 1 buffer.
   - GLB or YB is used or both are counted as 1 buffer.
   - GLC or YC is used or both are counted as 1 buffer.

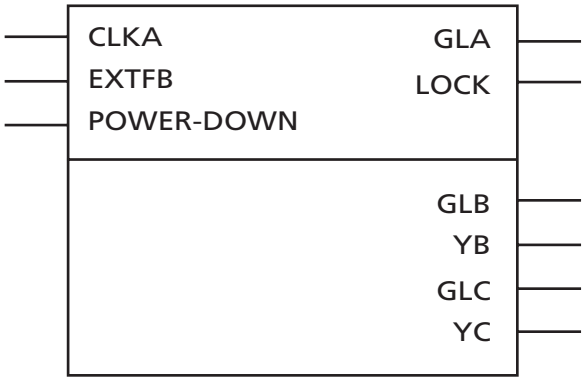


Figure 6 • **PLL in ProASIC3/E**

You can use the syn_global_buffers attribute in Synplify to specify a maximum number of global macros to be inserted in the netlist. This can also be used to restrict the number of global buffers inserted. In the current Synplicity 8.1 version, a new attribute "syn_global_minfanout" has been added for ProASIC3/E devices. This enables you to promote only the high fanout signal to global. However, be aware that you can only have six signals assigned to chip global networks and the rest of the global signals should be assigned to quadrant global networks. So, if the netlist has 18 global macros, the remaining 12 global macros should have fanout that allows the instances driven by these globals to be placed inside a quadrant.

Global Promotion and Demotion Using PDC

The HDL source file or schematic is the preferred place for defining which signals should be assigned to a clock network using clock macro instantiation. This method is preferred because it is guaranteed to be honored by the synthesis tools and Designer software and stop any replication on this net by the synthesis tool. Note that a signal with fanout may have logic replication if it is not promoted to global during synthesis. In that case, the user cannot promote that signal to global using PDC. Please check synplicity help for details on using this attribute.To help you with global management, Designer software allows you to promote a signal to a global network or demote a global macro to a regular macro from the user netlist using the Compile Options and/or PDC command.

The following are the PDC constraints you can use to promote a signal to a global network:

1. PDC syntax to promote a regular net to a chip global clock:

   ```
   assign_global_clock –net netname
   ```

   The following will happen during promotion of a regular signal to a global network:
   - If the net is external, the net will be driven by a CLKINT inserted automatically by compile.
   - The I/O macro will not be changed to CLKBUF macros.
   - If the net is an internal net, the net will be driven by a CLKINT inserted automatically by Compile.
2. PDC syntax to promote a net to a quadrant clock:

   ```
   assign_local_clock –net netname –type quadrant UR|UL|LR|LL
   ```

   This follows the same rule as the chip global clock network.

The following PDC command demotes the clock nets to regular nets.

```
unassign_global_clock -net netname
```

The following will happen during demotion of a global signal to regular nets:

- CLKBUF_x becomes INBUF_x; CLKINT is removed from the netlist.
- The essential global macro, such as the output of the Clock Conditioning Circuit, cannot be demoted.
- No automatic buffering will happen.

Since no automatic buffering happens when a signal is demoted, this net may have a high delay due to large fanout. This may have a negative effect on the quality of the results. Actel recommends that the automatic global demotion should only be used on small fanout nets. Use clock networks for high fanout nets to improve timing and routability.

Spine Assignment

The ProASIC3/E architecture allows the global networks to be segmented and used as clock spines. These spines, also called local clocks, enable the use of PDC or MVN to assign a signal to a spine.

PDC syntax to promote a net to a spine/local clock:

```
assign_local_clock –net netname –type [quadrant|chip] Tn|Bn|Tn:Bm
```

If the net is driven by a clock macro, Designer automatically demotes the clock net to a regular net before it is assigned to a spine. Nets driven by a PLL or CLKDLY macro cannot be assigned to a local clock.

When assigning a signal to a spine and/or a quadrant global network using PDC (pre-compile), the Designer software will legalize the shared instances. The number of shared instances to be legalized can be controlled by compile options. If these networks are created in MVN (only quadrant globals can be created), then no legalization is done (as it is post-compile). Designer does not do legalization between non-clock nets.

As an example, consider two nets, net_clk and net_reset, driving the same flip-flop. The following PDC constraints are used:

```
assign_local_clock –net net_clk –type chip T3
assign_local_clock –net net_reset –type chip T1:T2
```

During compile, Designer adds a buffer in the reset net and places it in the T1 or T2 region, and places the flip-flop in the T3 spine region (Figure 7).

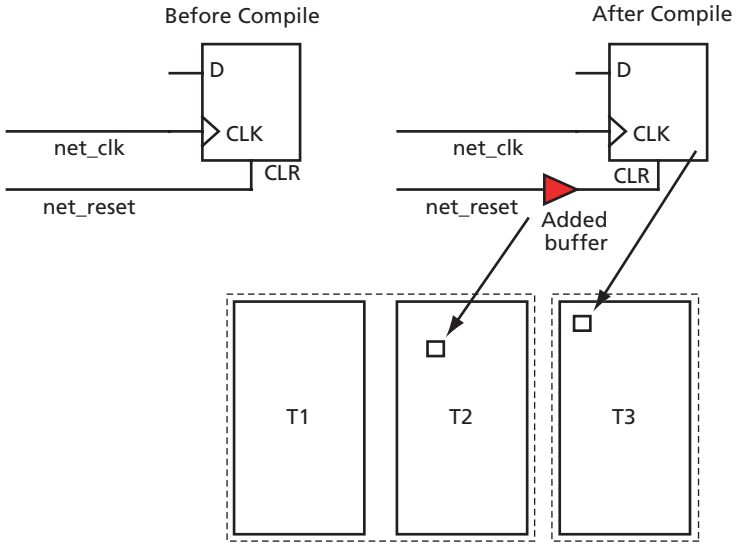


Figure 7 • **Adding a Buffer for Shared Instances**

You can control the maximum number of shared instances allowed for the legalization to take place using the Compile Option dialog box shown in Figure 8. Refer to Libero IDE/Designer online help for details on the Compile Option dialog box. A large number of shared instances most likely indicate a floorplanning problem that you should address.

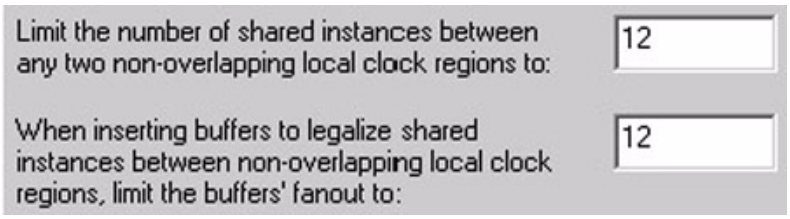


Figure 8 • **Shared Instances in the Compile Option Dialog Box**

Designer Flow for Global Assignment

To achieve the desired result, pay special attention to global management during synthesis and place-and-route. The current Synplify tool does not insert more than six global buffers in the netlist by default. Thus, the default flow will not assign any signal to the quadrant global network. However, you can use attributes in Synplify and increase the default global macro assignment in the netlist. Designer v6.2 supports automatic quadrant global assignment, which was not available in Designer v6.1. Layout will make the choice for assigning the correct signals to global. However, you can also utilize PDC and perform manual global assignment to overwrite any automatic assignment. The following step-by-step suggestions guide you in the layout of your design and help you improve timing in Designer:

1. Run Compile and check the compile report. The compile report has global information in the Device Utilization section that describes the number of chip and quadrant signals in the design. A Net Report section describes chip global nets, quadrant global nets, local clock nets, a list of nets listed by fanout, and net candidates for local clock assignment. Review this information. Note that YB or YC are counted as global only when they are used in isolation; if you use YB only and not GLB, this net is not shown in the global/quadrant nets report. Instead, it appears in the Global Utilization report.
2. If some signals have a very high fanout and are candidates for global promotion, then promote those signals to global using the Compile Options or PDC commands. Figure 9 shows the Globals Management section of the Compile Options. Select **Promote regular nets whose fanout is greater than** and input a reasonable value for fanouts.

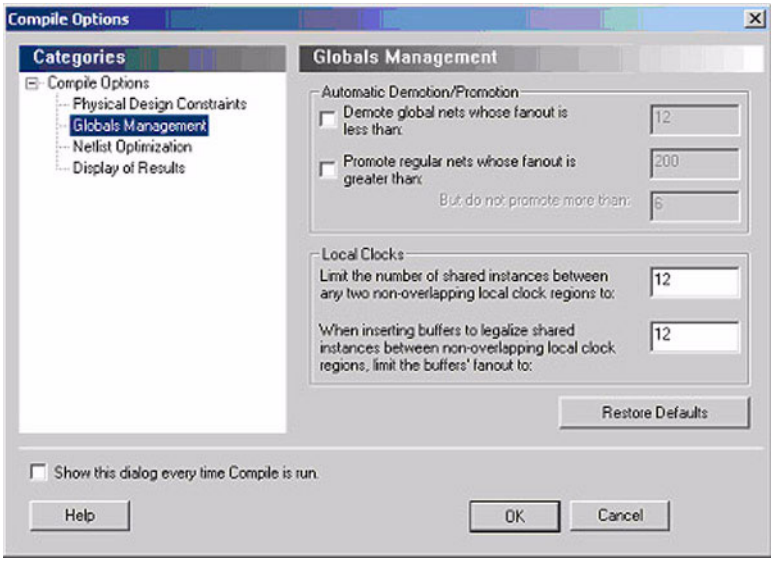


Figure 9 • **Global Management GUI in Designer**

3. Occasionally, the synthesis tool assigns a global macro to clock nets, even though the fanout is significantly less than other asynchronous signals. Select **Demote global nets whose fanout is less than** and input a reasonable value for fanouts. This frees up some global networks from the signals that have very low fanouts. This can also be done using PDC.
4. Use local clocks for the signals that do not need to go to the whole chip but should have low skew. This local clocks assignment can only be done using PDC.
5. Assign the I/O buffer using MVN if you have fixed I/O assignment. As shown in Figure 5 on page 7, there are three sets of global pins that have a hardwired connection to each global network. Do not try to put multiple CLKBUF macros in these three sets of global pins. For example, do not assign two CLKBUFs to GAA0x and GAA2x pins.
6. You must select **Commit** at the end of MVN assignment. This runs the pre-layout checker and checks the validity of global assignment.
7. Always run Compile with the **Keep existing physical constraints** option on. This would use the quadrant clock network assignment in the MVN assignment, and check if you have the desired signals on the global networks.
8. Run Layout and check the timing.

Simple Design Example

Consider a design consisting of six building blocks (shift-register) and targeted for an A3PE600-PQ208 (Figure 7 on page 12). The example design consists of two PLLs (PLL1 has GLA only, PLL2 has GLA, and GLB both), a global reset (ACLR), an enable (EN_ALL), and three external clock domains (QCLK1, QCLK2, and QCLK3) driving the different blocks of the design. Note that the PQ208 package only has two PLLs (which access the chip global network). Because of fanout, the global reset and enable signals need to be assigned to the chip global resources. There is only one free chip global for the remaining global (QCLK1, QCLK2, QCLK3). Place two of these signals to the quadrant global resource. The design example demonstrates manually assign QCLK1 and QCLK2 to the quadrant global using the PDC command.

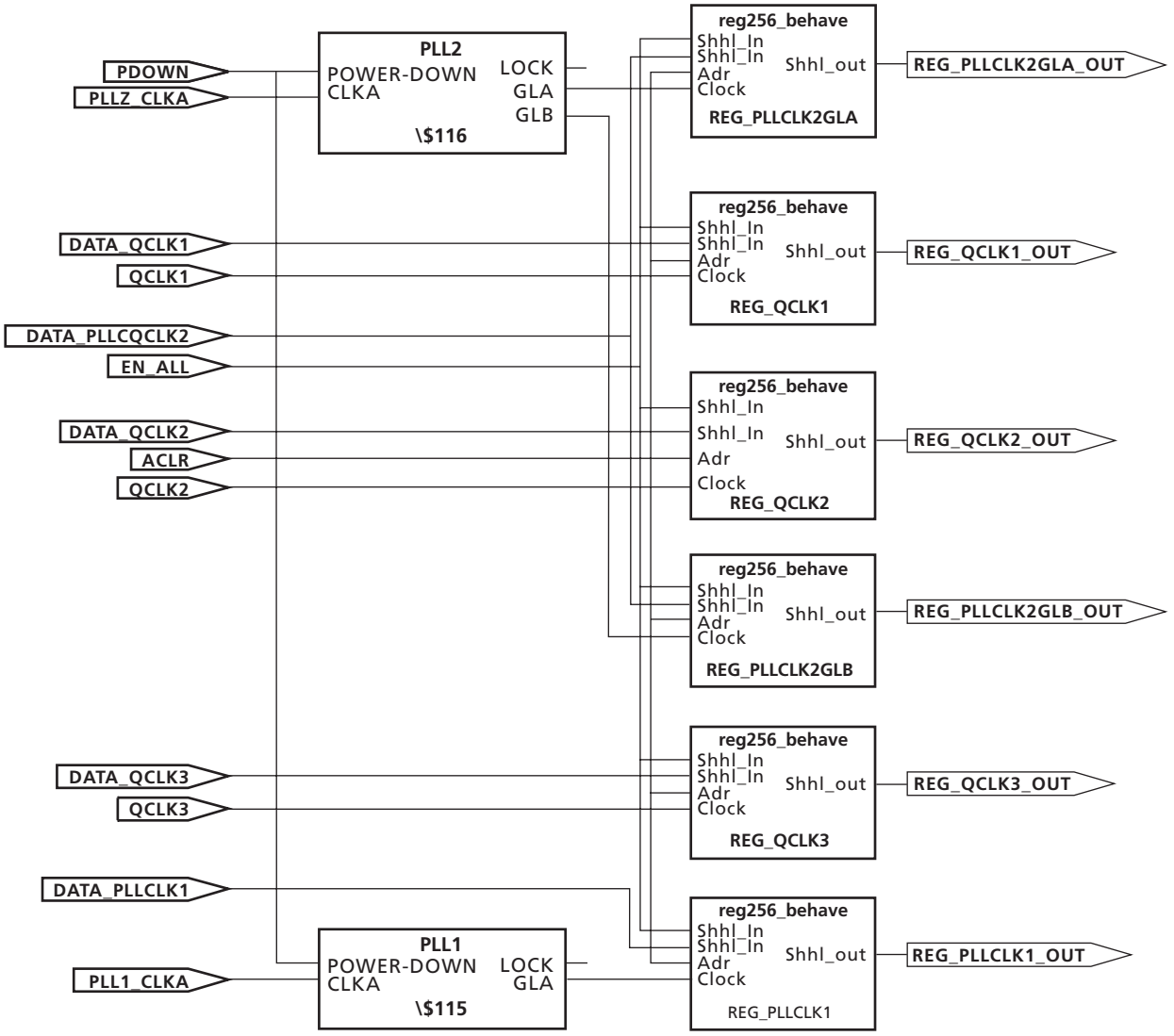


Figure 10 • **Block Diagram of the Global Management Example Design**

Step1

Run synthesis with default options. The Synplicity log shows the following device utilization:

Cell usage:

	cell count	area	count*area
DFN1E1C1	1536	2.0	3072.0
BUFF	278	1.0	278.0
INBUF	10	0.0	0.0
VCC	9	0.0	0.0
GND	9	0.0	0.0
OUTBUF	6	0.0	0.0
CLKBUF	3	0.0	0.0
PLL	2	0.0	0.0
TOTAL	1853		3350.0

Step 2

Run Compile with the **Promote regular nets whose fanout is greater than** option checked in Designer; you will see the following in the Compile report:

```
Device utilization report:
==========================

CORE               Used:   1536  Total:  13824   (11.11%)
IO (W/ clocks)     Used:     19  Total:    147   (12.93%)
Differential IO    Used:      0  Total:     65   (0.00%)
GLOBAL             Used:      8  Total:    18   (44.44%)
PLL                Used:      2  Total:    2   (100.00%)
RAM/FIFO           Used:      0  Total:    24   (0.00%)
FlashROM           Used:      0  Total:    1    (0.00%)

……….

The following nets have been assigned to a global resource:

Fanout  Type          Name
--------------------------

1536    INT_NET         Net   : EN_ALL_c
                        Driver: EN_ALL_pad_CLKINT
                        Source: AUTO PROMOTED

1536    SET/RESET_NET   Net   : ACLR_c
                        Driver: ACLR_pad_CLKINT
                        Source: AUTO PROMOTED

256     CLK_NET         Net   : QCLK1_c
                        Driver: QCLK1_pad_CLKINT
                        Source: AUTO PROMOTED

256     CLK_NET         Net   : QCLK2_c
                        Driver: QCLK2_pad_CLKINT
                        Source: AUTO PROMOTED

256     CLK_NET         Net   : QCLK3_c
                        Driver: QCLK3_pad_CLKINT
                        Source: AUTO PROMOTED

256     CLK_NET         Net   : $1N14
                        Driver: $1I5/Core
                        Source: ESSENTIAL

256     CLK_NET         Net   : $1N12
                        Driver: $1I6/Core
                        Source: ESSENTIAL

256     CLK_NET         Net   : $1N10
                        Driver: $1I6/Core
                        Source: ESSENTIAL
```

Designer will promote five more signals to global due to high fanout. There are eight signals assigned to global networks.

During Layout, Designer will assign two of the signals to quadrant global location.

Step 3 (Optional)

You can also assign the QCLK1_c and QCLK2_c nets to quadrant regions using the following PDC commands:

```
assign_local_clock -net QCLK1_c  -type quadrant UL
assign_local_clock -net QCLK2_c  -type quadrant LL
```

Step 4

Import this PDC with the netlist and run Compile again. You will see the following in the Compile report:

```
The following nets have been assigned to a global resource:
Fanout  Type          Name
---------------------------
1536    INT_NET         Net    : EN_ALL_c
                        Driver: EN_ALL_pad_CLKINT
                        Source: AUTO PROMOTED
1536    SET/RESET_NET   Net    : ACLR_c
                        Driver: ACLR_pad_CLKINT
                        Source: AUTO PROMOTED
256     CLK_NET         Net    : QCLK3_c
                        Driver: QCLK3_pad_CLKINT
                        Source: AUTO PROMOTED
256     CLK_NET         Net    : $1N14
                        Driver: $1I5/Core
                        Source: ESSENTIAL
256     CLK_NET         Net    : $1N12
                        Driver: $1I6/Core
                        Source: ESSENTIAL
256     CLK_NET         Net    : $1N10
                        Driver: $1I6/Core
                        Source: ESSENTIAL
The following nets have been assigned to a quadrant clock resource using PDC:
Fanout  Type          Name
---------------------------
256     CLK_NET         Net    : QCLK1_c
                        Driver: QCLK1_pad_CLKINT
                        Region: quadrant_UL
256     CLK_NET         Net    : QCLK2_c
                        Driver: QCLK2_pad_CLKINT
                        Region: quadrant_LL
```

Step 5

Run Layout.

Global Management in PLL Design

This section describes the legal global network connections to PLLs in the ProASIC3/E devices. Actel recommends that you use the dedicated global pins to directly drive the reference clock input of the associated PLL for reduced propagation delays and clock distortion. However, ProASIC3/E does offer the flexibility to connect other signals to reference clock inputs. Each PLL is associated with three global networks (Figure 6 on page 10). There are some limitations, such as when trying to use the global and PLL at the same time:

- If you use a PLL with only primary output, you can still use the remaining two free global networks.
- If you use three globals associated with a PLL location, you cannot use the PLL on that location.
- If the YB or YC output is used standalone, it will occupy one global, even though this signal does not go to the global network.

Using Spines of Occupied Global Networks

When a signal is assigned to a global network, the Flash switches are programmed to set the MUX select lines (explained in the "Clock Aggregation" section on page 5) to drive the spines of that network with the global net. However, if the global net is restricted from reaching into the scope of a spine, the MUX drivers of that spine are available for other high-fanout or critical signals (Figure 11).

For example, if you want to limit the CLK1_c signal to the left half of the chip and want use the right side of the same global network for CLK2_c, you can add the following PDC commands:

```
define_region -name region1 -type inclusive 0 0 34 29
assign_net_macros region1 CLK1_c
assign_local_clock -net CLK2_c -type chip B2
```

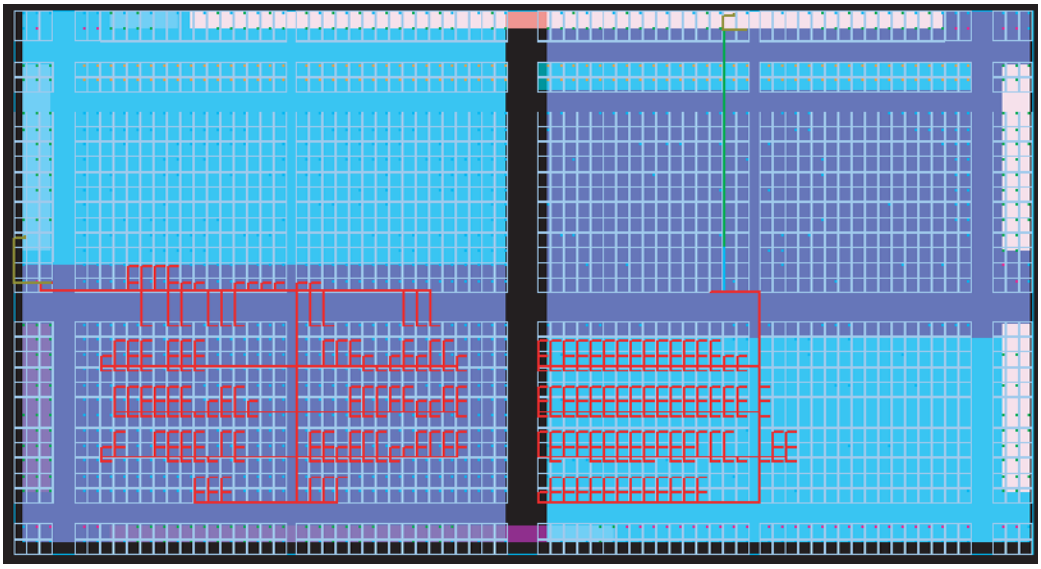


Figure 11 • **Design Example Using Spines of Occupied Global Networks**

Conclusion

ProASIC3/E devices contain 18 global networks; 6 chip global networks, and 12 quadrant global networks. These global networks can be segmented into local low-skew networks called spines. The spines provide low-skew networks for the high-fanout signals of a design. These allow you up to 252 different internal/external clocks in an A3PE2000 device. This application note described the architecture for the global network, plus guidelines and methodologies in assigning signals to globals and spines.

Related Documents

Datasheets

ProASIC3 Flash Family FPGAs

http://www.actel.com/documents/PA3_DS.pdf

ProASIC3E Flash Family FPGAs

http://www.actel.com/documents/PA3E_DS.pdf

User's Guides

ProASIC3/E Macro Library Guide

http://www.actel.com/documents/pa3_libguide.pdf

List of Changes

Previous Version	Changes in the current version 51900087-1/7.05	Page
51900087-1/3.05	Figure 2 was updated.	2
	The "Naming of Global I/Os" section was updated.	6
	The "Using Global Macros in Synplicity®" section was updated.	10
	The "Global Promotion and Demotion Using PDC" section was updated.	11
	The "Designer Flow for Global Assignment" section was updated.	13
	The "Simple Design Example" section was updated.	14
51900087-0/1.05	Table 1 was updated.	3

Note: *The part number is located on the last page of the document.*

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