Angelo Family Datasheet

Version 1.0 February 2009

Agate Logic, Inc.

The information in this document has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, Agate Logic, Inc. reserves the right to discontinue or make changes, without prior notice, to any products herein to improve reliability, function, or design. Agate Logic, Inc. advises its customers to obtain the latest version of the relevant information to verify, before placing orders, that the information being relied upon is current.

Contents

About This Datasheet

This datasheet provides comprehensive information about the Agate Logic Angelo devices.

Typographic Conventions

The following typographic conventions are used in this document.

Visual Cue	Meaning
Bold	Headings, figure and table indexes, figure titles, and table items. Example: **Figure 2.1.1 Top Level Architecture**
Italic Bold	Table titles. Example: ***Table 1.1 Angelo Features***
Helvetica	Text and figures in tables. Example: Core Voltage
Arial	Note reminders. Example: Notes for above tables
Palatino Linotype in italic	Reference to sections within this document. Example: *Clock Bundle Control Logic*
●	A list of items whose sequence is not important
(1), (2)……	Numbers in a note instruction
√	A procedure that consists of one step only.

Additional Resources

To find additional documentation about Agate Logic products, please see the Agate Logic website at:

www.agatelogic.com.cn

To find the up-to-date information about Agate Logic products, please see the Agate Logic website at:

www.agatelogic.com.cn

Technical Support Assistance

Tel: +86 10 82150100

E-mail: support@agatelogic.com

Website: www.agatelogic.com.cn

Introduction

Section 1 | Datasheet

This document provides designers with the datasheet specifications for one member of the Agate Logic Configurable Logic Device family: Angelo. These sections contain feature definitions of the ordering information, function descriptions, configuration, DC & switching characteristics, pinout information, etc.

1.1 Overview

Agate Logic Angelo is constructed on a brand-new architecture, based on a leading-edge 0.13 micron process technology. With the unique combination of the soft IP cores for 4096 Field Programmable logic cells (LCs), 8 embedded memory blocks with 9K bits (EMB9Ks), and 2 phase-locked loops (PLLs), Agate Logic Angelo provides you better solutions.

The architecture of Agate Logic Angelo is optimized, giving 16 global clocks and 2 PLL for clock management, JTAG port, SPI Port and Bootstrap & Reset Unit for convenient configuration and reset, EMB9K to address on-chip memory demand, and TQFP100/ LQFP144/ PQFP208 packages to provide the customers with great flexibility and convenience.

1.2 Features

Angelo devices offer the following features:

- Field-programmable through internal DPRAM-based FPGA fabric
- Capacity to accommodate the unique designs
  - ✓ Up to 4096 Field Programmable LCs
  - ✓ Each LC includes one 4-input LUT and register
  - ✓ Up to 72K bits of configurable and pipeline-able true dual-port RAM
  - ✓ Up to two PLLs per device Frequency Synthesis, Deskew, Phase-shift
  - ✓ Up to 16 low skew global clocks and reset trees
- Flexible I/O options
  - ✓ Software Programmable I/Os: 3.3V LVCMOS/LVTTL, with programmable drive strength of 2 mA/4 mA/8 mA/12 mA/16 mA
- Internal Nonvolatile Memory for security: protect customer's design
- Support customer for multiple intellectual property (IP) cores
- Temperature: commerce and industry grades

- ESD 4000V HBM
- Power on reset
- Routing architecture delivers predictable timing and high utilization
- Manufactured in leading-edge 0.13 micron process for maximum performance and density
- Package options
  - ✓ 100 pin TQFP with internal flash, 16 x 16 mm package size 56 user I/Os
  - ✓ 144 pin LQFP with internal flash, 22 x 22 mm package size 96 user I/Os
  - ✓ 208 pin PQFP with internal flash, 30.6 x 30.6 mm package size 156 user I/Os
  - ✓ 208 pin PQFP without internal flash, 30.6 x 30.6 mm package size 153 user I/Os

Table 1.1 summarizes the features of the Angelo devices.

Table 1.1 Angelo Features

Feature	Value
Core Voltage	1.2 V
I/O Voltage	3.3 V
Process Technology	130-nm
LC	4,096
User I/O Pin	Up to 156
EMB9K	8
PLL	2
I/O Standards Support	LVCMOS/LVTTL 3.3V

1.3 Supported Packages

Angelo devices provide four kinds of packages including TQFP100 with internal flash, LQFP144 with internal flash, PQFP208 with internal flash, and PQFP208 without internal flash. See the detailed pinout information in *Pinout Information* section

Integrating 4096 Field Programmable LUT/Register Logic Cells, a large block of RAM and so on, the Agate Logic Angelo is optimized for low-cost, more flexible industrial control applications. This section provides comprehensive information about the functionalities of Agate Angelo devices.

2.1 Architecture Overview

Figure 2.1 Top Level Architecture shows the top level architecture for Angelo. The Angelo device is constructed from four basic units, including Basic Logic Block (BLB), I/O Block (IOB), EMB9K and PLL.

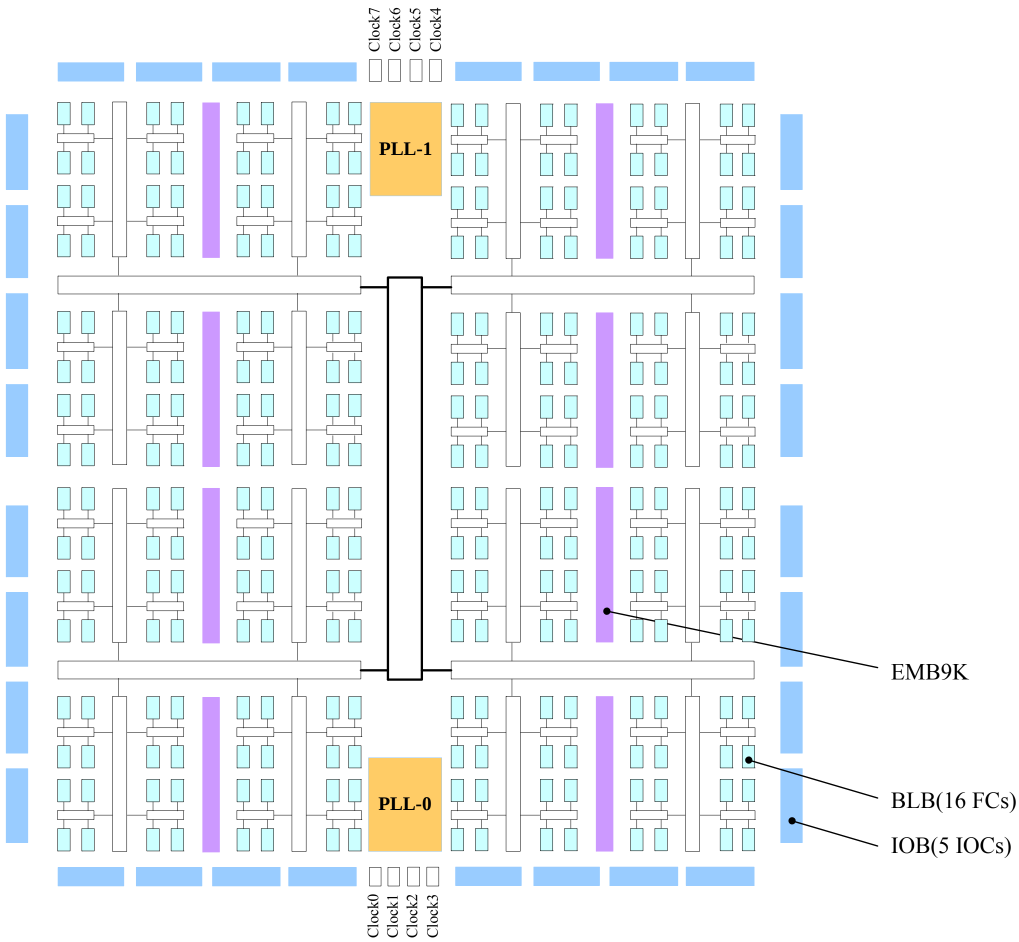


Figure 2.1 Top Level Architecture

The BLB contains 16 logic cells. There are 256 BLBs in Angelo device, which are connected together using a hybrid routing architecture of Quad-Tree hierarchical architecture and Crosslink planar architecture. Under the Quad-Tree arch, 4 BLB is grouped into level-2 block. In a same way, 4 of this level-2 block is grouped into level-3 block. Since there are 4096 logic cells or 256 BLBs, so there are 4 levels in Angelo device.

The IOB contains 5 I/O cells. Each side there are 8 IOBs, so there can be up to 160 (8x4x5=160) User I/Os totally. For different package, we bound out part of these 160 user I/Os. The IOB is connected to logic array using the Crosslink planar architecture.

The EMB9K contains 9K-bit SRAM. There are 8 EMB9Ks in Angelo devices and there are distributed equally into the logic array. Each EMB9K can be configured into different depth and width ranged from 9Kx1 to 256x36. The EMB9K is connected to logic array using the Crosslink planar architecture.

The PLL block can be used for clock multiplication, division and phase shift. There are 2 PLLs in Angelo devices. There are 4 dedicated clock pads attached to each PLL as the clock source. Each PLL block generate 8 global clocks and there can be up to 16 global clocks in Angelo devices.

Table 2.1 Angelo Performance

Applications	Resources Used	Performance	
	LCs	Frequency	Units
MUX16-1	10	303	MHz
MUX32-1	21	135.4	MHz
adder16	16	317	MHz
adder32	32	194	MHz
adder64	64	123.6	MHz
counter8	8	350	MHz
counter16	16	350	MHz
counter32	32	280	MHz

Note:

(1) The data above are samples.

(2) Because of the PLL limitation, the max frequency of counter8 and counter16 is 350MHz.

2.2 Logic Cell & Carry Chain

Logic cell is the smallest unit in the Field Programmable (FP) block, providing beneficial features as:

- A 4-input LUT that can implement any function of four variables
- The CarryGen function can be used for adder/subtracter
- The Nor chain and WLUT chain can extend the function of LUT

- A programmable register
- Support register feedback to LUT

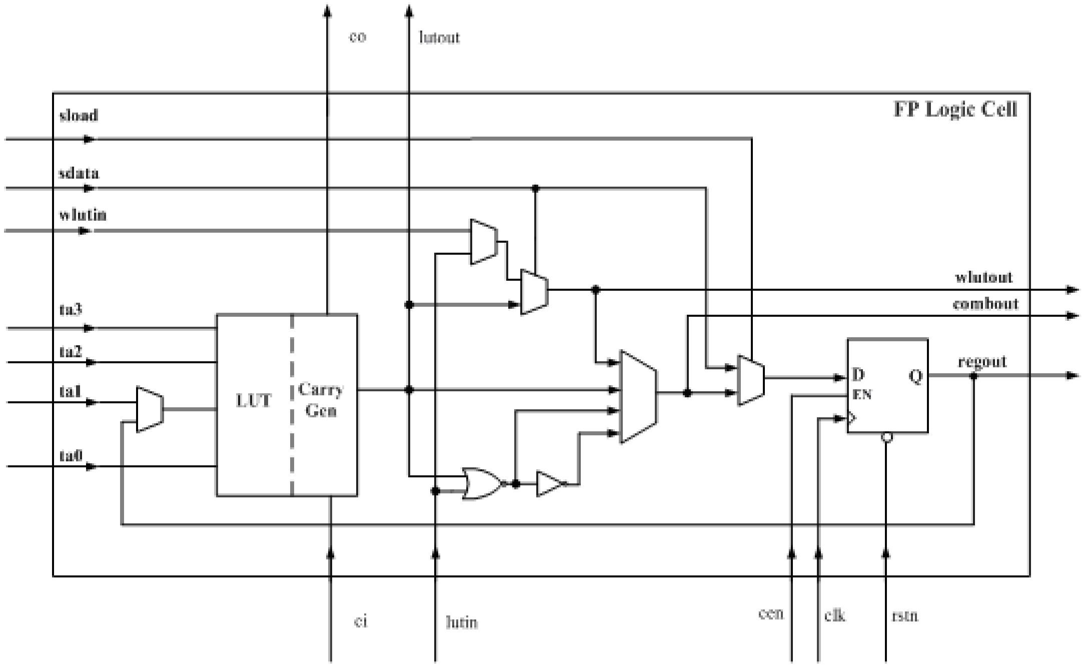


Figure 2.2.1 Logic Cell

The carry chains are cascaded together through the carry chain input (CI) and carry chain output (CO) signals. The Nor chain are cascaded together through lutin and lutout; The WLUT chain are cascaded together through wlutin and wlutout. **Figure 2.2.2** shows the cascading of LCs.

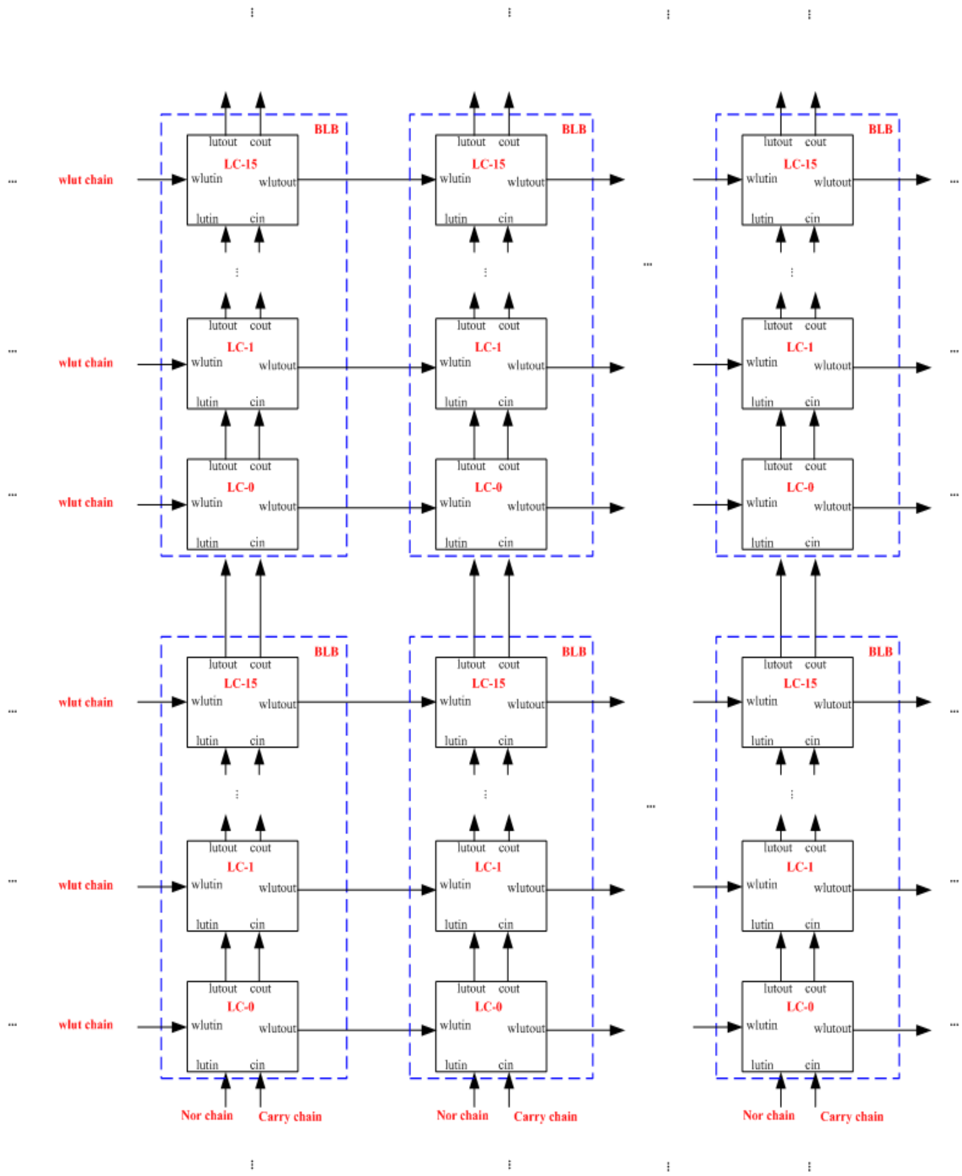


Figure 2.2.2 Carry Chain, Nor chain and WLUT chain

2.3 Routing Resources

2.3.1 Hierarchical logic box and hierarchical switch box

Routing resource is composed of a Quad-Tree style routing MUX architecture and crosslink routing architecture. The hierarchical Quad-Tree routing resource provide sufficient routing path for all BLB, wherein BLB is the smallest node of the tree and contains 16 LCs. The Crosslink routing resource provide fast routing path between BLBs.

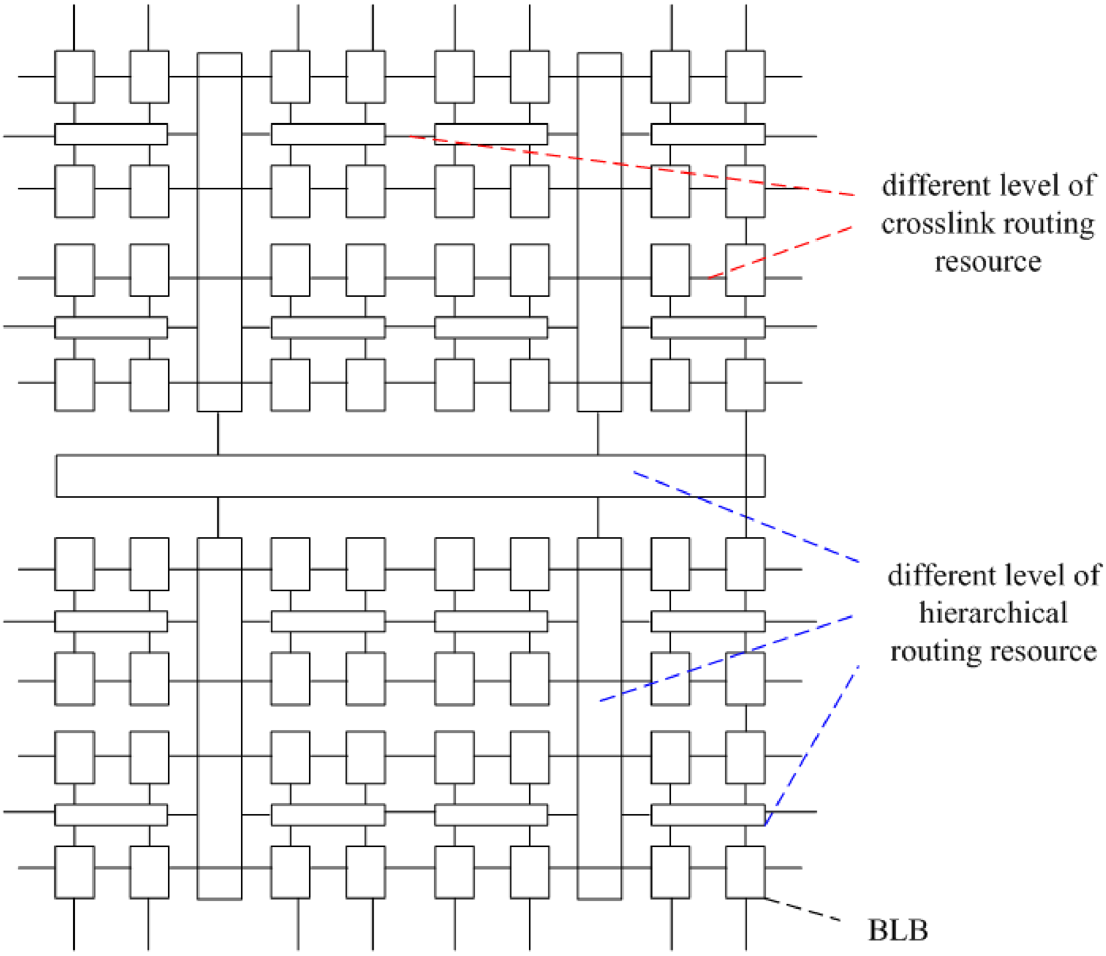


Figure 2.3.1 Diagram of Routing Resource

BLB

BLB is composed of 16 LCs and the BLB_ctrl block. BLB_ctrl provides the clk, cen, rstn and sload signal for all the 16 cells.

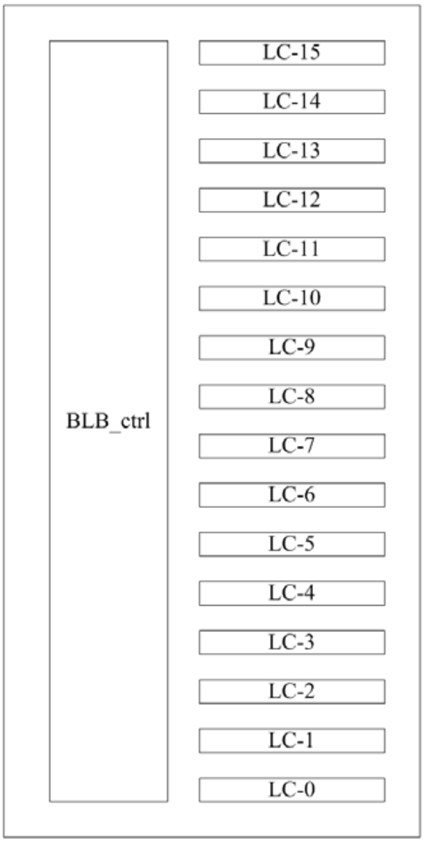


Figure 2.3.2 BLB Structure

2.4 Block RAM

The Angelo consists of the type of EMB9K to address on-chip memory needs. The EMB9K is a dual-port SRAM that can implement various types of memory with or without parity, including true dual-port, simple dual-port and single-port RAM. The memory blocks can be used to provide memory functions such as RAM and FIFO. There are 8 blocks of EMB9K Angelo devices.

2.4.1 Features

The EMB blocks support the following features:

- 9,216 RAM bits
- True dual-port mode
- Simple dual-port mode
- Single-port mode
- FIFO Buffers
- Mixed clock mode

- Byte enable
- Parity bit
- Support the following width configurations: 9k × 1, 8K × 1, 4k × 2, 2k × 4, 1k × 8, 1k × 9, 512 × 16, 512 × 18, 256 × 32, 256 × 36

2.4.2 Memory Modes

The EMB9K includes input registers that synchronize writes. EMB9K offers a true dual-port mode to support any combination of two-port operations: two read ports, two write ports, or one read and one write at two different clock frequencies. **Figure 2.4.1** shows true dual-port memory mode.

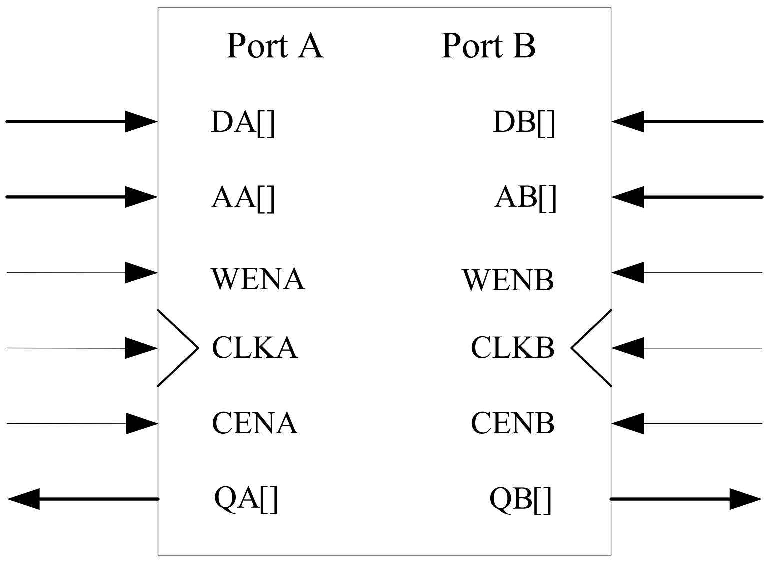


Figure 2.4.1 True Dual-port Memory Mode

The following tables summarize the ports and the function of true dual-port memory mode.

Table 2.4.1 shows the pin descriptions of true dual-port memory mode.

Table 2.4.1 Pin Descriptions of True Dual-port Memory Mode		
Name	**Type**	**Description**
AA (B)	Input	Port A (B) Address.
DA (B)	Input	Port A (B) Data Input.
QA (B)	Output	Port A (B) Data Output.
WENA (B)	Input	Port A (B) Write Enable. Data is written into the dual-port SRAM upon the rising edge of the clock when both WENA (B) and CENA (B) are high.
CENA (B)	Input	Port A (B) Enable. When CENA (B) is high and WENA (B) is low, data read from the dual-port SRAM address AA (B) is available upon the next rising edge of CLKA (B). If CENA (B) is low, QA (B) retains its value.
CLKA (B)	Input	Port A (B) Clock.

Table 2.4.2 shows a logic table of true dual-port mode function.

Table 2.4.2 Logic Table of True Dual-port Memory Mode Function				
Inputs			**Outputs**	
CENA (B)	**WENA (B)**	**CLK**	**Status**	**QA (B)**
0	X	X	HOLD	Data stored in the memory is retained.
1	0	↑	READ	Data is read from the memory location specified by the address bus.
1	1	↑	WRITE	DA (B)

Read and write operation waveforms of true dual-port memory mode are shown in **Figure 2.4.2**.

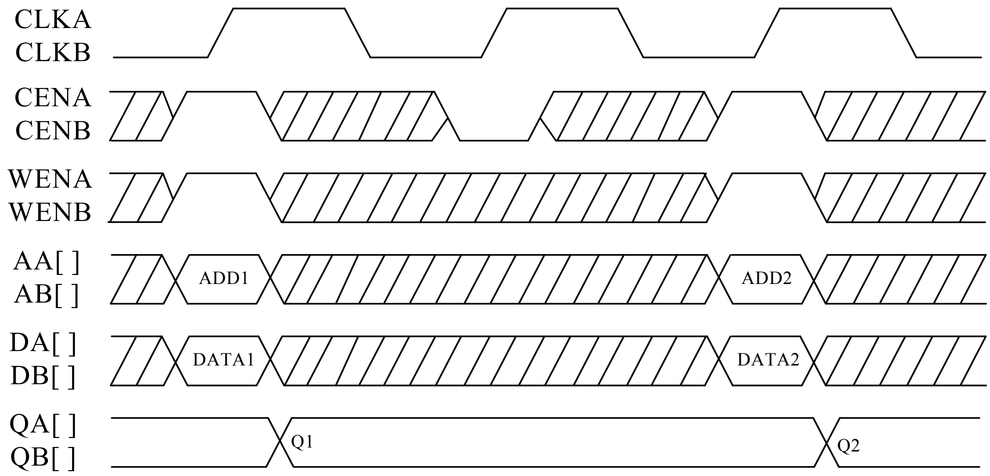


Figure 2.4.2 True Dual-Port Memory Read-Write Waveform

Besides, the EMB9K memory also supports simple dual-port memory mode.

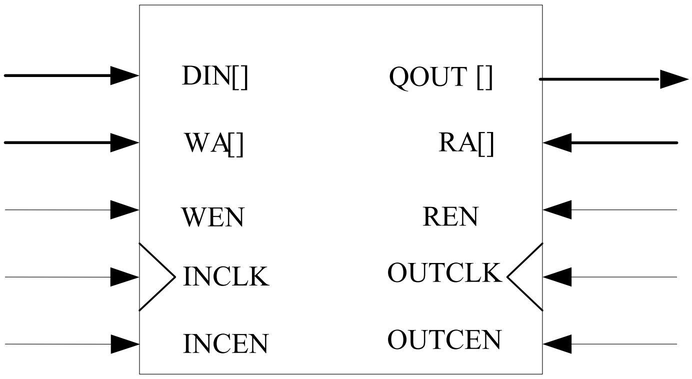


Figure 2.4.3 Simple dual-port memory mode

Table 2.4.3 Pin Descriptions of Simple Dual-port Memory Mode		
Name	**Type**	**Description**
DIN	Input	Data Input.
WA	Input	Write Address.
WEN	Input	Write Enable.
INCLK	Input	Input Clock.
INCEN	Input	Input Clock Enable.
QOUT	Input	Port A (B) Clock.
RA	Output	Read Address.
REN	Input	Read Enable.
OUTCLK	Input	Output Clock.
OUTCEN	Input	Output Clock Enable.

Read and write operation waveforms of simple dual-port memory mode are shown in **Figure 2.4.4.**

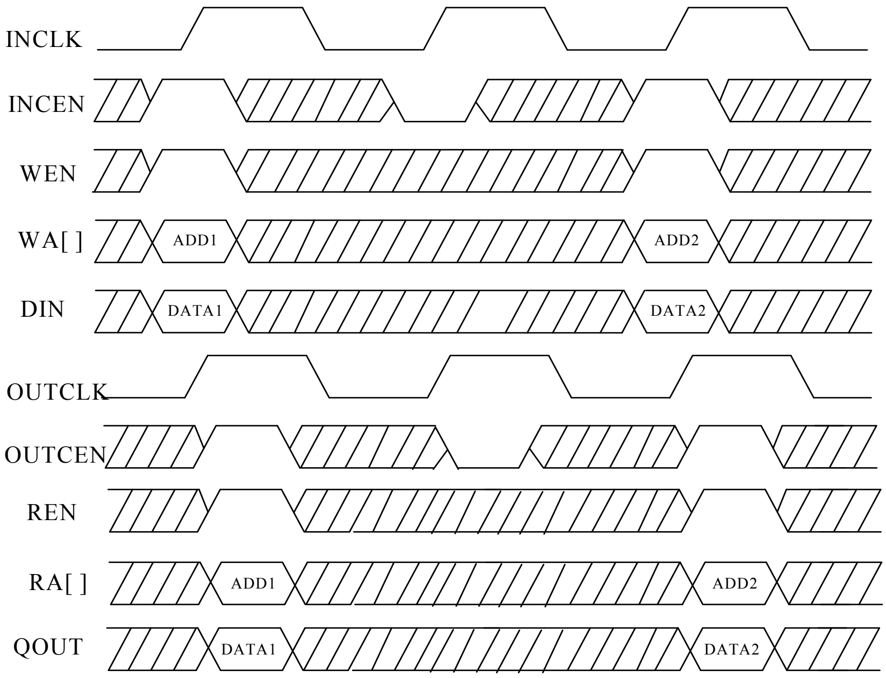


Figure 2.4.4 Simple Dual-Port Memory Read-Write Waveform

In addition to true dual-port memory mode, the EMB9K memory blocks support single-port memory mode. **Figure 2.4.5** shows this mode of Angelo EMB9K memory blocks.

Figure 2.4.5 Single-port Memory Mode

Figure 2.4.6 gives the waveforms of read and write operations in this mode.

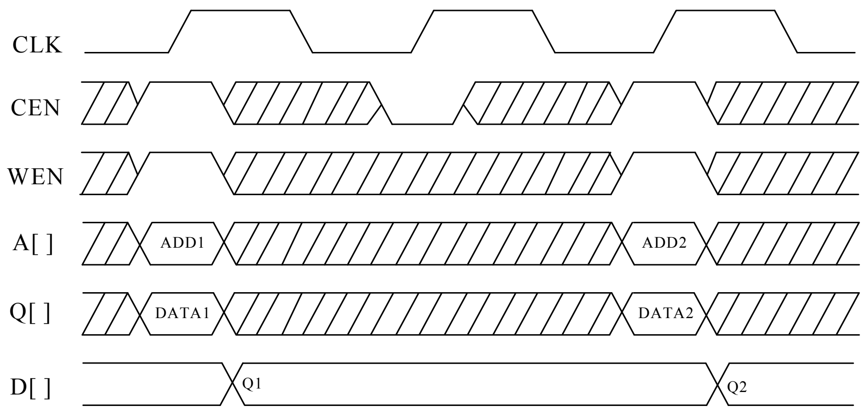


Figure 2.4.6 Single-Port Memory Read-Write Waveform

The memory blocks also enable mixed-width data ports for reading and writing to the EMB9K ports in dual-port EMB9K configuration. For example, the memory block can be written in × 1 mode at port A and read out in × 16 mode from port B.

2.4.3 Conflict Avoidance

For dual-port memory modes, both ports can access any memory address at any time. When both ports access the same address, the read and write behaviour should observe certain clock timing restrictions. These restrictions are adaptable to both synchronous and asynchronous clock.

Figures 2.4.7, **Figure 2.4.8**, and **Figure 2.4.9** illustrate the clock timings that may cause conflict in read and write operations with dual-port memory modes.

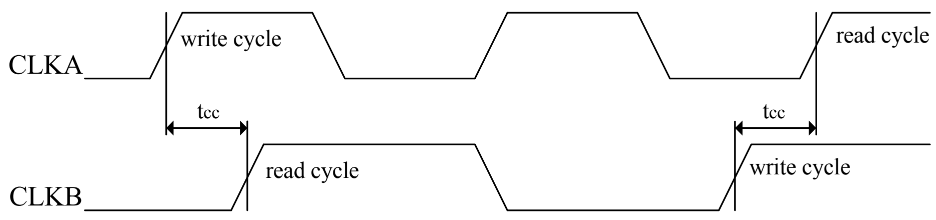


Figure 2.4.7 Dual-port memory Write-Read Clock Timing

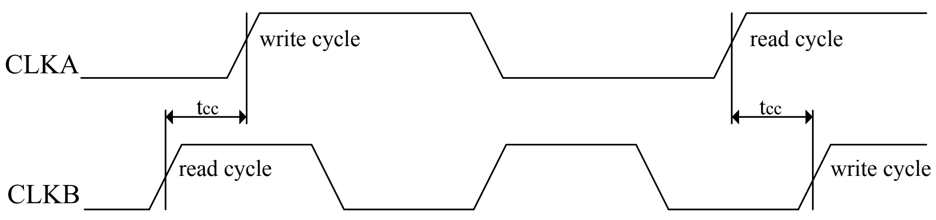


Figure 2.4.8 Dual-port memory Read-Write Clock Timing

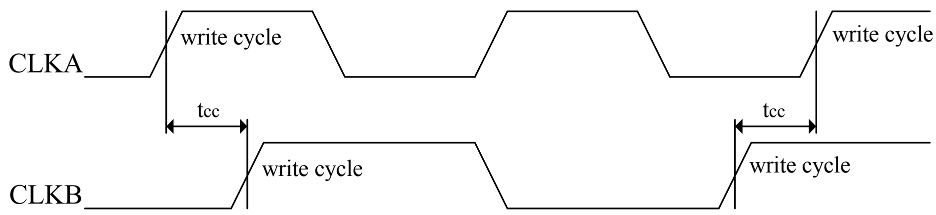


Figure 2.4.9 Dual-port memory Write-Write Clock Timing

Note for **Figure 2.4.6** to **Figure 2.4.9**:

(1) tcc means clock collision. The Min value of it is 0.748ns based on the conditions of temperature = 25 ^{o}C, power supply = 1.2 V.

Table 2.4.4 shows read and write behaviour during clock conflicts, when both ports access the same address.

Table 2.4.4 Dual-port Memory Read and Write Behaviour when accessing the same address

Action	**Condition**	**Behaviour**
Write from one port then read from the other port	t_{cc} is satisfied (see **Figure 2.4.5**)	Write OK D-to-Q write through OK Read (new data) OK
	t_{cc} is not satisfied (see **Figure 2.4.5**)	Write fails D-to-Q write through OK Read fails
Read from one port then write from the other port	t_{cc} is satisfied (see **Figure 2.4.6**)	Write OK D-to-Q write through OK Read (old data) OK
	t_{cc} is not satisfied (see **Figure 2.4.6**)	Write fails D-to-Q write through OK Read fails
Write from one port then write from the other port	t_{cc} is satisfied (see **Figure 2.4.7**)	Both writes OK (second write overwrites first write) D-to-Q write through OK
	t_{cc} is not satisfied (see **Figure 2.4.7**)	Both writes fail D-to-Q write through OK
Read from one port then read from the other port	No restriction	Both reads OK

2.4.4 Parity Bit Support

The EMB9K blocks support a parity bit for each byte. The parity bit, along with internal LC, can implement parity checking for error detection to ensure data integrity. You can also use parity-sized data words to store user-specified control bits. Byte enables are also available for data input masking when writing operations.

2.4.5 Memory Configuration Sizes

The memory address depths and output widths can be configured as **Table 2.4.5, Table 2.4.6,** and **Table 2.4.7**. Mixed-width configurations are also possible, allowing different read and write widths.

Table 2.4.5 EMB9K Block Configurations (Single Port)									
Port A									
8K×1	4K×2	2K×4	1K×8	512×16	256×32	9 k×1	1K×9	512×18	256 ×36

Table 2.4.6 EMB9K Block Configurations (Simple Dual-Port)										
Port A	Port B									
	8K×1	4K×2	2K×4	1K×8	512×16	256×32	9 k×1	1K×9	512×18	256×36
8K × 1	√	√	√	√	√	√				
4K × 2	√	√	√	√	√	√				
2K × 4	√	√	√	√	√	√				
1K × 8	√	√	√	√	√	√				
512 × 16	√	√	√	√	√	√				
256 × 32	√	√	√	√	√	√				
9K × 1							√			
1K × 9								√	√	√
512 × 18								√	√	√
256 × 36								√	√	√

Table 2.4.7 EMB9K Block Configurations (True Dual-Port)								
Port A	Port B							
	8K × 1	4K × 2	2K × 4	1K × 8	512 × 16	9 k × 1	1K × 9	512 × 18
8K × 1	√	√	√	√	√			
4K × 2	√	√	√	√	√			
2K × 4	√	√	√	√	√			
1K × 8	√	√	√	√	√			
512 × 16	√	√	√	√	√			
9K × 1						√		
1K × 9							√	√
512 × 18							√	√

2.4.6 Byte Enables

EMB9K blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value.

Table 2.4.8 summarizes byte selection.

Table 2.4.8 Byte Enable for EMB9K Blocks

wena[3..0]	din[15..0]	din[17..0]	din[31..0]	din[35..0]
[0] = 0	[7..0]	[8..0]	[7..0]	[8..0]
[1] = 0	[15..8]	[17..9]	[15..8]	[17..9]
[2] = 0	–	–	[23..16]	[26..18]
[3] = 0	–	–	[31..24]	[35..27]

2.5 Global Clock Network and PLL

Angelo devices offer up to 16 global clocks and 2 PLLs to provide precision for time management.

2.5.1 Global Clock Network

There are 16 global clocks, which can be driven by dedicated clock pins, PLL outputs, and LCs. Angelo devices provide up to 8 dedicated clock pins.

Global clock network provides clock for FP, Internal DPRAMs, and IOCs. Global clock can be of clock control signal for FP, such as clock signal and reset signal of FP register. At the same time, global clock, asynchronous reset signal, and clock enable signal also can be driven by FP internal logic.

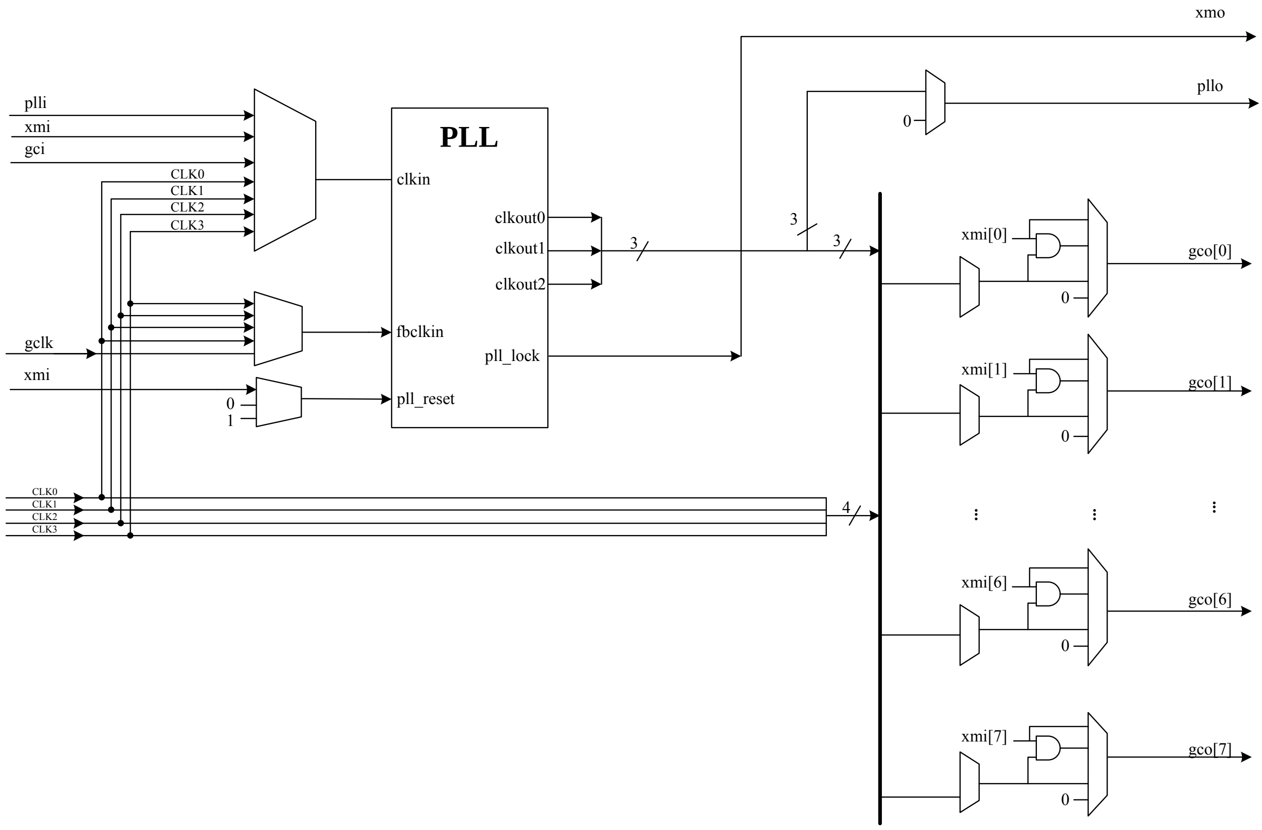


Figure 2.5.1 Global Clock Controller

Table 2.5.1 gives the detailed information of PLL signal connection relationship for Angelo.

Table 2.5.1 Signal connection of PLL

Signal	Source / Destination
plli	From the other PLL to cascade the PLLs together
xmi	From FP core
gci	From the other PLL to provide source signals for clkin
CLK[3:0]	From dedicated clock pins
gclk[15:0]	From Global Clock Network, eight bits from gco[7:0], and the other eight bits from gco[15:8]
pllo	To the other PLL to cascade the PLLs together
xmo	To FP core
gco[7:0]	To Global Clock Network

2.5.2 Global Clock for I/O

Angelo provides four I/O Banks: BANK1 to BANK4. Each bank includes 8 IOBs, each IOB contains 5 IOCs, and all the clocks are from global clock network shown as **Figure 2.5.2**:

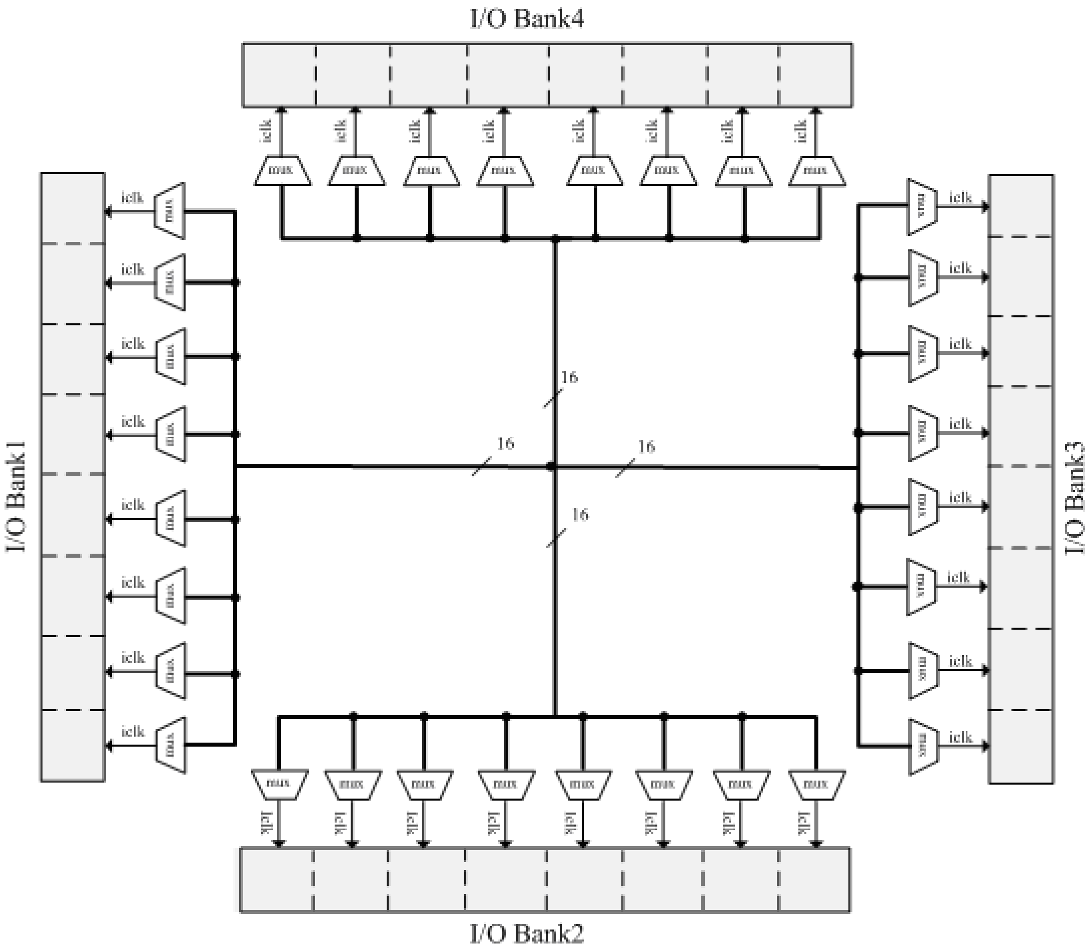


Figure 2.5.2 Clock for I/O

2.5.3 Global Clock for Internal EMB9K

There are 8 internal EMB9Ks in Angelo devices. Each EMB9K has a different clock domain. Diagram of clock for internal memory is shown as **Figure 2.5.3**.

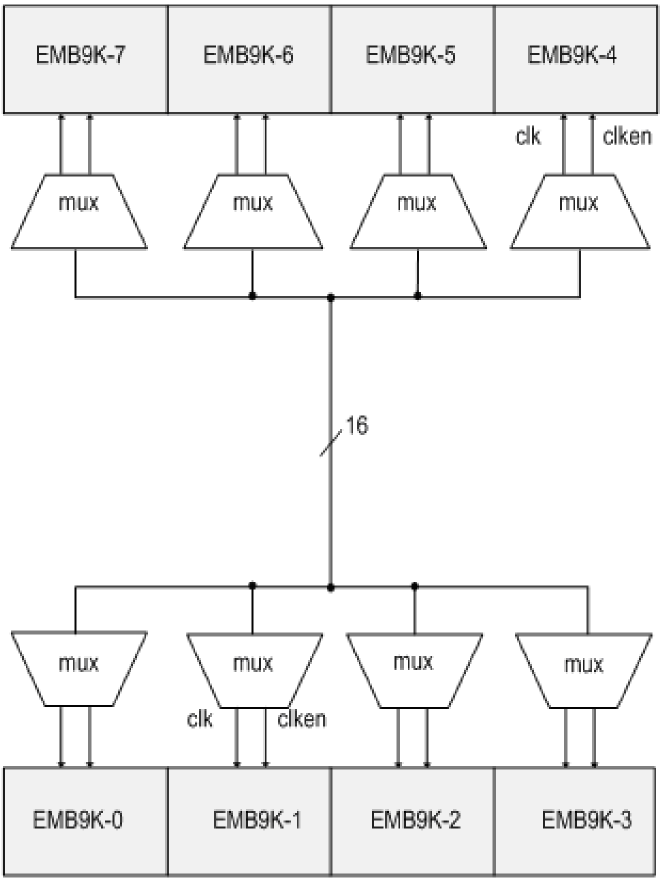


Figure 2.5.3 Clock for EMB9K

2.5.4 PLLs

Angelo PLLs provide general-purpose clocks with clock multiplication and division. Angelo device contains two PLLs.

The PLLs in Angelo devices provide the following features:

- Support of Clock Bypass Mode;
- Support of Power-down mode, realizing minimum power consumption;
- Clock multiplication and division: include reference division counter (N), multiplication counter (M) and post-scale counters(C0,C1, C2);
- Optional phase shift function: 1/10, 1/20, 1/40, 1/80, 1/160, 1/320 shift output;
- Internal and board level deskew function for system synchronization;

- Up to three different post-scale counters for each PLL;
- Lock detection output;

Table 2.5.2 shows the PLL features in Angelo.

Table 2.5.2 PLL Specification		
Parameter		**Value**
Input reference frequency range		5MHz - 350MHz
VCO output frequency range		320MHz - 800MHz
PFD input frequency range		5MHz - 350MHz
Output frequency range	Without phase shift option	10 MHz - 350 MHz
	Of 10 output phase step	320 MHz - 350 MHz
	Of 20 output phase step	160 MHz - 350 MHz
	Of 40 output phase steps	80 MHz - 200 MHz
	Of 80 output phase steps	40 MHz - 100 MHz
	Of 160 output phase steps	20 MHz - 50 MHz
	Of 320 output phase steps	10 MHz - 25 MHz
Output Duty Cycle		50% ± 16.7%
Range of counter N		2- 32
Range of counter M		1- 512
Range of counter C		1- 32
Power Consumption	Deskew with phase shift mode, 3 outputs at 350 MHz	12 mA
	Normal mode	7.5 mA
	Powerdown mode	1 mA
Operation voltage range		1.2 V ± 10%

Figure 2.5.4 shows the signal connection of Angelo PLL.

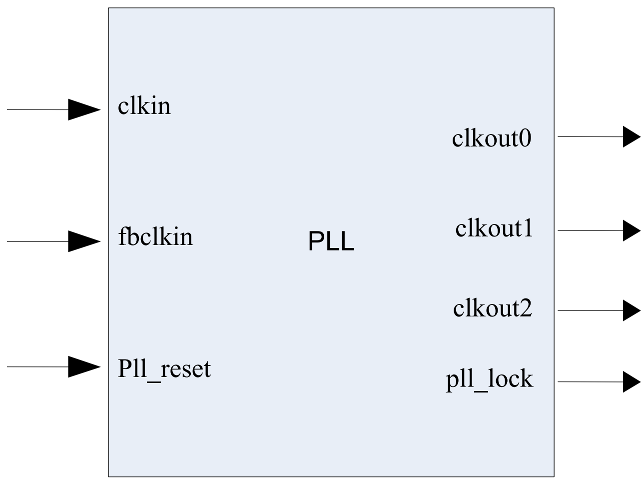


Figure 2.5.4 PLL Interface

Table 2.5.3 shows the detail information of PLL interface. For the device with 8 clock pins, CLK0/1/2/3 drive PLL0; while CLK4/5/6/7 drive PLL1.For the device with 4 clock pins, CLK0/1 drive PLL0; while CLK2/3 drive PLL1.

Table 2.5.3 Port Definition of PLL

Name	Type	Width	Description
clkin	Input	1	Reference clock input.
fbclkin	Input	1	Feedback clock input, used in deskew mode.
pll_reset	Input	1	PLL reset signal. High active. When reset, all outputs are low.
clkout0	Output	1	Main clock output.
clkout1	Output	1	First shifted phase clock output. Can run at different frequency in synthesize mode.
clkout2	Output	1	Second shifted phase clock output. Can run at different frequency in synthesize mode.
pll_lock	Output	1	Lock status output. High active.

2.5.5 Clock Multiplication and Division

Figure 2.5.5 is the schematic diagram of Angelo PLL.

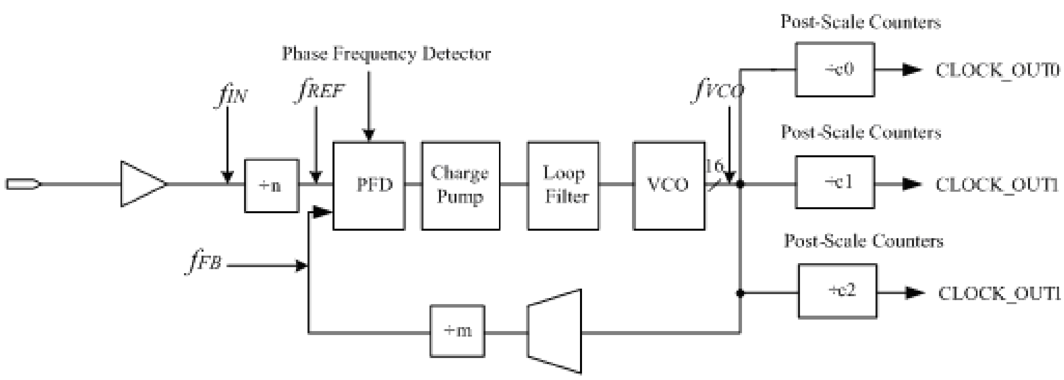


Figure 2.5.5 Angelo PLL

$$\mathbf{f_{REF} = f_{IN} / n;}$$

$$\mathbf{f_{VCO} = f_{REF} * m = f_{IN} * (m / n)}$$

$$\mathbf{f_{FB} = f_{VCO} / m;}$$

$$\mathbf{f_{CLOCK\_OUT0} = f_{VCO} / c0 = f_{IN} * (m / (n * c0))}$$

$$\mathbf{f_{CLOCK\_OUT1} = f_{VCO} / c1 = f_{IN} * (m / (n * c1))}$$

$$\mathbf{f_{CLOCK\_OUT2} = f_{VCO} / c2 = f_{IN} * (m / (n * c2))}$$

Angelo PLL provides clock synthesis for three PLL output ports, all using m/ (n x o) scaling factors. The input clock is divided by a reference divider, *n*, and is then multiplied by the *m* feedback factor. The control loop drives the VCO to match f_{IN} ×

(*m*/*n*). Then the port0 and port1 have a post-scale counter to divide down the high-frequency VCO. The frequency of port0, port1 and port2 is divided by a post-scale divider, c.

PLL has one reference divider, *n*, that can range in value from 2 to 32. PLL also has one multiply divider, *m*, which can range in value from 1 to 512. The pose-scale divider has a value range from 1 to 32.

2.6 I/O Capabilities

2.6.1 Features

Angelo IOCs support many features including:

- LVCMOS/LVTTL input and output
- Joint Test Action Group (JTAG) Boundary-Scan Test (BST) support
- Output drive strength control
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable pull-down resistor
- Asynchronous input/output
- Synchronous input/output aligned with positive/negative clock edge

Angelo device IOCs contains a bidirectional I/O buffer and three registers for complete internal bidirectional single or dual data rate transfer.

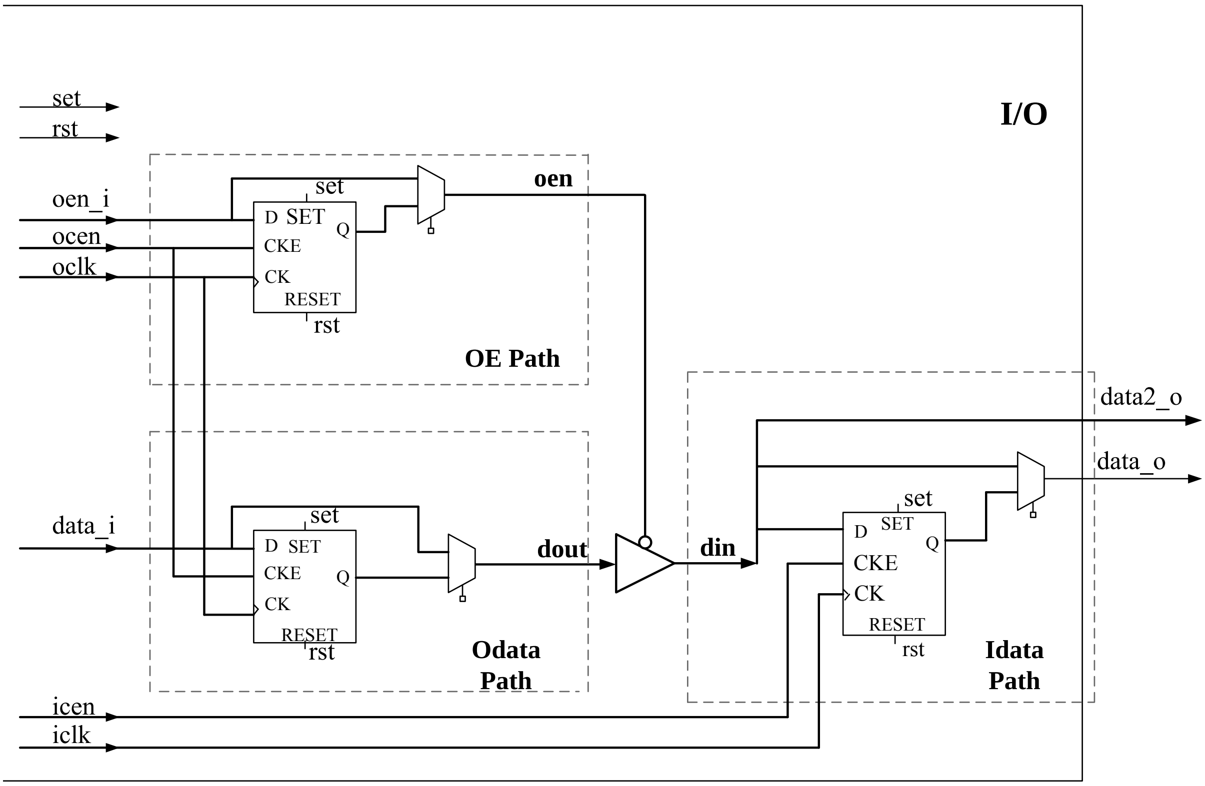


Figure 2.6 Angelo I/O Structure

2.6.2 Programmable Drive Strength

The output buffer for each Angelo device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL and LVCMOS standards have several levels of drive strength that you can control. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2.6 shows the possible settings for the I/O standards with drive strength control.

Table 2.6 Drive Strength and Maximum Output Clock Toggle Rate on Angelo Devices

I/O Standard	Driving strength	Maximum Output Clock Toggle Rate (MHz)
LVTTL/LVCMOS (3.3 V)	2mA	160
	4mA	180
	8mA	260
	12mA	280
	16mA	300

2.6.3 Slew Rate Control

Each I/O output buffer has a control bit to control the switching edge rate. This control bit can be individually programmed to either 0 (default) or 1. A 0 value means fast slew rate and a 1 value means slow slew rate.

Each I/O has a control bit. This output slew-rate control can be individually configured. This configuration affects the rising edge and descending edge of output signal. Both rising edge and descending edge of slew rate can be controlled by adjusting driving-strength.

Each user I/O has an individually configured pull-up resistor. This resistor will drag the I/O output to VDDIO. The value of this resistor is between 60-90k ohms. Each user I/O also has an individually configured pull-down resistor. This resistor will drag the I/O output to 0. The value of this resistor is between 60-90k ohms.

2.6.4 Bus Hold

Each Angelo device user I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls un-driven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than VCCIO to prevent overdriving signals.

If the bus-hold feature is enabled, the device cannot use the programmable pull-up option. Bus hold circuitry is not available on dedicated clock pins.

The bus-hold circuitry is only active after configuration. After you enter the user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

2.7 Power-On Reset Circuitry

Angelo devices have internal Power-On Reset (POR) circuits to monitor VCCINT and VCCIO voltage levels during power-up. The POR circuit keeps the device in reset state until VCCINT and VCCIO reach the trigger point. The POR circuit of Angelo device does not monitor the VCCINT and VCCIO voltage levels after the device enters into user mode. In the user mode, POR circuit can accept external reset signal and drag the chip into reset stage until this signal was released.

Configuration

3.1 Configuration Overview

The LCs of the Angelo devices use SRAM cells to store configuration data. Since SRAM is volatile, configuration data must be downloaded to device each time the device powers up. You can download configuration data to Angelo devices using the SPI or JTAG interfaces.

Figure 3.1.1 and **Figure 3.1.2** show the pin connection information of SPI configuration scheme and JTAG-based configuration for Angelo devices.

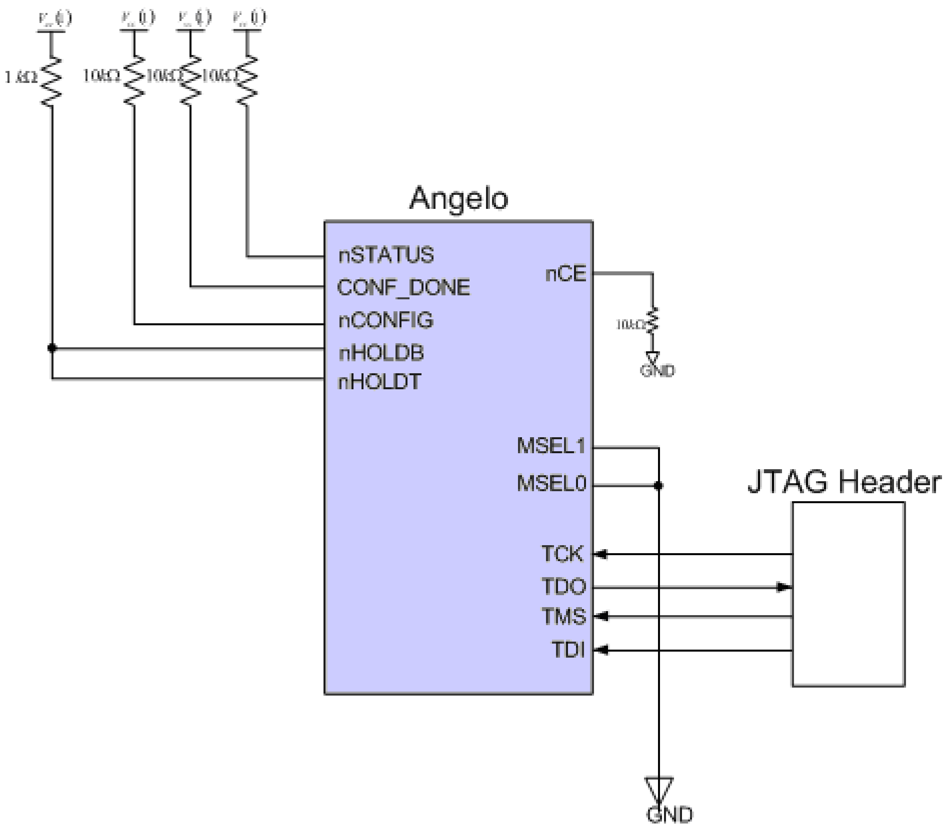


Figure 3.1.1 Configuration for devices with internal flash

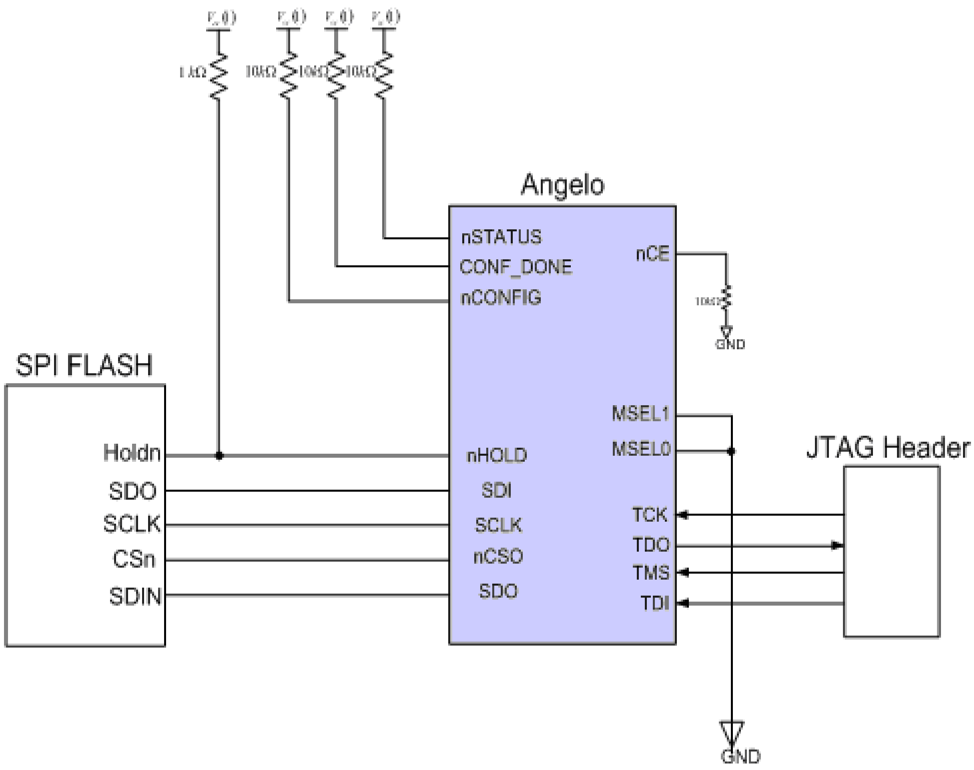


Figure 3.1.2 Configuration for devices without internal flash

Note:

(1) For more information about descriptions of the configuration related pins on Angelo device, please refer to **Table 3.2 -** Configuration Pin Information Summary in the *Configuration Pins and Behavior* section.

(2) Vcc=3.3V

3.2 Configuration Pins and Behavior

This part describes the function information of configuration pins. See **Table 3.2**.

Table 3.2 Configuration and JTAG Pins

nCONFIG	**input**	**Chip global reset input. Active low**
nSTATUS	Bidirectional(open drain)	This is a dedicated configuration status pin , not user I/O
CONF_DONE	Bidirectional(open drain)	This is a dedicated configuration status pin , not user I/O
MSEL0/1	Input	Dedicated mode select control pins for the configuration mode for the device : 00 :Active Serial (Auto Configuration) , 01 Passive Serial , 11 TEST MODE , if JTAG is selected then bits are ignored .
nCE	Input	Configuration Enable. active low

nCEO	I/O, output	Output that drive low when device configuration is completed. During multi device configuration, this pin feeds a subsequence device's CEn pin. During single device configuration and for the last device in multi-device configuration, this pin can be used
TMS	Input	JTAG input pin.
TDI	Input	JTAG input pin.
TCK	Input	JTAG input pin.
TDO	Output	JTAG output pin.
SCLK	input(PS mode) , output (AS mode)	In passive serial configuration mode, SCLK is a clock input used to clock configuration data from external device source into Angelo device. In active serial configuration mode, SCLK is a clock output from Angelo device which is a master in this mode.
SDI	input	Dedicated configuration data input pin.
SDO	I/O, Output	Active serial data output from the Angelo device. In passive serial configuration, this pin becomes user I/O pin.
nCSO	I/O, Output	Chip select output to enable/disable a serial configuration device. This output is used during active serial configuration mode. In passive serial configuration mode this pin become user I/O.
nHOLD	bidirectional(open drain)	Signal of SPI interface. To pause any communication with the device without deselecting it. Active low.
nHOLDB	bidirectional(open drain)	Signal of SPI interface. To pause any communication with the device without deselecting it. Active low.
nHOLDT	bidirectional(open drain)	Signal of SPI interface. To pause any communication with the device without deselecting it. Active low.

Note:

(1) The SCLK, SDIN, HOLDn pins only exist in the packages with external flash: 144-pin TQFP with external flash and 208-pin PQFP with external flash.

(2) PS mode is only applied to PQFP 208 without internal flash

(3) nHOLDB and nHOLDT should connect together with a 1k pull-up resistor for the devices with internal flash.

3.3 JTAG and SPI Configuration Descriptions

There are two different configurations: JTAG configuration and SPI configuration as the following table.

Table 3.3 Angelo configuration mode			
MSEL1	**MSEL0**	**Mode**	**Description**
0	0	AS	Configuration data was read from flash by internal SPI controller
0	1	PS	Angelo acts as slave. External SPI controller feed configuration data into Angelo via SPI interface.
1	0	JTAG	JTAG configuration takes high privilege over AS mode
1	1	Reserved	For testing purpose, not open to customer.

Notes:

1) JTAG configuration is available in AS and JTAG modes; in AS mode, JTAG configuration takes precedence over SPI configuration.

2) Do not leave these pins floating; connect them to VCCIO or ground.

3.3.1 JTAG Configuration

During JTAG configuration, data is downloaded to the device on the board through download cable. Configuring devices through a cable is similar to programming devices in-system.

Angelo devices are designed in such ways that JTAG instructions have precede CEn over any device operating modes. So JTAG configuration can take place without waiting for other configuration to complete (e.g. configuration with serial or enhanced configuration devices). If you attempt JTAG configuration in Angelo devices during non-JTAG configuration, non-JTAG configuration is terminated and JTAG configuration is initiated.

3.3.2 SPI Configuration

Active Serial (AS) SPI Configuration

In the AS configuration scheme, Angelo MSEL1 pin should be set to 0 and MSEL0 should be set to 0. Angelo devices are configured using the industry-standard SPI serial devices. These configuration devices are low cost ones with a non-volatile memory that features a simple few pin interface and a small form factor. These features make serial configuration devices an ideal solution for configuring the low-cost Angelo devices.

Serial configuration devices provide a serial interface to access configuration data. During device configuration, Angelo devices read configuration data via the serial interface, and configure their SRAM cells. This scheme is referred to as an AS configuration scheme because the device controls the configuration interface.

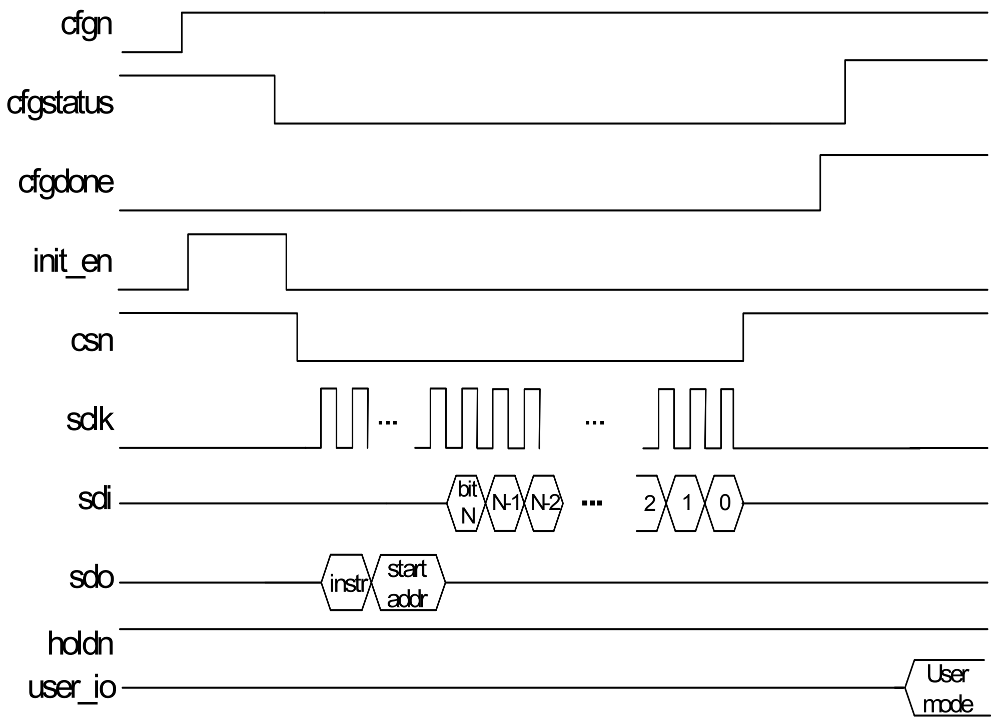


Figure 3.3 Angelo AS Waveform

Above is the AS configuration process. After pow-on-reset, initialization process will start in parallel and will last for 25752 cycles. Init_en will keep high during initialization process. Cfgstatus will go low to prepare for the configuration process when initialization done. When initialization completed, device will send out csn and sclk for reading configuration data in flash. It will also send the read instruction and the read start address by sdo in serial. Instruction is 8 bit long and start address is twenty-four bit long. Then configuration data will then be read out in serial. Holdn will keep logic high level during AS configuration process. Csn will reach a logic high level when reading configuration data process ends. Cfgdone will be pulled up by an external resistor about six cycles after csn goes to high level. Then cfgstatus will also be pulled up at the next negedge of sysclk when cfgdone is one. User mode will go high one clock cycle after the posedge of cfgdone.

Passive Serial (PS) SPI Configuration

In the PS scheme, an external host (configuration device, internal processor, or host PC) controls configuration. Configuration data is input to the target Angelo devices via the SDIN pin at each rising edge of SCLK.

You should select the PS configuration scheme for your application by setting Angelo MSEL1 as 0 and MSEL0 as 1.

DC & Switching Characteristics

4.1 DC Specifications

This section mainly describes the DC specifications of Agate Logic Angelo devices.

4.1.1 LVCMOS33 D.C. Specifications

Table 4.1.1 LVCMOS33 D.C. Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage	VCCIO	-	2.97	3.3	3.63	V
Input Voltage Low	VIL	-	-0.3	-	0.8	V
Input Voltage High	VIH	-	2.0	-	VCCIO+0.3	V
Output Voltage Low	VOL	Iol = 0.1mA	-	-	0.2	V
		Iol = 2 to 16mA	-	-	0.4	V
Output Voltage High	VOH	Ioh = -0.1mA	VCCIO-0.2	-	-	V
		Ioh = -2 to -16mA	2.4	-	-	V

4.1.2 LVTTL33 D.C. Specifications

Table 4.1.2 LVTTL33 D.C. Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage	VCCIO	-	2.97	3.3	3.63	V
Input Voltage Low	VIL	-	-0.3	-	0.8	V
Input Voltage High	VIH	-	2.0	-	VCCIO+0.3	V
Output Voltage Low	VOL	Iol = 2 to 16mA	-	-	0.4	V
Output Voltage High	VOH	Ioh = -2 to -16mA	2.4	-	-	V

Notes for the tables above:

(1) Descriptions of the symbols used in these tables are as follows:

VCCIO – Supply voltage for single-ended inputs and for output drivers

Iol – Output current condition under which VOL is tested

Ioh – Output current condition under which VOH is tested

VIL – Input voltage that indicates a low logic level
VIH – Input voltage that indicates a high logic level
VOL – Output voltage that indicates a low logic level
VOH – Output voltage that indicates a high logic level
(2) Absolute maximum ratings are stress ratings. Continuously operating at or beyond these ratings listed above may cause unrecoverable damage to the device.

4.1.3 Different I/O Driven Strength

Table 4.1.3 I/O Driven Strength

I/O Standard (V)	**Driven Strength(mA)**				
3.3 LVTTL/LVCMOS	16	12	8	4	2

Note:
(1) The values in this table are based on the conditions of testing temperature = 25 ^{o}C, VCCINT = 1.2V, VCCIO = 3.3V.

Pinout Descriptions

5.1 Overview

The Angelo devices are available in three package styles: TQFP100 with internal flash, LQFP144 with internal flash, PQFP 208 with internal flash, and PQFP208 without internal flash. This section mainly describes the various pins on Angelo and how they connect within the supported component packages.

5.2 Pin Types

Most pins of Angelo devices are general-purpose, user-defined I/O pins. There are, however, up to 3 different functional types of pins on Angelo packages, which are Power Supply and Voltage Reference Pins, Clock and PLL Pins and Configuration and JTAG Pins, as outlined in **Table 5.2**.

Table 5.2 Types of Pins on Angelo

Pin Name	Pin Type	Pin Description
Power Supply and Voltage Reference Pins		
VCCIO	Power	Digital VDD for I/O 3.3V
VCCCORE	Power	Digital VDD for CORE 1.2V
GND	Ground	Digital Ground.
VCCA_PLL1/2	Power	Analog power for PLLs. It should connect to 1.5V even if PLL is not used
GNDA_PLL1/2	Ground	Analog ground for PLLs. It can connect to Ground plan on the board
Configuration and JTAG Pins		
nCONFIG	input	Chip reset pin. Active low
nSTATUS	Bidirectional(open drain)	This is a dedicated configuration status pin.
CONF_DONE	Bidirectional(open drain)	This is a dedicated configuration status pin.
MSEL0/1	Input	Dedicated mode select control pins for the configuration mode for the device: 00: Active Serial (Auto Configuration), 01 Passive Serial, 11 TEST MODE, if JTAG is selected then bits is ignored.
nCE	Input	Configuration Enable. active low

nCEO	I/O, output	Output that drives low when device configuration is completed. During multi-device configuration, this pin feeds a subsequence device's nCE pin. During single device configuration and for the last device in multi-device configuration, this pin can be used
TMS	Input	JTAG input pin.
TDI	Input	JTAG input pin.
TCK	Input	JTAG input pin.
TDO	Output	JTAG output pin.
SCLK	input(PS mode) , output (AS mode)	In passive serial configuration mode, SCLK is a clock input used to clock configuration data from external device source into Angelo device. In active serial configuration mode, SCLK is a clock output from Angelo device which is a master in this mode.
SDI	input	Dedicated configuration data input pin.
SDO	I/O, Output	Active serial data output from the Angelo device. In passive serial configuration, this pin becomes user I/O pin.
nCSO	I/O, Output	Chip select output to enable/disable a serial configuration device. This output is used during active serial configuration mode. In passive serial configuration mode this pin become user I/O.
nHOLD	bidirectional(open drain)	Signal of SPI interface. To pause any communication with the device without deselecting it. Active low.
nHOLDB	bidirectional(open drain)	Signal of SPI interface. To pause any communication with the device without deselecting it. Active low.
nHOLDT	bidirectional(open drain)	Signal of SPI interface. To pause any communication with the device without deselecting it. Active low.
Clock and PLL Pins		
CLK0/1/2/3	Input	Dedicated global clock input, If it is not used as clock input, this pin can be general input port.
CLK4/5/6/7	Input	Dedicated global clock input, If it is not used as clock input , this pin can be general input port.

Notes:

(1) The pinout information of Configuration and JTAG Pins is presented in the Configuration *Pins and Behavior* section.

(2) PS mode is only applied to PQFP 208 without internal flash

(3) nHOLDB and nHOLDT should connect together with a 1k pull-up resistor for the devices with internal flash.

5.3 100-Pin Thin Quad Flat Package (TQFP100) with internal flash

Angelo is available in the 100-pin plastic quad flat package with internal flash. **Table 5.3** lists all the package pins. They are arranged in pin numbers.

Table5.3 100-Pin Thin Quad Flat Package Pins with internal flash on Angelo

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	I/O1	35	I/O13	69	GND
2	I/O2	36	VCCINT	70	VCCINT
3	I/O3	37	GND	71	VCCIO5
4	I/O4	38	I/O14	72	I/O37
5	I/O5	39	VCCA_PLL0	73	I/O38
6	I/O6	40	GNDA_PLL0	74	I/O39
7	VCCINT	41	I/O15(CLK0)	75	GND
8	GND	42	I/O16(CLK1)	76	GND
9	GND	43	I/O17(CLK2)	77	I/O40
10	VCCIO0	44	I/O18(CLK3)	78	I/O41
11	nHOLDB	45	I/O19	79	I/O42
12	TMS	46	I/O20	80	VCCIO6
13	TCK	47	GND	81	I/O43
14	TDI	48	VCCIO3	82	I/O44
15	TDO	49	I/O21	83	I/O45
16	I/O7	50	I/O22(nCEO)	84	VCCA_PLL1
17	I/O8	51	I/O23	85	GNDA_PLL1
18	I/O9	52	I/O24	86	I/O46(CLK4)
19	VCCINT	53	GND	87	I/O47(CLK5)
20	GND	54	VCCINT	88	I/O48(CLK6)
21	I/O10	55	I/O25	89	I/O49(CLK7)
22	I/O11	56	I/O26	90	I/O50
23	GND	57	I/O27	91	VCCINT
24	nHOLDT	58	I/O28	92	GND
25	VCCIO1	59	I/O29	93	GND
26	VCCIO2	60	I/O30	94	VCCIO7
27	GND	61	VCCIO4	95	I/O51
28	nCONFIG	62	GND	96	I/O52
29	nCE	63	I/O31	97	I/O53
30	MSEL0	64	I/O32	98	I/O54
31	MSEL1	65	I/O33	99	I/O55

32	CONF_DONE	66	I/O34	100	I/O56
33	nSTATUS	67	I/O35		
34	I/O12	68	I/O36		

5.4 144-Pin Low-profile Quad Flat Package (LQFP144) with internal flash

Angelo is available in the 144-pin low-profile quad flat package with internal flash. **Table 5.4** lists all the package pins. They are arranged in pin numbers.

Table5.4 144-Pin Low-profile Quad Flat Package Pins with internal flash on Angelo

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	I/O1	49	IO27	97	IO63
2	I/O2	50	GND	98	GND
3	I/O3	51	VCCIO3	99	VCCINT
4	I/O4	52	IO28	100	VCCIO6
5	I/O5	53	IO29	101	IO64
6	I/O6	54	VCCINT	102	IO65
7	I/O7	55	GND	103	I/O66
8	I/O8	56	I/O30	104	I/O67
9	I/O9	57	VCCA_PLL0	105	I/O68
10	VCCINT	58	GNDA_PLL0	106	I/O69
11	GND	59	I/O31(CLK0)	107	I/O70
12	I/O10	60	I/O32(CLK1)	108	GND
13	I/O11	61	I/O33	109	GND
14	GND	62	I/O34	110	I/O71
15	VCCIO0	63	I/O35	111	I/O72
16	nHOLDB	64	I/O36	112	I/O73
17	I/O12	65	GND	113	I/O74
18	I/O13	66	VCCIO4	114	I/O75
19	I/O14	67	I/O37	115	VCCIO7
20	TMS	68	I/O38	116	I/O76
21	TCK	69	I/O39	117	I/O77

22	TDI	70	I/O40(nCEO)	118	I/O78
23	TDO	71	I/O41	119	I/O79
24	I/O15	72	I/O42	120	I/O80
25	I/O16	73	I/O43	121	VCCA_PLL1
26	I/O17	74	I/O44	122	GNDA_PLL1
27	I/O18	75	I/O45	123	I/O81(CLK2)
28	VCCINT	76	I/O46	124	I/O82(CLK3)
29	GND	77	GND	125	I/O83
30	I/O19	78	VCCINT	126	I/O84
31	I/O20	79	I/O47	127	I/O85
32	I/O21	80	I/O48	128	I/O86
33	I/O22	81	I/O49	129	VCCINT
34	GND	82	I/O50	130	GND
35	nHOLDT	83	I/O51	131	GND
36	VCCIO1	84	I/O52	132	VCCIO8
37	VCCIO2	85	I/O53	133	I/O87
38	GND	86	I/O54	134	I/O88
39	nCONFIG	87	I/O55	135	I/O89
40	nCE	88	VCCIO5	136	I/O90
41	MSEL0	89	GND	137	I/O91
42	MSEL1	90	I/O56	138	I/O92
43	I/O23	91	I/O57	139	GND
44	I/O24	92	I/O58	140	VCCIO9
45	I/O25	93	I/O59	141	I/O93
46	CONF_DONE	94	I/O60	142	I/O94
47	nSTATUS	95	I/O61	143	I/O95
48	I/O26	96	I/O62	144	I/O96

5.5 208-Pin Plastic Quad Flat Package (PQFP208) with internal flash

Angelo is available in the 208-pin plastic quad flat package with internal flash. **Table 5.5** lists all the package pins. They are arranged in pin number.

Table 5.5 208-Pin Plastic Quad Flat Package with internal flash Pins on Angelo

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	I/O1	71	GND	141	I/O103
2	I/O2	72	VCCIO4	142	GND
3	I/O3	73	I/O47	143	VCCINT
4	I/O4	74	I/O48	144	I/O104
5	I/O5	75	I/O49	145	I/O105
6	I/O6	76	I/O50	146	VCCIO8
7	I/O7	77	I/O51	147	I/O106
8	VCCIO0	78	I/O52	148	I/O107
9	GND	79	VCCINT	149	I/O108
10	I/O8	80	GND	150	I/O109
11	I/O9	81	I/O53	151	I/O110
12	I/O10	82	I/O54	152	I/O111
13	I/O11	83	VCCA_PLL0	153	I/O112
14	VCCINT	84	GNDA_PLL0	154	I/O113
15	GND	85	I/O55(CLK0)	155	I/O114
16	I/O12	86	I/O56(CLK1)	156	GND
17	I/O13	87	I/O57(CLK2)	157	GND
18	GND	88	I/O58(CLK3)	158	I/O115
19	VCCIO1	89	I/O59	159	I/O116
20	I/O14	90	I/O60	160	I/O117
21	I/O15	91	I/O61	161	I/O118
22	nHOLDB	92	I/O62	162	I/O119
23	I/O16	93	GND	163	VCCIO9
24	I/O17	94	VCCIO5	164	I/O120
25	I/O18	95	I/O63	165	I/O121
26	I/O19	96	I/O64	166	I/O122
27	I/O20	97	I/O65	167	I/O123
28	TMS	98	I/O66	168	I/O124
29	TCK	99	I/O67	169	I/O125
30	TDI	100	I/O68	170	I/O126
31	TDO	101	I/O69(nCEO)	171	I/O127

32	I/O21	102	I/O70	172	I/O128
33	I/O22	103	I/O71	173	VDDA_PLL1
34	I/O23	104	I/O72	174	GNDA_PLL1
35	I/O24	105	I/O73	175	I/O129(CLK4)
36	I/O25	106	I/O74	176	I/O130(CLK5)
37	I/O26	107	I/O75	177	I/O131(CLK6)
38	I/O27	108	I/O76	178	I/O132(CLK7)
39	I/O28	109	GND	179	I/O133
40	I/O29	110	VCCINT	180	I/O134
41	I/O30	111	VCCIO6	181	I/O135
42	VCCINT	112	GND	182	I/O136
43	GND	113	I/O77	183	I/O137
44	I/O31	114	I/O78	184	I/O138
45	I/O32	115	I/O79	185	I/O139
46	I/O33	116	I/O80	186	VCCINT
47	I/O34	117	I/O81	187	GND
48	I/O35	118	I/O82	188	I/O140
49	I/O36	119	I/O83	189	I/O141
50	GND	120	I/O84	190	GND
51	nHOLDT	121	I/O85	191	VCCIO10
52	VCCIO2	122	I/O86	192	I/O142
53	VCCIO3	123	I/O87	193	I/O143
54	GND	124	I/O88	194	I/O144
55	nCONFIG	125	I/O89	195	I/O145
56	nCE	126	VCCIO7	196	I/O146
57	MSEL0	127	GND	197	I/O147
58	MSEL1	128	I/O90	198	I/O148
59	I/O37	129	I/O91	199	I/O149
60	I/O38	130	I/O92	200	I/O150
61	I/O39	131	I/O93	201	I/O151
62	I/O40	132	I/O94	202	GND
63	I/O41	133	I/O95	203	VCCIO11
64	I/O42	134	I/O96	204	I/O152
65	CONF_DONE	135	I/O97	205	I/O153

66	nSTATUS	136	I/O98	206	I/O154
67	I/O43	137	I/O99	207	I/O155
68	I/O44	138	I/O100	208	I/O156
69	I/O45	139	I/O101		
70	I/O46	140	I/O102		

5.6 208-Pin Plastic Quad Flat Package (PQFP208) without internal flash

Angelo is available in the 208-Pin plastic quad flat package without internal flash. **Table 5.6** lists all the package pins. They are arranged in pin number.

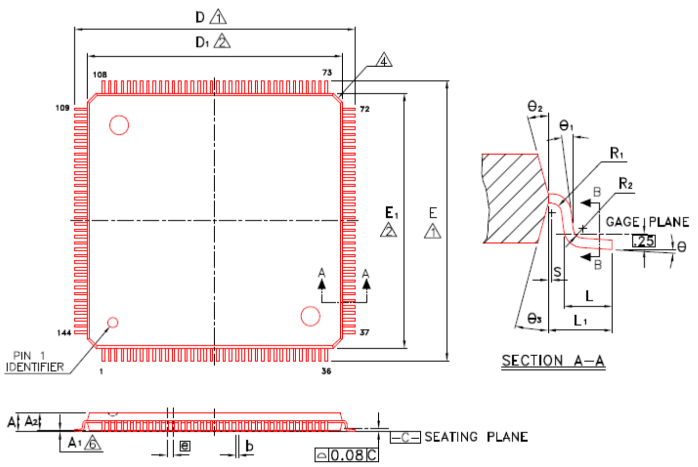
Table 5.6 208-Pin Plastic Quad Flat Package without internal flash Pins on Angelo

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	I/O1	71	GND	141	I/O100
2	I/O2	72	VCCIO4	142	GND
3	I/O3	73	I/O44	.143	VCCINT
4	I/O4	74	I/O45	144	I/O101
5	I/O5	75	I/O46	145	I/O102
6	I/O6	76	I/O47	146	VCCIO8
7	I/O7	77	I/O48	147	I/O103
8	VCCIO0	78	I/O49	148	I/O104
9	GND	79	VCCINT	149	I/O105
10	nCSO	80	GND	150	I/O106
11	SDO	81	I/O50	151	I/O107
12	SDIN	82	I/O51	152	I/O108
13	SCLK	83	VCCA_PLL0	153	I/O109
14	VCCINT	84	GNDA_PLL0	154	I/O110
15	GND	85	I/O52(CLK0)	155	I/O111
16	I/O8	86	I/O53(CLK1)	156	GND
17	I/O9	87	I/O54(CLK2)	157	GND
18	GND	88	I/O55(CLK3)	158	I/O112
19	VCCIO1	89	I/O56	159	I/O113

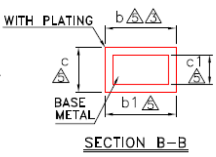
20	I/O10	90	I/O57	160	I/O114
21	nHOLD	91	I/O58	161	I/O115
22	I/O11	92	I/O59	162	I/O116
23	I/O12	93	GND	163	VCCIO9
24	I/O13	94	VCCIO5	164	I/O117
25	I/O14	95	I/O60	165	I/O118
26	I/O15	96	I/O61	166	I/O119
27	I/O16	97	I/O62	167	I/O120
28	TMS	98	I/O63	168	I/O121
29	TCK	99	I/O64	169	I/O122
30	TDI	100	I/O65	170	I/O123
31	TDO	101	I/O66(nCEO)	171	I/O124
32	I/O17	102	I/O67	172	I/O125
33	I/O18	103	I/O68	173	VCCA_PLL1
34	I/O19	104	I/O69	174	GNDA_PLL1
35	I/O20	105	I/O70	175	I/O126(CLK4)
36	I/O21	106	I/O71	176	I/O127(CLK5)
37	I/O22	107	I/O72	177	I/O128(CLK6)
38	I/O23	108	I/O73	178	I/O129(CLK7)
39	I/O24	109	GND	179	I/O130
40	I/O25	110	VCCINT	180	I/O131
41	I/O26	111	VCCIO6	181	I/O132
42	VCCINT	112	GND	182	I/O133
43	GND	113	I/O74	183	I/O134
44	I/O27	114	I/O75	184	I/O135
45	I/O28	115	I/O76	185	I/O136
46	I/O29	116	I/O77	186	VCCINT
47	I/O30	117	I/O78	187	GND
48	I/O31	118	I/O79	188	I/O137
49	I/O32	119	I/O80	189	I/O138
50	I/O33	120	I/O81	190	GND
51	GND	121	I/O82	191	VCCIO10
52	VCCIO2	122	I/O83	192	I/O139
53	VCCIO3	123	I/O84	193	I/O140

54	GND	124	I/O85	194	I/O141
55	nCONFIG	125	I/O86	195	I/O142
56	nCE	126	VCCIO7	196	I/O143
57	MSEL0	127	GND	197	I/O144
58	MSEL1	128	I/O87	198	I/O145
59	I/O34	129	I/O88	199	I/O146
60	I/O35	130	I/O89	200	I/O147
61	I/O36	131	I/O90	201	I/O148
62	I/O37	132	I/O91	202	GND
63	I/O38	133	I/O92	203	VCCIO11
64	I/O39	134	I/O93	204	I/O149
65	CFNF_DONE	135	I/O94	205	I/O150
66	nSTATUS	136	I/O95	206	I/O151
67	I/O40	137	I/O96	207	I/O152
68	I/O41	138	I/O97	208	I/O153
69	I/O42	139	I/O98		
70	I/O43	140	I/O99		

Mechanical



NOTE :
1. TO BE DETERMINED AT SEATING PLANE –C– .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026 , BFB.



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.20 REF			0.008 REF		
c	0.12	—	0.20	0.005	—	0.008
c_1	0.13 REF			0.005 REF		
D	21.85	22.00	22.15	0.860	0.866	0.872
D_1	19.90	20.00	20.10	0.783	0.787	0.791
E	21.85	22.00	22.15	0.860	0.866	0.872
E_1	19.90	20.00	20.10	0.783	0.787	0.791
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.15 REF			0.006 REF		
R_2	0.15 REF			0.006 REF		
S	0.19 REF			0.007 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	7° REF			7° REF		
$θ_2$	12° REF			12° REF		
$θ_3$	12° REF			12° REF		

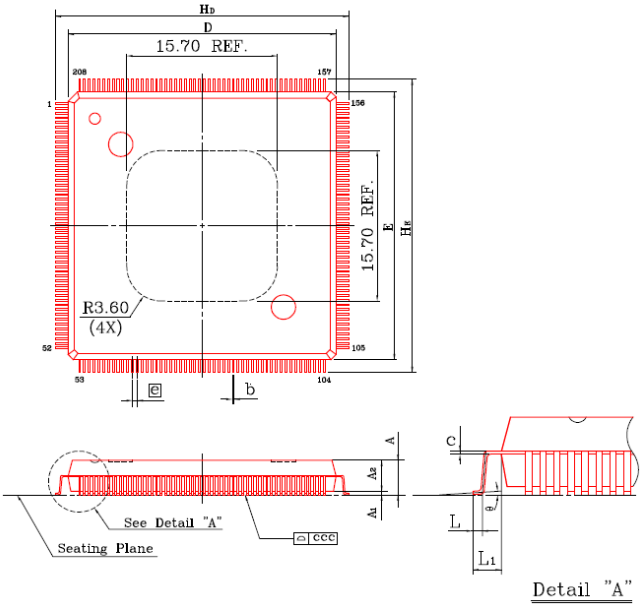
TITLE: 144LD LQFP(20x20x1.4mm) PACKAGE OUTLINE –Cu L/F,FOOTPRINT 2.0mm			
L/F MATERIAL: C7025 1/2H			
APPR.	Holman Chen	DWG NO.	D144–SW1
ENG.	Richard Lee	REV NO.	B
QM.	S.T.Liao	PRODUCT CODE	D1441C
CHK.	Y.Y.Lai	DATE	07/11/'01
DWG.	Rex Lee	SHT No.	1/1
SILICONWARE PRECISION INDUSTRIES CO., LTD.			

COPY CONTROLLED

REV NO	DESCRIPTION	DATE
B	dwg name from TQFP to LQFP	07/11/'01

REV.B

01–5700–10



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	4.07	—	—	0.160
A_1	0.25	—	—	0.010	—	—
A_2	3.15	3.23	3.30	0.124	0.127	0.130
b	0.18	—	0.28	0.007	—	0.011
c	0.13	—	0.23	0.005	—	0.009
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
$\boxed{e}$	0.50 BSC			0.020 BSC		
H_D	30.35	30.60	30.85	1.195	1.205	1.215
H_E	30.35	30.60	30.85	1.195	1.205	1.215
L	0.35	0.50	0.65	0.014	0.020	0.026
L_1	1.30 REF			0.051 REF		
ccc	0.10			0.004		
θ	0°	—	7°	0°	—	7°

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. Heat Spreader material: Al
6. Special Characteristics C class : ccc

TITLE: 208LD EDHS-QFP(28X28mm) PACKAGE OUTLINE -Cu L/F, FOOTPRINT 2.6mm			
LEADFRAME MATERIAL: C7025 1/2H			
APPR.	F.D.Tang	DWG NO.	V208-SW3
ENG.	Albert Lee Jack Lee	REV NO.	B
Q.M	S.T.Liao	PRODUCT CODE	V2082C
CHK.	Y.Y.Lai	DATE	02/15/'05
DWG.	R.K.Wang	SHT NO.	1/1

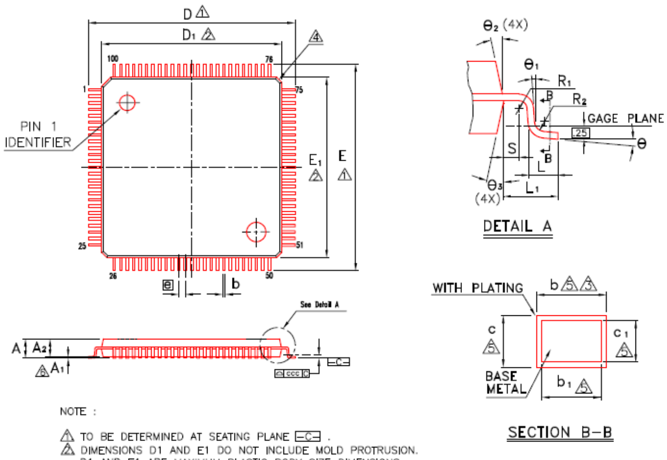
COPY CONTROLLED

REV NO	DESCRIPTION	DATE
B	ADD HEAT SINK DIMENSION & NOTE 6	02/15/'05

SILICONWARE PRECISION INDUSTRIES CO., LTD.

REV.B

QI-5700-10



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	16.00 BSC			0.630 BSC		
D_1	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E_1	14.00 BSC			0.551 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026
9. SPECIAL CHARACTERISTICS C CLASS: ccc

TITLE: 100LD TQFP(14x14x1.0mm) PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm		
L/F MATERIAL: C7025 1/2H		

APPR.	F.D.Tang	DWG NO.	Z100-SW1
ENG.	Albert Lee Chih Hsin Lai	REV NO.	B
Q.M	S.T.Liao	PRODUCT CODE	Z1001C
CHK.	Y.Y.Lai	DATE	02/15/'05
DWG.	R.K.Wang	SHT NO.	1/1

SILICONWARE PRECISION INDUSTRIES CO., LTD.

REV NO	DESCRIPTION	DATE
B	(1) UPDATE "c1" MAX. INCH DIMENSION FROM 0.630 TO 0.006 (2) ADD NOTE 9	02/15/'05

COPY CONTROLLED

REV.B

OI-5700-10

Ordering Information

AG1F	4	E5	N1	Q208	G	C7	-	ES

FPGA Density

4: 4096

Optional Suffix

ES: Optional Suffix

RoHS Compliant

G: Pb-free

MCU Type

E5: 8051

A7: Arm7

A9: Arm9

Nonvolatile Memory

N: Flash

T: OTP

1: 1M

2: 2M

4: 4M

8: 8M

Package Type

T: Thin quad flat pack (TQFP)

L: Low profile quad flat package (LQFP)

Q: Plastic Quad Flat Pack (PQFP)

F: FinelineBGA

208:208 pin

100:100 pin

144:144 pin

C/I/M and Speed

C: Commercial (0, +85)

I: Industria (-40, +100)

M: Military (-55, +125)

8: Speed 8

7: Speed 7

6: Speed 6

Contact Information

Tel: +8610 82150100

E-mail: sales@agatelogic.com

Website: www.agatelogic.com.cn