Flash Controller User Guide

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Agate Logic, Inc.

Contents

About This Guide

The Flash Controller IP v1.0 User Guide describes the read and write operation of a flash, as well as information about designing and implementing the IP.

Introduction

Section 1

1.1 Device Family Support

The Flash Controller IP supports the following target AGATELOGIC device families:

- Angelo

1.2 Introduction

Users can operate the configurable flash chip by the flash controller IP. This IP offers a very simple parallel interface to user.

1.3 Features

- Support erase flash one sector one time only
- Support write flash 1 to 256 bytes one time
- Support read flash 4N bytes

2.1 Flash Controller Interfaces

Figure 1 illustrates the flash controller interfaces.

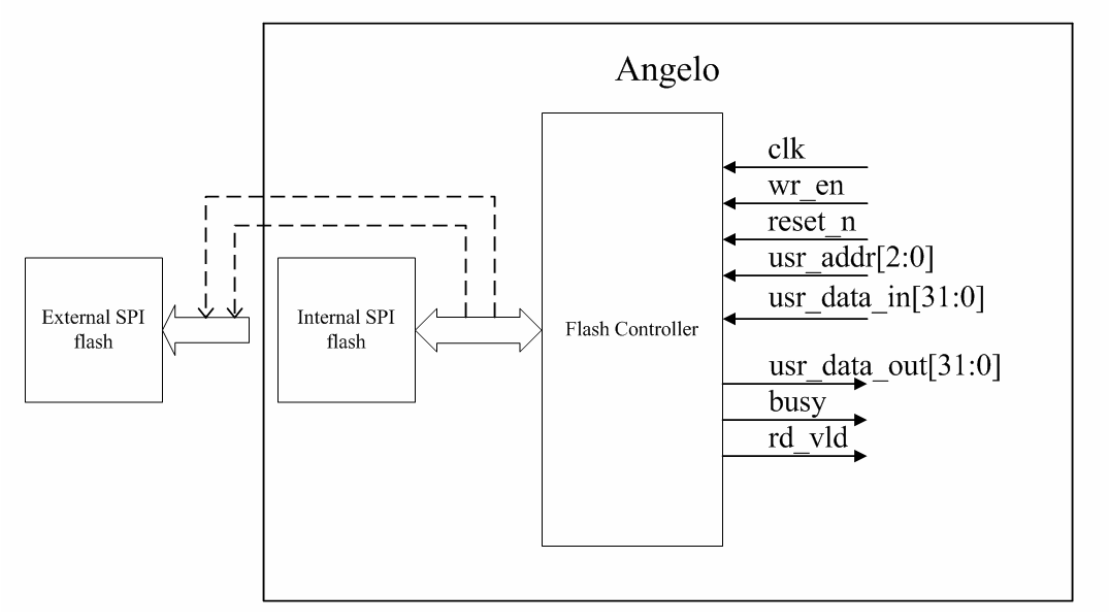

Figure 1 Flash Controller Interfaces

2.2 Interface Signals

Table 2 defines the signals for the SPI user interface.

Table 1 SPI User Interface Signals

Name	Direction	Width	Description
clk	Input	1	system clock: above 15MHz
reset_n	Input	1	reset signal: active low
wr_en	Input	1	write enable: the rising wr_en signal, data is written to registers
usr_addr	Input	3	register address
usr_data_in	Iutput	32	write into data
usr_data_out	Output	32	read out data
busy	Output	1	write busy signal: active high
rd_vld	Output	1	read valid: active high

2.3 Flash Controller Usage

2.3.1. Registers

Table 2 describes the flash controller IP registers. All the control flash commands will be written to flash command register. The start address of read and write operation will be written to start address register. Read and write flash length amount will be written to operation length register. If read operation, the MSB of operation length register must be 1, and the write operation the MSB of operation length register must be 0.

Table 2 User Registers

Register name	Width	Register address	Comment
Flash command register	32	0	Refer to table 3
Start address register	32	1	Start address of read and write operation
Operation length register	32	2	The length of read and write operation
Input data register	32	3	

2.3.2. Flash operation command

Table 3 Flash Operation Command

Function Name	Encoded Value	Description
WREN	32'h00000006	Write Enable
READ	32'h00000003	Read operation
SE	32'h000000d8	Sector Erase
PP	32'h00000002	Write operation

2.3.3. Write and Read Flash Operation

In Angelo devices, the capacity of a configurable flash is 4M bits. The first 2M-bit space only deposits the FPGA configurable data which can neither be read and written by users. The other 2M-bit space is available for users to read and write. The corresponding sector addresses must be erased before the flash is written. Users can write data, from 1 to 256 bytes each time, to the flash. If users want to write 30 bytes to flash and must write 29 to the operation length register. The rule also applies to the read operation. In this IP of data interface is 32-bit width and the MSB will be written to flash first. If users want to write 0x1234 to flash, they must set the operation length to 1 and write 0x12340000 to input data register. If the busy signal is high, users can't write command or data to the IP. The length of read operation must be a multiple of 4. When the rd_vld signal is valid, users can read 32-bit data from flash one time. If the data are not read, the data will be covered when the next rd_vld comes.

Erase Flash Flow

- Set flash write enable (write 32’h00000006 to flash command register)
- Set the erase sector address (write address to start address register)
- Set flash erase sector command (write 32’h000000d8 to flash command register)

  Figure 2 describes the ease flash timing. Users must wait for 1.5ms to start a new write operation after sending erase command.

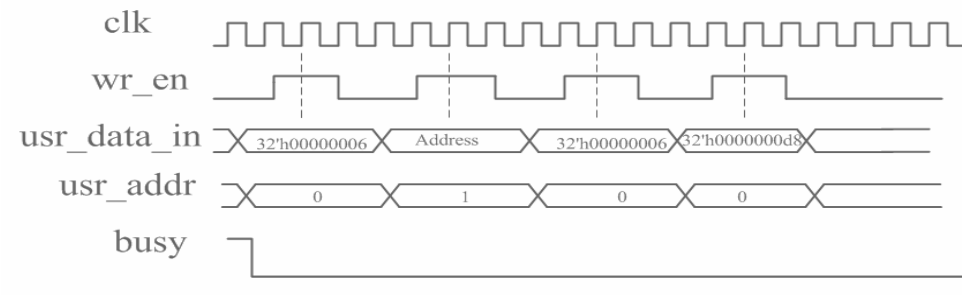

Figure 2 Erase Flash Timing

Write Flash Flow

- Set flash write enable (write 32’h00000006 to flash command register)
- Set the write operation start address (write address to start address register)
- Set the write operation length (write operation length to operation length register)
- Set flash write command (write 32’h00000002 to flash command register)
- Send the written data (write data to input data register)

  Figure 3 describes the write flash timing. The interval of two write operations must exceed 1.5ms. When the busy signal is high, don’t write any data and command to registers.

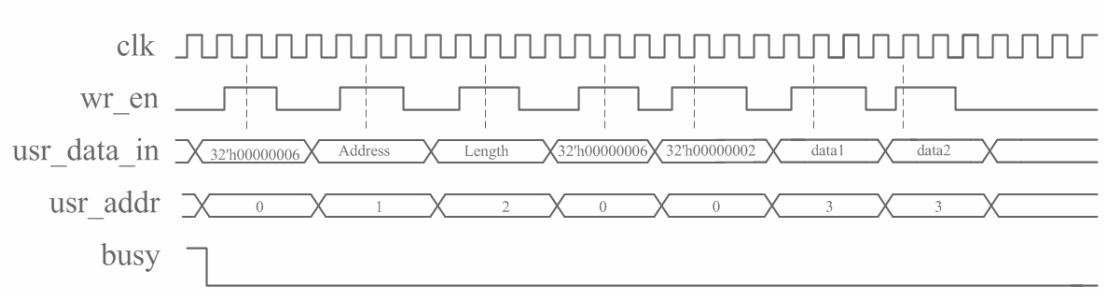

Figure 3 Write Flash Timing

Read Flash Flow

- Set flash write enable (write 32’h00000006 to flash command register)
- Set the read operation start address (write address to start address register)
- Set the read operation length (write operation length to operation length register)
- Set flash write enable (write 32’h00000006 to flash command register)
- Set flash read command (write 32’h00000003 to flash command register)

Figure 4 describes the read flash timing. User must note that the data will be covered when the next rd_vld comes.

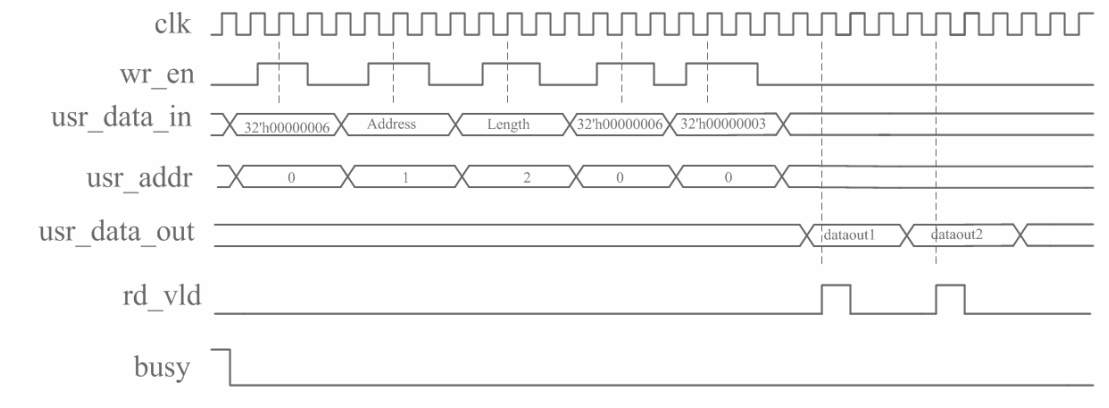

Figure 4 Read Flash Timing

Simulating Design

Section 3

3.1 Simulating Your Design

The AGATELOGIC provides the behavioral model to customers for simulation.

The behavioral models are considered to be zero-delay models, as the modeled write-to-read latency is nearly zero. The behavioral models are functionally correct, and will represent the behavioral of the flash controller.

4.1 SPI User Interface IP Instantiation

```
module ip_module_name(
        clk,
        reset_n,
        wr_en,
        usr_data_in,
        usr_data_out,
        usr_addr,
        busy,
        rd_vld);


input    clk;
input    reset_n;
input    wr_en;
input [2:0] usr_addr;
input [31:0] usr_data_in;
output [31:0] usr_data_out;
outputt busy;
output rd_vld;

            flash_controller    inst (
               .clk(clk),
               .reset_n (reset_n),
               .wr_en (wr_en),
               .usr_addr (usr_addr),
               .usr_data_in (usr_data_in),
               .usr_data_out(usr_data_out),
               .busy (busy),
               .rd_vld (rd_vld));
```

About Agate Logic

Agate Logic is the global pioneer and leader of the innovative Adaptable Programmable Gate Array (APGA) technologies. The company offers a full spectrum of programmable logic devices, software design tools, intellectual property (IP) and design services. Focusing on multiple applications such as telecommunication equipments, industrial control systems and consumer products, we use the Chinese leading foundry partner, SMIC, to manufacture our chips to offer solutions tailored for the market in China.

Technical Support Assistance

Tel: +86 10 82150100

E-mail: support@agatelogic.com

Website: www.agatelogic.com.cn