Agate Logic Flexera Family Datasheet

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About This Datasheet

This datasheet provides comprehensive information about the Agate Logic Flexera family devices.

Revision History

The revision history of this document is listed as below:

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1	November, 2006.	1.0	Initial Release
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3	November, 2006.	1.0	Initial Release
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5	November, 2006.	1.0	Initial Release

Additional Resources

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Introduction

Chapter 1   **Complete Datasheet**

This document provides designers with the datasheet specifications for the first APGA family devices of Agate Logic Corporation: Flexera. The chapters contain feature definitions of the internal architecture, configuration, DC operating conditions.

This document contains the following chapters:

- Chapter 1.Introduction
- Chapter 2.Flexera Architecture
- Chapter 3.Configuration
- Chapter 4.DC & Switching Characteristics
- Chapter 5. Pinout Information

Overview

The first APGA generation Flexera was designed to provide a perfect mix of density and features to provide a low-cost and more flexible alternative to ASICs and FPGAs. The Flexera series provides a flexible, risk-free option without up-front non-recurring engineering charges or minimum order quantities. With its low-cost solution unmatched by any FPGA, the HyperBlox MP sections of Flexera have been configuration to some advanced features such as MCU,SDR/DDR core logic and I/O,PCI core logic and I/Os, etc. The HyperBlox FP sections of Flexera can be configured by user. Flexera series APGA provide 8K to 32K logic cells (LUT/Register). Half of the logic cells are for FP and the others are for MP. They also offer from 10 to 32 256*36 bit true double port RAM Blocks. The max user I/Os are more than 300. Flexera devices are manufactured on 300-mm wafers using SMIC 130-nm 1P8M 1.2V/3.3V CMOS process.

The Flexera device family offers the following features:

Features

- Field-programmable through embedded SRAM-based FPGA fabric
- Capacity to accommodate the unique designs
    - 4k to 16k Field Programmable LUT/Register Core Cells
    - An additional 4k to 16k Via Mask Programmable LUT/Register Core Cells
    - Up to 288 Kbits (32 * 256*36 bits) of configurable pipeline able dual-ported RAM in 9Kb blocks
    - 2 PLLs & 4 DLLs (Phase-Locked/Delay-Locked Loop) with programmable phase-shift and division
    - Up to 16 low skew global clocks and reset trees

- Flexible I/O options
    - ✓ General Purpose I/O: 3.3V, 2.5V, 1.8V LVCMOS/LVTTL, PCI, HSTL, SSTL, LVDS
- DDR memory support
- Routing architecture delivers predictable timing and high utilization
- Supports system speeds over 250 MHz
- 150 ps maximum clock skew distribution architecture
- Mask-programmable option has higher reliability and design security than using field programmable portion alone
- Compatible with industry-standard ASIC and FPGA design tools
- Manufactured in leading-edge 0.13 micron process for maximum performance and density
- Package options
    - ✓ 144 pin TQFP 22 x 22 mm size 98 user I/Os
    - ✓ 240 pin PQFP 34.6x34.6 mm size 185 user I/Os
    - ✓ 256 pin FineLine BGA 17 x 17 mm size 185user I/Os
    - ✓ 324 pin FineLine BGA 19 x 19mm size 249user I/Os
    - ✓ 400 pin FineLine BGA 21 x 21mm size 301user I/Os

Table 1.1 summarizes the features of the Flexera series

Table 1.1 Flexera Series Features	
Parameter	**Flexera**
Core Voltage	1.2 V
I/O Voltage	3.3 V, 2.5 V, 1.8 V, 1.5 V
Process Technology	130-nm
FP Logic Cells	4,096 to 16,384
MP Logic Cells	4,096 to 16,384
User I/O Pins	104 to 301
RAM8K Blocks	10 to 64
PLL	2
DLL	4
I/O Standards Support	LVTTL, LVCMOS, PCI, SSTL,LVDS, RSDS
External Memory Interfaces	SDR, DDR
Speed Grades	-6, -7, -8

Table 1.2 summarizes Flexera Package Options & I/O Pin Counts.

Table 1.2 Flexera Package Options & I/O Pin Counts					
Device	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
AG1F8	104	185			
AG1F12	98	185	185		
AG1F24		173	185	249	
AG1F32				233	301

Table 1.3 summarizes Flexera OFP & FineLine BAG Package Sizes.

Table 1.3 Flexera QFP & FineLine BGA Package Sizes					
Dimension	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
Pitch (mm)	0. 5	0.5	1.0	1.0	1.0
Area (mm²)	484	1,024	289	361	441
Length × width (mm × mm)	22 × 22	34.6 × 34.6	17 × 17	19 × 19	21 × 21

Top-level Architecture

Chapter 2.1   **Complete Datasheet**

Flexera family is the first APGA generation of Agate Logic Corporation. Built with an extremely efficient architecture, Flexera is designed to offer flexible, risk-free, and low-cost options to users. This section provides comprehensive information about the architecture of Flexera devices.

The following shows the main chapters in the Flexera Architecture:

Architecture Overview

The Flexera device architectures contain an array of filed programmable logic blocks (FP) surrounded by soft Programmable I/O Cells element (SPIO). Rows of Embedded Block DPRAM are alongside of FP logic array, and up to two PLLs as well as four DLLs were provided for a complete clock management solution. In addition, DDR controller hardware IP and 8051 IP were embedded in the devices, which supplies with more flexible and efficient usage for users.

The FP core consists of an array of configurable logic cells and configurable routing muxes that interconnect the logic cells in a hierarchical architecture, which delivers predictable timing and high utilization. 4096 LUT4 and 8192 D-type flip-flops or D-type latches are available in Flexera FP core.

The SPIO of Flexera devices support General Purpose I/O: 3.3V, 2.5V, 1.8V LVCMOS/LVTTL, PCI, HSTL, SSTL, LVDS etc.

Flexera Embedded DPRAM is a true dual-port RAM. Each block can be configured to the following DPRAM width: $1 \times 8k$, $1 \times 9k$, $2 \times 4k$, $4 \times 2k$, $8 \times 1k$, $9 \times 1k$, 16×512, 18×512, 32×256, and 36×256.

Flexera devices contain up to two PLLs and four DLLs. 16-Phases PLL Clock

Generator has multiplication, division and phase shifting capabilities, and one of the four DLLs is used for DDR controller hardware IP.

Every device in the family has a JTAG Port and a SPI port. SPI Port is used to interface with serial Flash and other EEPROM devices for loading the configuration bit stream into the device. The Flexera devices can support both Master and Slave modes.

Flexera devices are manufactured on 300-mm wafers using SMIC 130-nm 1P8M 1.2V/3.3V CMOS process.

Figure 2.1.1 shows the top level architecture of Flexera device.
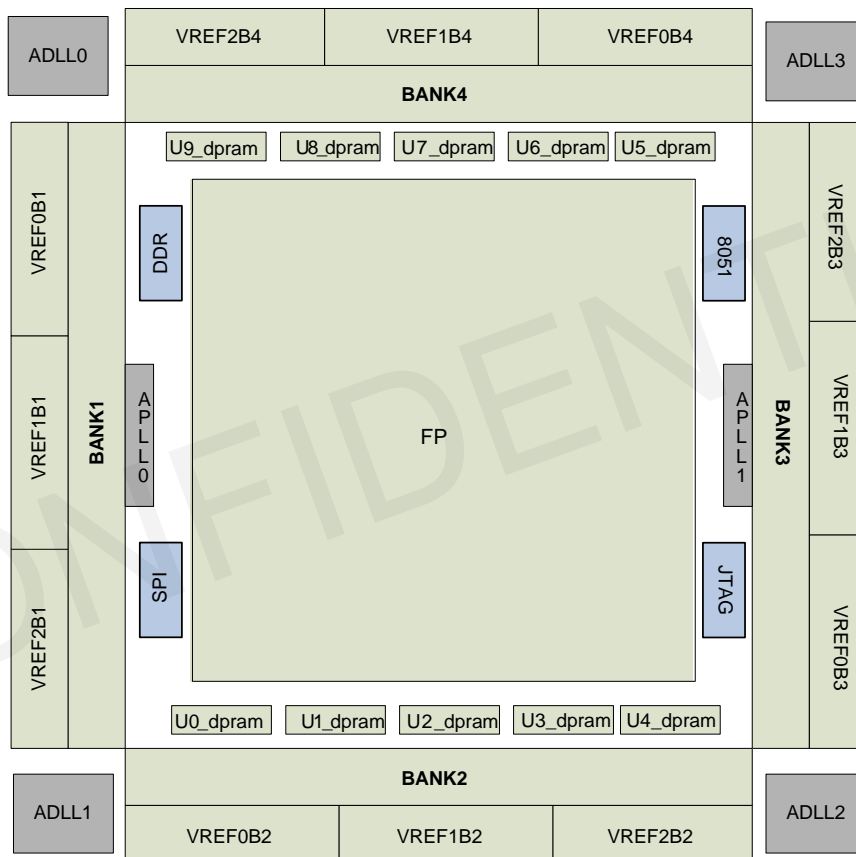
Figure 2.1.1 Top Level Architecture

Field programmable (FP) Core

Chapter 2.2   **Complete Datasheet**

Features

As the first APGA generation of Agate Logic, Flexera devices contain an array of filed programmable logic blocks (FP). Features of the FP are described as follows:

- 4096 logic cells.
- 4096 auxiliary inputs available.
- 4096 auxiliary outputs available.
- 16 global signals available as register clock, reset signals.
- 8192 D-type flip-flops available.
- 8192 D-type latches available.
- Maximum wide LUT function of 14 inputs.
- 2 configurable shift registers path.
- Dual logic cell functions 8-input AND, 8-input OR, and 8-input XOR.
- Dedicated Arithmetic circuitry

FP Logic Cell

The architecture of the logic cell is shown in **Figure 2.2.1.** The logic cell contains a 4-input Look-Up table (LUT) and 2 logic paths: path0 and path1. Each path leads to a logic cell output that drives the routing fabric. The path1 output is also considered a auxiliary output and can drive other components in Flexera devices, such as embedded DPRAM、SPIO、DLL、PLL、hardware DDR Controller IP etc. Path0 has a configurable option to receive the auxiliary input (which can be driven by the output of embedded DPRAM、SPIO、DLL、PLL、hardware DDR Controller IP etc.)and send it directly to the routing fabric. Each path can be configured independently as a registered path, either registered by a D-type flip-flop or a D-type latch. Or, each path can be configured to bypass the registers if the logic cell represents a level of logic in a multi-level logic cone.
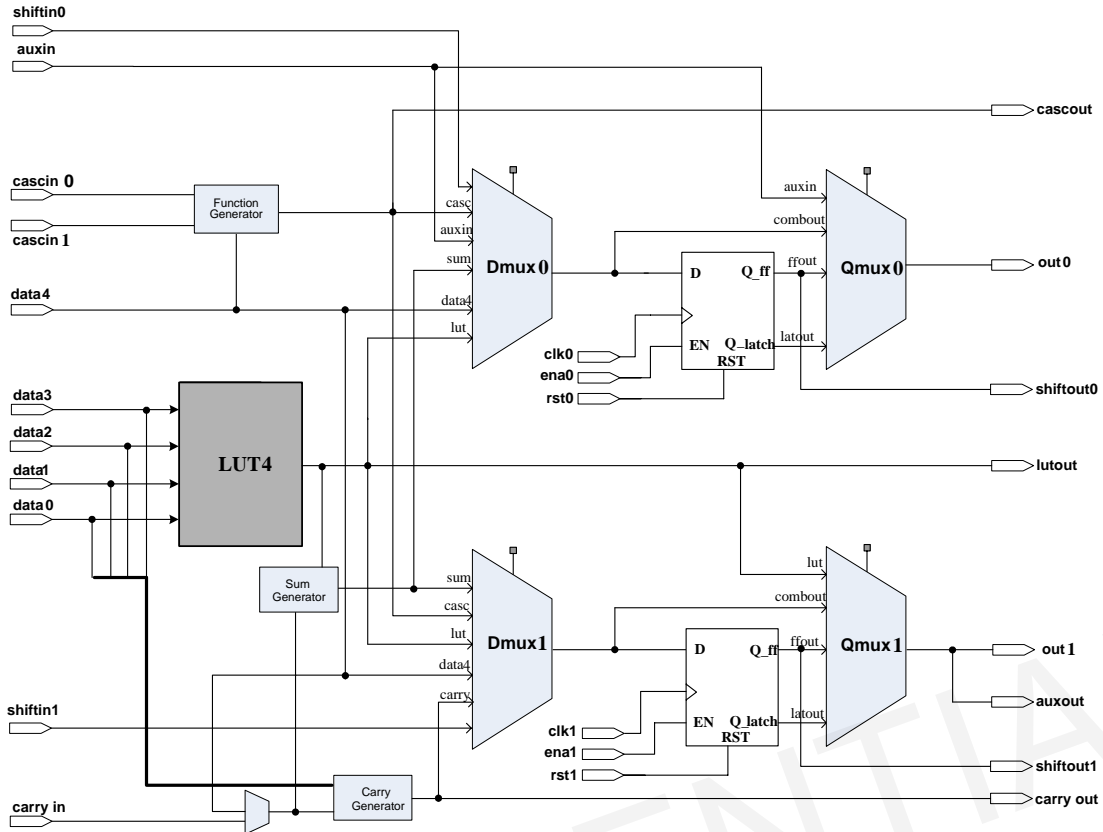
Figure 2.2.1 FP Logic Cell

The D-type flip-flop (DFF) and the latch in path0 share the same clock, reset, and clock enable coming from that logic cell's clock bundle control unit. Similarly, the DFF and latch in path1 share the same clock, reset, and clock enable that are independent of the global signals driving the path0 register elements. Clocks entering the logic cells trigger the DFF's on the rising-edge and open the latches when the logic level is VDD. Resets entering the logic cells are asynchronous and active-high. Clock enables entering the logic cells are active-high. For more information on clock, reset and clock enable signal, see the Clock Bundle Control Logic section.

Normal mode

The logic cell in normal mode contains a 16-bit LUT and one DFF/LATCH. User design can be synthesized friendly based on the basic cell. **Figure 2.2.2** shows the logic cell in normal mode.
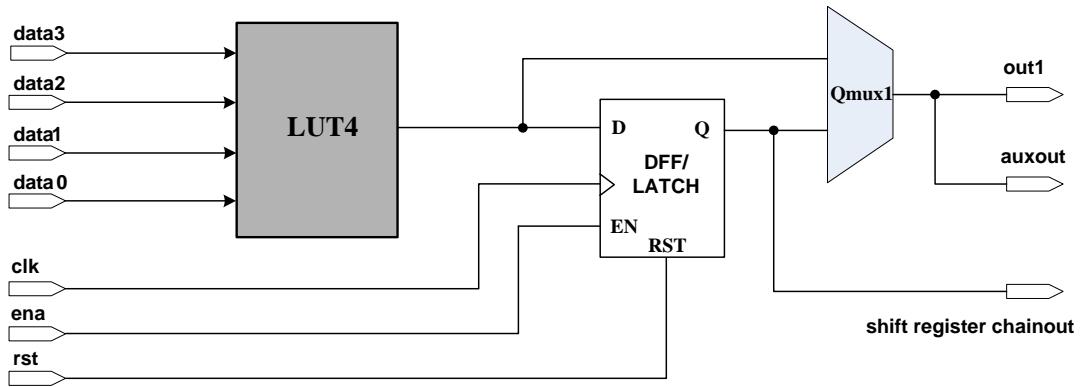
Figure 2.2.2 Normal Mode

The 16-bit LUT is used as a whole to realize a LUT4 function: the output of LUT4 can lead to routing fabric directly, or pass through DFF/Latch to routing fabric then drive the auxout. Output of the register can be the input of shift register in next level.

Arithmetic Mode

The sum generator simply is an XOR of the LUT4 result and the carry input. It produces the sum value of a 1-bit full adder entirely within the logic cell. The adder operands are 2 of the 4 inputs to the LUT4 function, where the other inputs must be configured as enables. The next part describes adder and subtracters in more detail.

Each logic cell produces a sum of 1-bit operands as shown in **Figure 2.2.3**.
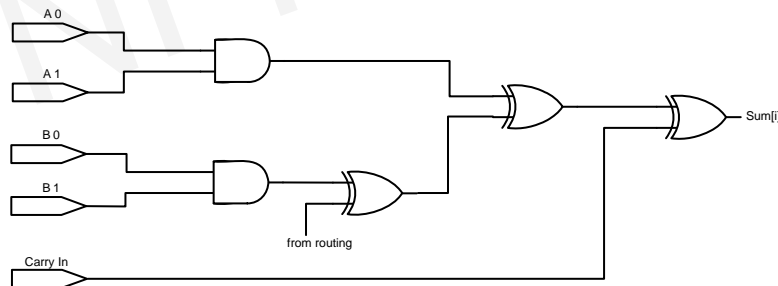
Figure 2.2.3: FP Logic Cell Sum Generation

Here, the LUT is programmed to pattern 0x7888, which implements the logic shown. The operand drives either A0 or A1 with the other tied to VDD. The B operand drives either B0 or B1 with the other tied to VDD. The VDD tie-offs enable the operand bits to pass through into the sum logic, which is the XOR gate representation inside the LUT. The sum of the operand bits then would be summed with the carry input in the sum generator. Whichever output path is chosen to propagate the sum, the respective Dmux is configured to select and pass the result from the sum generator onto the output logic, where it may be optionally registered. To realize more complex added functions, configure the LUT with the appropriate pattern. For example, the inputs otherwise tied off could be used as a parallel load signal and an up/down select for a counter

configuration. Program the LUT accordingly to realize the additional functionality.

The carry logic in a logic cell is shown in **Figure 2.2.4**.
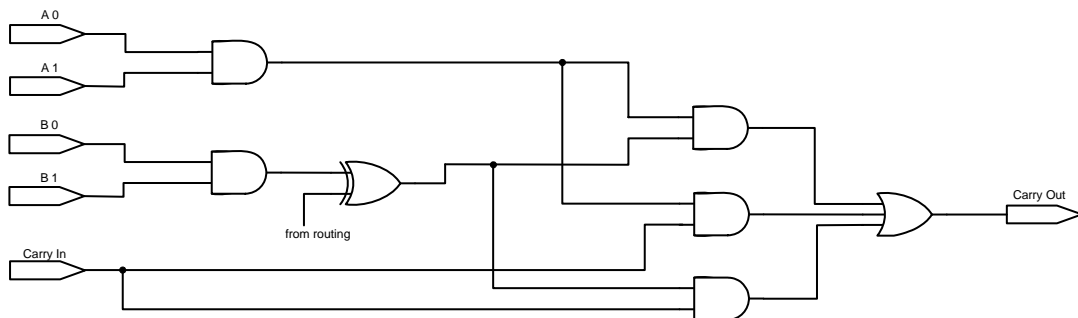
Figure 2.2.4: FP Logic Cell Carry Generator

The carry logic is a standard carry generator for ripple carry full adders with additional AND gates after the operand bits to allow flexibility in swapping, for example, A0 and A1 for the A operand (the other, of course, must be tied to VDD to allow the operand to pass through the carry generator). On the B operand, a configurable mux selects between the operand and its inverse. By default, the B operand passes through for add functions. If either Dmux is set to SUB, the setting is encoded to select the inverse of the B operand for subtract functions.

Carry Chains

An arbitrary number of contiguous logic cells can be configured to realize an adder or subtracter function with ripple carry. **Figure 2.2.5** shows a series of logic cells configured as an adder.
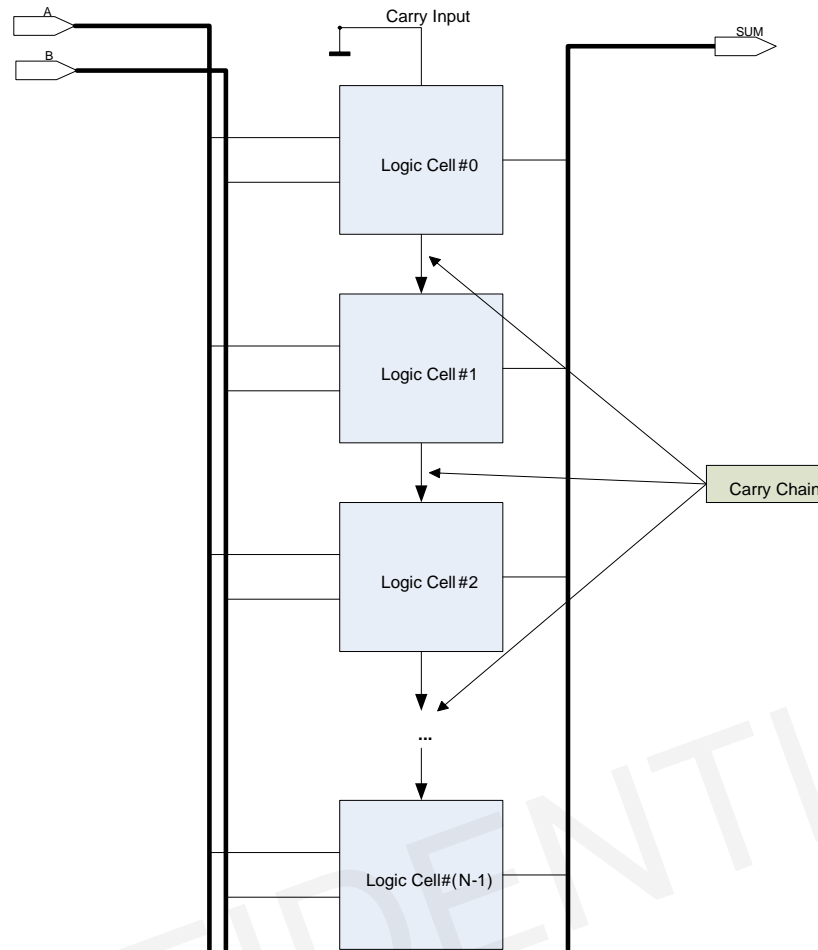
Figure2.2.5: FP Adder

Here, an N-length adder is configured where, at each logic cell, 2 of the 4 inputs to the LUT are allocated for the adder operands. The other 2 inputs should be configured to VDD to enable the operands. Specifically, input #0 or #1 can be configured to drive in operand A (the other input in the pair configured to VDD) and input #2 or #3 can be configured to drive in operand B (the other input in the pair configured to VDD also). The LUT pattern at each cell would be a function of the operands and the carry input to the logic cell (provided the cell is configured as SUM or SUB at either or both Dmuxes).

Function Generator

The Function Generator allows the logic cell to implement logic functions of more than the four or five basic logic signals that feed the LUT as described above. Each individual Function generator module can be configured to be AND, OR, XOR, or MUX. The two inputs for the AND, OR, and XOR gates are the LUT outputs as are the data inputs to the MUX. The "data4" input of the logic cell is used as the select input of the mux with the 0 select value choosing the "even" input and the 1 selecting the "odd" input. **Figure 2.2.6** describes an example of Dual logic cell functions: 8-input AND:
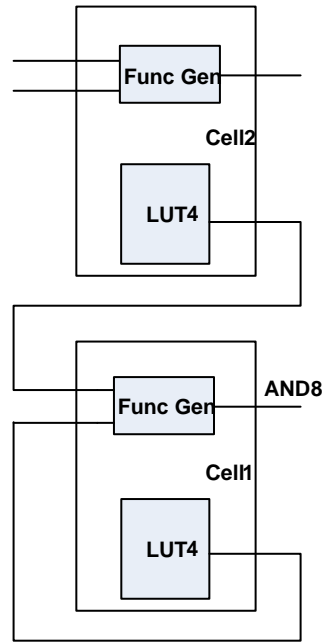
Figure 2.2.6 Dual logic cell function

Figure 2.2.7 shows how to combine to LUT5, LUT6, and LUT7.
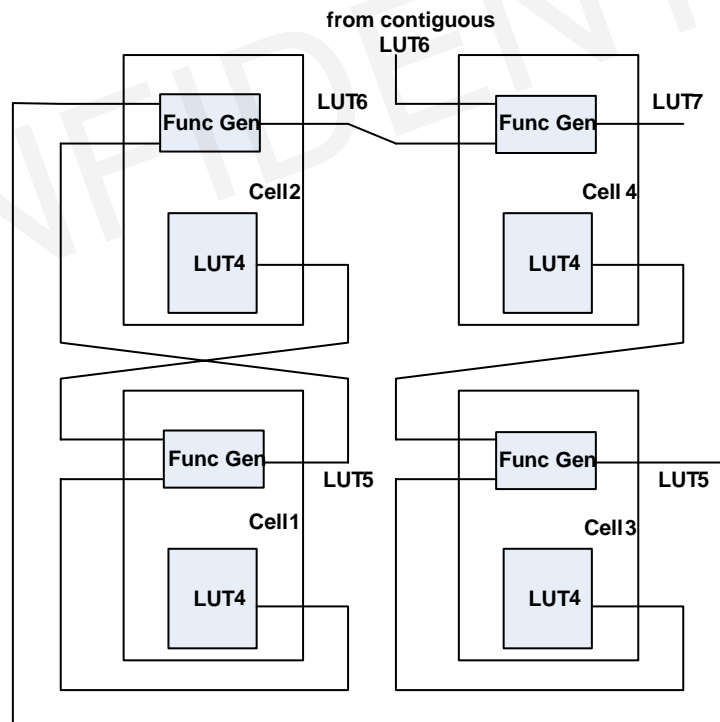
Figure 2.2.7 Combined LUTs

Table2.2.1 lists the multiple logic cells functions supported and the number of contiguous logic cells required.

Table 2.2.1 Multiple Logic Cell Functions	
Function	**Number of Logic Cells**
LUT5	2
LUT6	4
LUT7	8
LUT8	16
LUT9	32
LUT10	64
LUT11	128
LUT12	256
LUT13	512
LUT14	1024
AND8	2
OR8	2
XOR8	2

Wide LUT functions of up to 14 inputs are possible, which would max out the number of available logic cells to implement the function. In addition, there are 4 special logic functions that require 2 adjacent logic cells. The logic cell at the even position (if cells are numbered starting with 0 at one end of the routing tree) produces the function result and takes the AND, OR, XOR,or MUX of the LUT results from the 2 logic cells involved.

Shift Registers

An arbitrary number of contiguous logic cells can be configured to realize a shift register. Up to 2 independent shift registers can be configured across the same set of logic cells.

Figure 2.2.8 shows a pair of shift registers using all flip-flop resources in the logic cells involved.
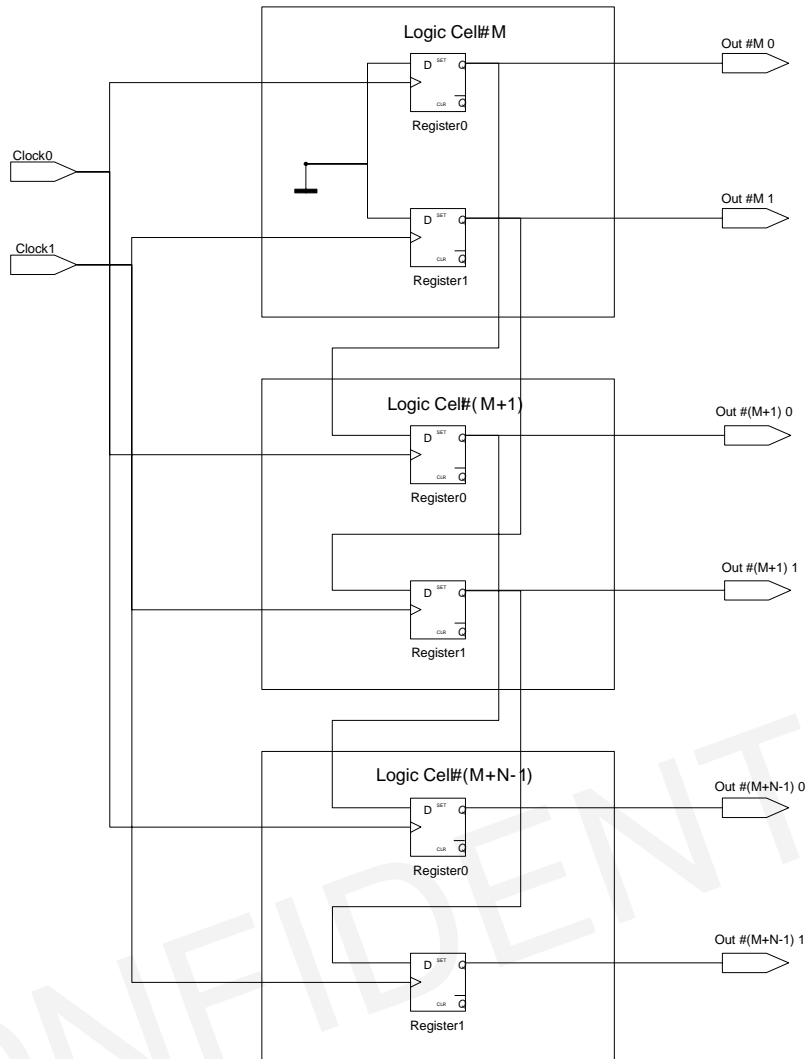
Figure 2.2.8 FP Shift Registers

In the pruned down diagram, the shift registers configured are each clocked by their own clocks, so each can shift data independently of the other. The shift registers are configured with their anchors (bit 0) at logic cell M (diagram shows simplified LUT configured as GND to pad 0's into the shift registers). Both are shown configured to length N, but they can be configured independently of each other. The Dmuxes and Qmuxes are not shown. Dmuxes would have to be configured to SHIFT to allow data from a previous cell to pass through the next. Qmuxes would have to be configured to DFF if the shifted values in the registers are to be used outside the shift registers.

In general, any logic cell can anchor a shift register. Each shift register can be of any length. It's also possible to wrap a shift register from the 4096th logic cell (cell #4095) back to the 1st logic cell (cell #0).

Clock Bundle Control logic

A clock control unit exists for every 16 logic cells. This unit contains configurable

muxes to select the source of the logic cell register clocks, resets, and enables for the 16 logic cells associated with it. **Figure 2.2.9** shows the logic composition of the clock control unit.
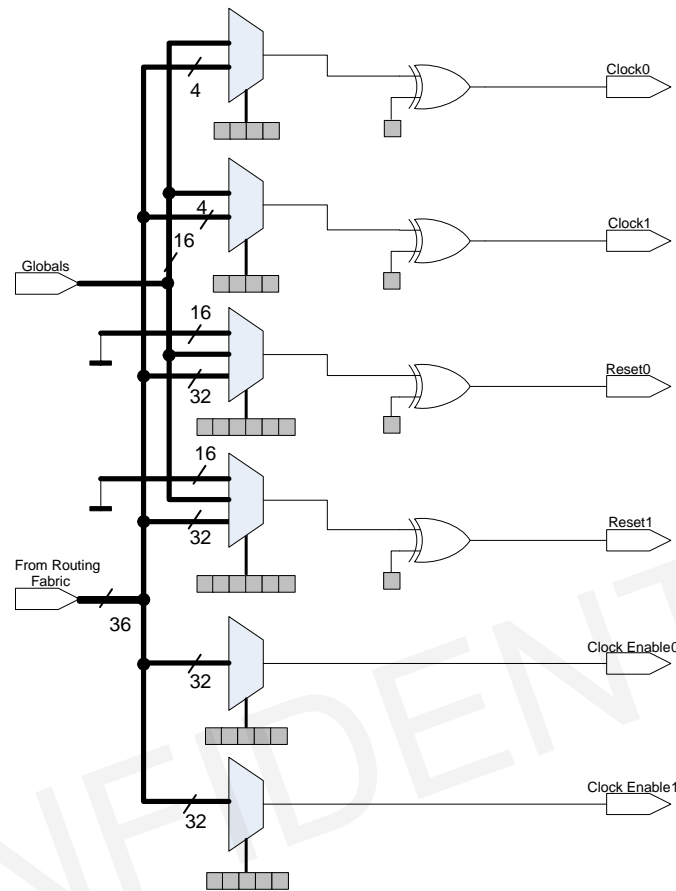
Figure 2.2.9 FP Clock Control

The squares in gray indicate configuration memory bits that control the selection of the clocks, resets, and enables to the logic cells as well as active logic level of the clocks and resets. The path0 clock, reset, and enables fan-out to 16 logic cells clustered near the clock control, driving the path0 registers in each of those cells. Likewise, the path1 clock, reset, and enables fan-out to those same logic cells but drive the path1 registers.

Each clock mux can be configured to select 1 out of 16 global signals and 4 routing fabric wires to use as logic cell register clocks. The same global can also be configured at each reset mux to use as logic cell register asynchronous resets. In addition, the reset muxes can select 1 out of 32 of the 36 available routing lines for resets generated by configured logic elsewhere in the core. The 16 upper-most selects at each reset mux are grounded. The clock enable muxes can select 1 out of 32 of the same 36 routing lines. The assignment of routing lines at each reset or clock enable mux varies.

Following each clock mux is an XOR gate that, under configuration, can reverse the polarity of the clock. By default, clocks are rising-edge triggering for DFF's and active

when its level is VDD for latches. If the configuration bit at the XOR gate is set, the clock at that point becomes falling-edge triggering or active low. Similarly, each reset mux is followed by an XOR under configuration control for determining the active logic level of the selected reset. By default, resets are active-high. If the configuration bit is set, the reset at that point becomes active-low. Clock enables are always active-high signals.

Routing Architecture

The FP core consists of an array of configurable logic cells and configurable routing muxes that interconnect the logic cells in a hierarchical architecture. The routing architecture resembles a tree where the logic cells are at the leaf nodes of the tree and the routing muxes are at all other nodes. Muxes propagating signals from the logic cells up the tree towards the apex are referred to as output (direction relative to logic cells) or up muxes. Muxes propagating signals towards the logic cells and away from the apex are referred to as input or down muxes.

Figure 2.2.10 illustrates the tree structure of the routing architecture.
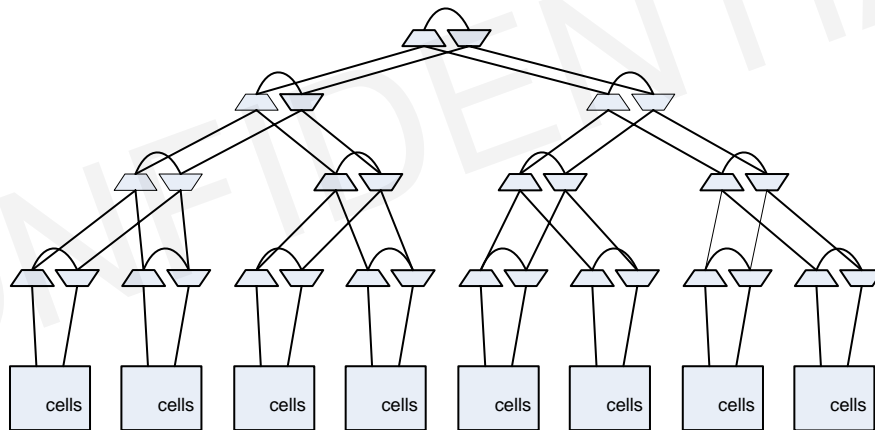
Figure 2.2.10 FP Routing Tree

The illustration provides a rough view of the routing architecture and how signals are propagated from logic cell to logic cell. Depending on the distance of the receiving cell from the sending cell, signals are driven from the sender onto the routing fabric, typically through some number of up muxes until turning at a node to a down mux (turns shown as arcs in the diagram), then traversing through the same number of down muxes until the receiver is reached. The specific details are much more elaborate than what **Figure 2.2.10** can show, but the diagram does show the basic idea of how logic is interconnected in the FP core.

Embedded Memory

Chapter 2.3   **Complete Datasheet**

The Flexera embedded memory consists of columns of RAM8K memory blocks. Each RAM8K block can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM.

The RAM8K blocks support the following features:

- 9,216RAM bits
- 250 MHz performance
- True dual-port memory
- Byte enable
- Parity bits
- Support the following DPRAM width configurations: 1×8k, 1×9k,2×4k, 4×2k, 8×1k, 9×1k, 16×512, 18×512,32×256, 36×256

Memory Modes

The RAM8K memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. RAM8K blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. **Figure 2.3.1** shows true dual-port memory.
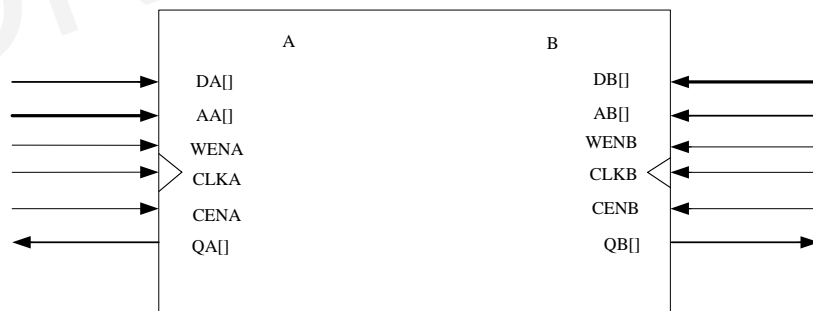
Figure 2.3.1 True Dual-port Memory Configuration

The following Tables summarize the ports and the function of True Dual-port Memory Configuration.

Table 2.3.1 shows the function of True Dual-port Memory Configuration.

Table 2.3.1 Function Table of True Dual-port Memory Configuration				
Inputs			Outputs	
CENA	WENA	CLK	Mem (AA)	QA
1	X	X	HOLD	0
0	1	↑	READ	DA
0	0	↑	WRITE	DA

Table 2.3.2 shows the function of True Dual-port Memory Configuration Ports.

Table 2.3.2 Ports of True Dual-port Memory Configuration		
Name	**Type**	**Description**
AA, AB	in	Port A (B) Address.
DA, DB	in	Port A (B) Data Input.
QA, QB	out	Port A (B) Data Output.
WENA, WENB	in	Port A (B) Write Enable. Data is written into the dual-port SRAM upon the rising edge of the clock when both WENA (WENB) and CENA (CENA) are low.
CENA, CENB	in	Port A (B) Enable. When CENA (CENB) is low and WENA (WENB) is high, data read from the dual-port SRAM address AA (AB) is available upon the next rising edge of CLKA (CLKB). If CENA (CENB) is high, QA (QB) retains its value.
CLKA, CLKB	in	Port A (B) Clock.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in ×1 mode at port A and read out in ×16 mode from port B.

The Flexera memory architecture can implement fully synchronous RAM by registering both the input and output signals to the RAM8K block. All RAM8K memory block inputs are registered, providing synchronous write cycles.

Parity Bit Support

The RAM8K blocks support a parity bit for each byte. The parity bit, along with internal FP Logic cell, can implement parity checking for error detection to ensure data integrity. You can also use parity-size data words to store user-specified control bits. Byte enables are also available for data input masking during write operations.

Memory Configuration Sizes

The memory address depths and output widths can be configured as $8,192 \times 1$, $9,216 \times 1$, $4,096 \times 2$, $2,048 \times 4$, $1,024 \times 8$ (or $1,024 \times 9$ bits), 512×16 (or 512×18 bits), and 256×32 (or 256×32 bits). Mixed-width configurations are also possible, allowing

different read and write widths. **Table 2.3.3** summarizes the possible RAM8K block configurations.

Table 2.3.3 RAM8K Block Configurations (True Dual-Port)										
Port A	**Port B**									
	8K ×1	**4K ×2**	**2K ×4**	**1K ×8**	**512 ×16**	**256 ×32**	**9 k ×1**	**1K ×9**	**512 ×18**	**256 ×36**
8K ×1	v	v	v	v	v	v				
4K ×2	v	v	v	v	v	v				
2K ×4	v	v	v	v	v	v				
1K ×8	v	v	v	v	v	v				
512 ×16	v	v	v	v	v	v				
256 ×32	v	v	v	v	v	v				
9K ×1							v	v	v	v
1K ×9							V	v	v	v
512 ×18							V	v	v	v
256 ×36							V	v	v	v

Byte Enables

RAM8K blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value.

Table 2.3.4 summarizes the byte selection.

Table 2.3.4 Byte Enable for RAM8K Blocks		
byteena[3..0]	**datain ×18**	**datain ×36**
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	–	[26..18]
[3] = 1	–	[35..27]

Global Clock Network, PLL &DLL

Flexera devices provide up to 16 global clocks and up to 2 PLLs. And they also provide up to 4 DLLS, one of which is used for hardware DDR controller IP.

Global Clock Network

There are 16 global clocks, driven by dedicated clock pins, userclk pin, PLL outputs, DLL0 outputs, FP logic cells. Flexera devices provide four dedicated clock pins, two pins on the left side and two pins on the right side.

Global clock network provides clock for FP, Embedded DPRAM, IOC, and 8051 Hardware IP. It also provides DQ read-write clock for hardware DDR controller IP. Global clock can be of clock control signal for FP, such as clock signal and reset signal of FP register. At the same time, global clock, asynchronous reset signal, and clock enable signal also can be driven form FP internal logic.

Figure 2.4.1 shows the global clock network of Flexera devices.
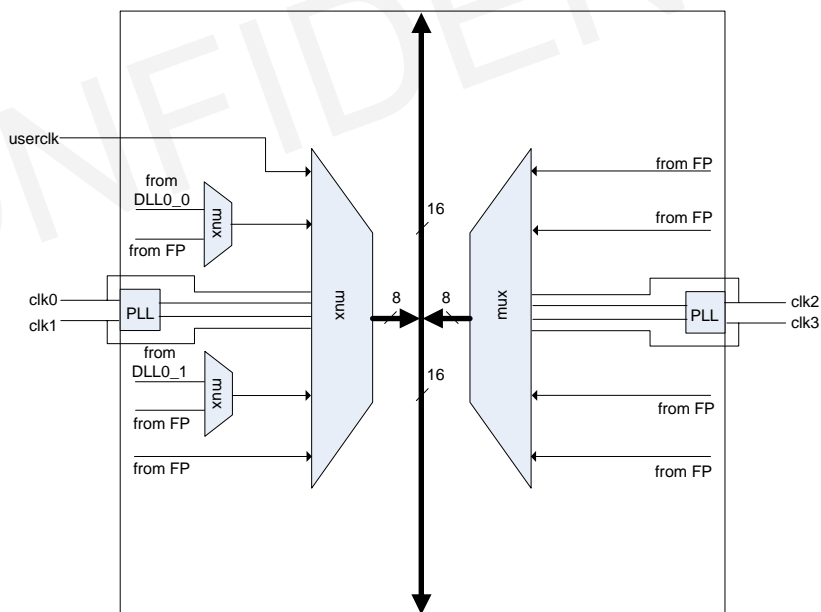
Figure 2.4.1 Global Clock Network

Global Clock for IO

Flexera Devices provide four IO Banks. BANK1 and BANK3 IO have two clock domains, but BANK2 and BANK4 are divided into three clock domains. All the clock domains are from Global clock network shown as **Figure 2.4.2**:
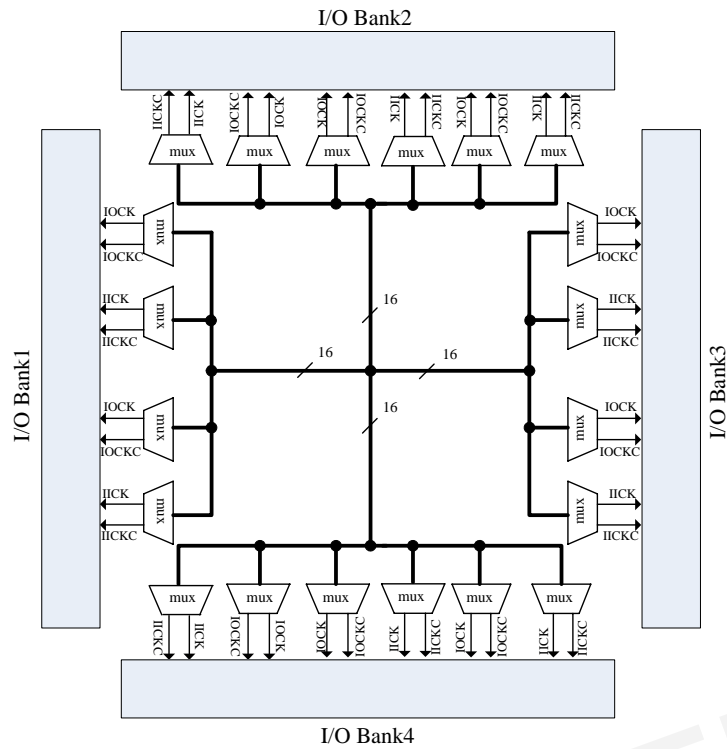
Figure 2.4.2 Clock for IO

Flexera Devices provide dedicated clock domain for DQ and DQS IOS of DDR to support read-write function of hardware DDR controller IP DQ signal. **Figure 2.4.3** shows the clock for DDR IO.
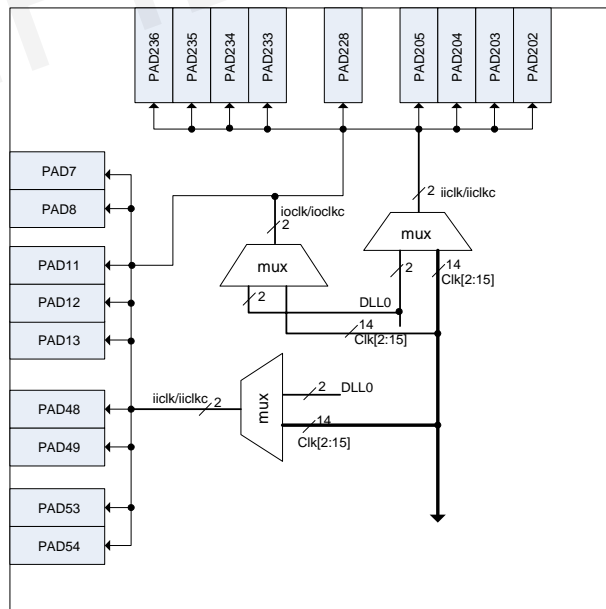
Figure 2.4.3 CLOCK for DDR IO

Global Clock for Embedded DPRAM

There are 10 embedded 9K DPRAMs in Flexera Devices. Each DPRAM has a different

clock domain. Diagram of clock for embedded memory shown as **Figure 2.4.4**.
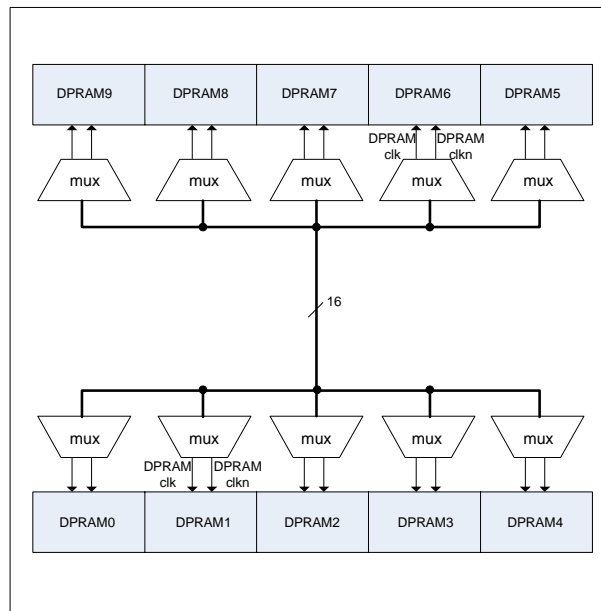
Figure 2.4.4 CLOCK for DPRAM

PLLs

Flexera PLLs provide general-purpose clocks with clock multiplication and phase shifting as well as outputs for differential I/O support. Flexera devices contain two PLLs.

Table 2.4.1 shows the PLL features in Flexera devices. **Figure 2.4.5** shows Flexera PLL.

Table 2.4.1 PLL Features	
parameter	**value**
VCO output frequency range	100MHz - 500MHz
Reference divider values	1-64
Feedback divider values	1-4096
Output divider values	1-64
Output phase separation	6.25% output cycle

This is the Flexera PLLs diagram.
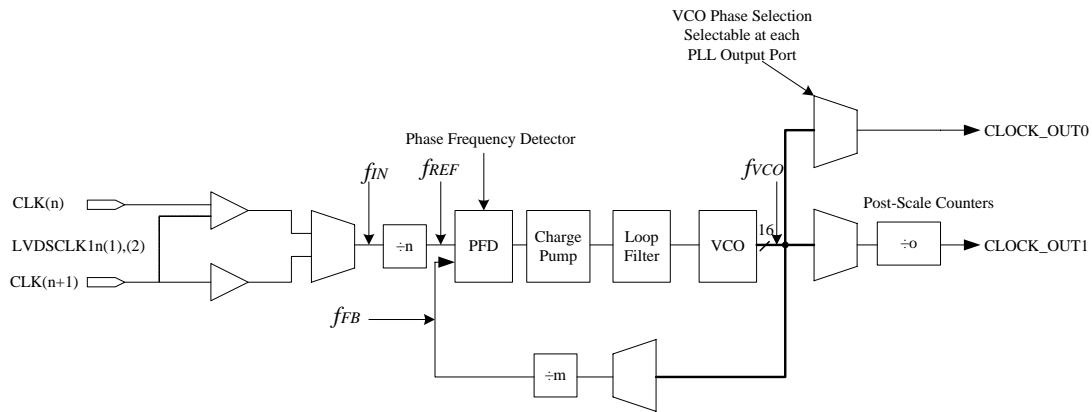
Figure 2.4.5 Flexera PLL

Clock Multiplication & Division

Flexera PLLs provide clock synthesis for PLL two output ports, port1 $m/ (n \times p)$ scaling factors, port2 using m/n scaling factors. The input clock is divided by a reference divider, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Port1 has a post-scale counter to divide down the high-frequency VCO, so the frequency of port1 divided by a post-scale divider, p. For multiple PLL outputs with different frequencies, the VCO is set to the least-common multiple of the output frequencies that meets its frequency specifications.

Each PLL has one reference divider, n, that can range in value from 1 to 64. Each PLL also has one multiply divider, m, which can range in value from 1 to 4096. The pose-scale divider, p of port1 has a value range from 1 to 64.

Phase Shifting

Each output port of Flexera PLLs supports 4 bits phase shifting simultaneity: With 6.25% VCO output period and output frequency 500MHZ, the output phase accuracy is +/-2.5%.

PLL Control Signals

There are four control signals: RESET，PWRDN，BYPASS, and FASTEN. You can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low-power applications.

When the RESET signal is high, the PLL counter will reset, clearing the PLL output and placing the PLL out of lock. And it will be in resting mode when PWRDN is driven high. PLL signal will be bypassed if BYPASS goes high. At this time, the output signal equals the input signal. When FASTEN is set to high, fast clock will be enable port, it enables and disables PLLs.

DLLs

Flexera Devices contain four DLLs, one is used to drive global clock network, which provides DQ read-write clock for hardware DDR controller IP, and others connect the inputs and outputs for FP.

Table 2.4.2 shows the DLL features in Flexera devices. **Figure 2.4.6** shows Flexera DLLs.

Table 2.4.2 DLL Features	
parameter	**value**
Reference input frequency range	100MHz - 500MHz
Slave delay adjustment range	0% - 100% of reference cycle
Slave delay adjustment resolution	1.25% of reference cycle
Number of slave adjustment steps	80 (7 bits)
Number of slaves	2 / cluster

Follow is the DLL diagram of Flexera devices.
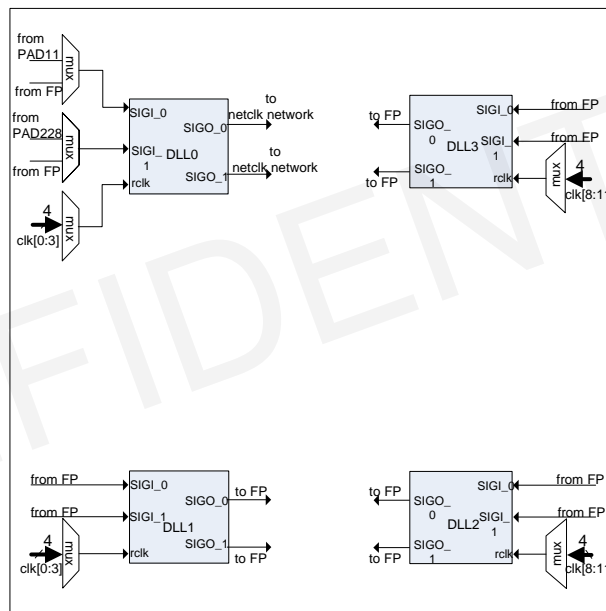
Figure 2.4.6 Flexera DLLs

Table 2.4.3 gives the detail information of connection relationship for DLL signal.

Table 2.4.3 Signal connection of DLL （part i）			
DLL0_SIGI_0	From PAD11 or From FP	DLL0_SIGO_0	To Global clk network
DLL0_SIGI_1	From PAD228 or From FP	DLL0_SIGO_1	To Global clk network
DLL1_SIGI_0	From FP	DLL1_SIGO_0	To FP
DLL1_SIGI_1	From FP	DLL1_SIGO_1	To FP

Table 2.4.3 Signal connection of DLL (part *ii*)			
DLL2_SIGI_0	From FP	DLL2_SIGO_0	To FP
DLL2_SIGI_1	From FP	DLL2_SIGO_1	To FP
DLL3_SIGI_0	From FP	DLL3_SIGO_0	To FP
DLL3_SIGI_1	From FP	DLL3_SIGO_1	To FP

Every DLL has two absolute inputs, and each signal has independent phase-shift control. There are 80 pats in phase shifting, and every pat will be 1.25% of the reference input clock cycle. Each DLL route contains phase-shift control register with seven bits, the phase-shift value is adj[6:0] × Tref /80. For example, if phase-shift control register is set to twenty, phase shifting will be a quarter of the reference clock cycle.

DLL Control Signals

DLL has two control signals: RESET and PWRDN. When RESET goes high, DLL will be reset. When PWREN is driven to high, DLL will be in resting mode.

I/O Structure

Chapter 2.5   **Complete Datasheet**

Features

Flexera Input/Output Cells (IOCs) support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- True DDR I/Os

Flexera device IOCs contains a bidirectional I/O buffer and six registers for complete embedded bidirectional single or dual data rate transfer.

Figure 2.5.1 shows the Flexera IOC structure. The IOC contains 4 output registers (two output registers, and two output enable registers).built-in clocked output mux, clocked enable mux, and a dual-edge clocked input register pair for DDR use. All IO's also can be configured as either registered or asynchronous.
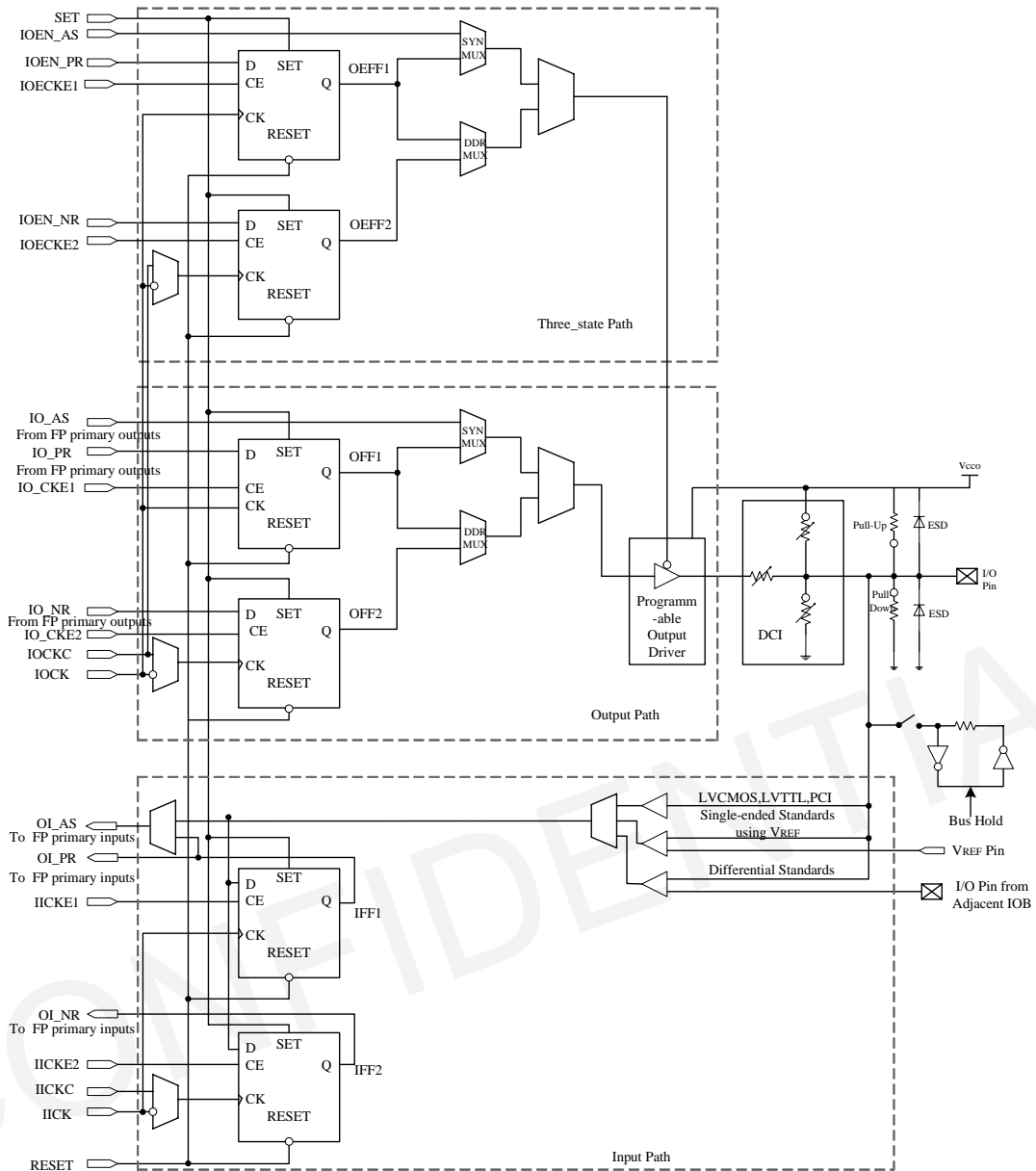
Figure 2.5.1 Simplified IOC Diagram

Note:

(1) All IOC signals communicating with the FPGA's internal logic have the option of inverting polarity.

Programmable Drive Strength

The output buffer for each Flexera device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL-2 class I and II, SSTL-18 class I and II, HSTL-18 class I and II, and HSTL-1.5 class I and II standards have several levels of drive strength that you can control. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2.5.1 shows the possible settings for the I/O standards with drive strength control.

Table 2.5.1 Programmable Drive Strength	
I/O Standard	**IOH/IOLCurrent Strength Setting (mA)**
	Top & Bottom I/O Pins
LVTTL (3.3 V)	4
	8
	12
	16
LVCMOS (3.3 V)	4
	8
	12
	16
LVTTL/LVCMOS (2.5 V)	4
	8
	12
LVTTL/LVCMOS (1.8 V)	4
	8
	12
LVCMOS (1.5 V)	4
	8

Note:

(1) The default current in the Flexera software is the maximum setting for each I/O standard.

Slew Rate Control

Slew rate control is performed by using programmable output drive strength.

Bus Hold

Each Flexera device user I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than VCCIO to prevent overdriving signals.

If the bus-hold feature is enabled, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals. Bus hold circuitry is not available on the dedicated clock pins.

The bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

I/O Standard Support

Table 2.5.2 shows the single-ended I/O standards supported by Flexera devices.

Table 2.5.2 Flexera Supported I/O Standards (Single-Ended)					
Standards	VCCO (V)	VREF (V)	Termination Voltage (V)	Max. Speed (MHz)	DCI Termination Type
LVTTL	3.3	N/A	N/A	300	N/A
PCI	3.3	N/A	N/A	66	N/A
PCI-X	3.3	N/A	N/A	133	N/A
LVCMOS33	3.3	N/A	N/A	300	serial
LVCMOS25	2.5	N/A	N/A	300	serial
LVCMOS18	1.8	N/A	N/A	250	serial
LVCMOS15	1.5	N/A	N/A	200	N/A
SSTL-3	3.3	1.5	1.5	200	shunt
SSTL-2	2.5	1.25	1.25	200	shunt
SSTL-18	1.8	0.9	0.9	267	shunt
HSTL-18	1.8	0.9	0.9	300	shunt
HSTL-15	1.5	0.9	0.9	300	shunt
HSTL-15B	1.5	0.75	0.75	300	shunt
GTL	Term.	0.8	-	100	N/A
GTLP	Term.	1.0	-	100	N/A
Cardbus	3.3	N/A	N/A	33	N/A
AGP-2X	3.3	N/A	N/A	66	N/A

Table 2.5.3 shows the differential I/O standards supported by Flexera devices.

Table 2.5.3 Flexera Supported I/O Standards (Differential)					
Standards	VCCO (V)	Vdout (V)	Termination Voltage (V)	Max. Speed (MHz)	DCI Termination Type
LVDS	2.5	0.25-0.40	N/A	500	shunt
Hyper Transport (ULVDS?)	2.5	0.5-0.7	N/A	800	shunt
LVPECL	2.5	0.49-1.22	N/A	450	N/A
RSDS	3.3	1.2	N/A	65	N/A
DHSTL-15	1.5	-	N/A	300	shunt
DSSTL-18	1.8	-	N/A	267	shuntl

MultiVolt I/O Interface

The Flexera architecture supports the MultiVolt I/O interface feature, which allows Flexera devices in all packages to interface with systems of different supply voltages. Flexera devices have one set of VCC pins (VCCINT) that power the internal device logic array and input buffers that use the LVPECL, LVDS, HSTL, or SSTL I/O standards. Flexera devices also have four or eight sets of VCC pins (VCCIO) that power the I/O output drivers and input buffers that use the LVTTL, LVCMOS, or PCI I/O standards.

The Flexera VCCINT pins must always be connected to a 1.2-V power supply. If the VCCINT level is 1.2 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems).When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V systems. **Table 2.5.4** summarizes Flexera MultiVolt I/O support.

Table 2.5.4 Flexera MultiVolt I/O Support								
V_{CCIO}(V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
1.5	v	v	v	v	v			
1.8	v	v	v	v	v	v		
2.5			v	v	v	v	v	
3.3			v	v	v	v	v	v

Configuration

The FP logic cells of Flexera family devices use SRAM cells to store configuration data. Since SRAM memory is volatile, configuration data must be downloaded to Flexera device each time the device powers up. You can download configuration data to Flexera devices using the SPI, or JTAG interfaces (see **Table 3.1**).

Table 3.1 Flexera APGA Configuration Schemes	
Configuration Scheme	**Description**
Active serial (AS)/SPI master configuration	Configuration using: ●Industry-standard SPI serial flash
Passive serial (PS)/SPI slave configuration	Configuration using: ●Intelligent host (microprocessor)
JTAG-based configuration	Configuration via JTAG pins using: ● Download cable ● Intelligent host (microprocessor)

You can select a Flexera device configuration scheme by driving its MODE1 and MODE0 pins either high (1) or low (0), as shown in **Table 3.2**.If your application only requires a single configuration mode, the MODE pins can be connected to VCC (the I/O bank's VCCIO voltage where the MODE pin resides) or to ground. If your application requires more than one configuration mode, the MODE pins can be switched after the APGA has been configured successfully. Toggling these pins during user mode does not affect the device operation. However, the MODE pins must be valid before initiating reconfiguration.

Table 3.2 Selecting Flexera Configuration Schemes		
MODE1	**MODE0**	**Configuration Scheme**
0	0	Active serial/SPI master
0	1	Passive serial (PS)/SPI slave
0	×	JTAG

Note:
(1) Do not leave MODE pins floating. Connect them to a low- or high-logic level. These pins support the non-JTAG configuration scheme used in production. If your design only uses JTAG configuration, you should connect the MODE0 pin to VCC.

You can configure Flexera devices using the 3.3-, 2.5-, 1.8-, or 1.5-V LVTTL I/O standard on configuration and JTAG input pins. These devices do not feature a VCCSEL pin; therefore, you should connect the VCCIO pins of the I/O banks containing configuration or JTAG pins according to the I/O standard specifications.

Configuration Schemes

This section describes the various configuration schemes you can use to configure

Flexera devices. Descriptions include an overview of the protocol, pin connections, and timing information. The schemes discussed are:

- AS configuration/SPI master(serial devices) configuration
- PS configuration/SPI slave configuration
- JTAG-based configuration

Active Serial/SPI Configuration (SPI serial Devices)

In the AS configuration scheme, Flexera devices are configured using the industry-standard SPI serial devices. These configuration devices are low cost devices with non-volatile memory that feature a simple few pin interface and a small form factor. These features make serial configuration devices an ideal solution for configuring the low-cost Flexera devices.

Serial configuration devices provide a serial interface to access configuration data. During device configuration, Flexera devices read configuration data via the serial interface, and configure their SRAM cells. This scheme is referred to as an AS configuration scheme because the device controls the configuration interface.

Serial configuration devices have a several pins interface: serial clock input (SCLK), serial data output (SDO), serial data input (SDIN), and an active low chip select (CSn), and a hold signal (Holdn). This pin interface connects to Flexera pins as shown in **Figure 3.1**.
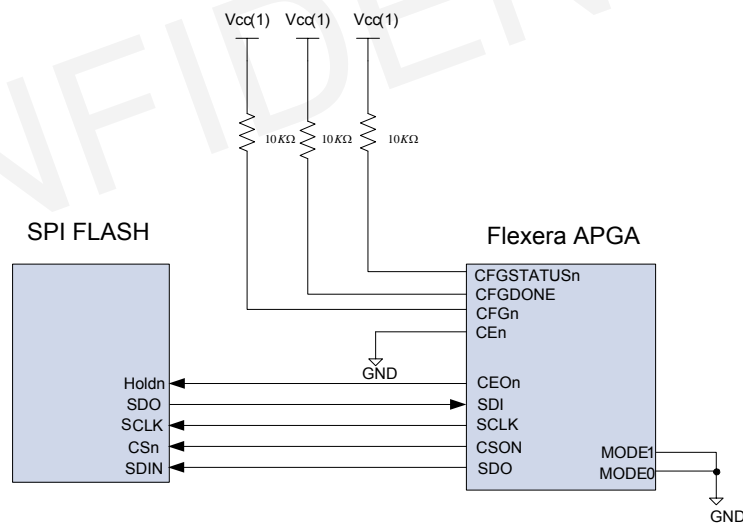
Figure 3.1 AS/SPI master Configuration of a Single Flexera device
Notes:
(1) Connect the pull-up resistors to a 3.3-V supply.
(2) Flexera devices use the SDO to SDIN path to control the configuration device. Connecting the MODE [1...0] pins to00 select the AS/SPI master configuration scheme. The Flexera chip enable signal, CEn, must also be connected to ground or driven low for successful configuration.

During system power up, both the Flexera and serial configuration device enter a power-on reset (POR) period. As soon as the Flexera device enters POR, it drives low to indicate it is busy and drives CFGDONE low to indicate that it has not been configured. After POR, which typically lasts 100 ms, the Flexera device releases and

enters configuration mode when this signal is pulled high by the external $10\text{-}k\Omega$ resistor. Once the APGA successfully exits POR, all user I/O pins are tri-stated. Flexera devices have weak pull-up resistors on the user I/O pins which are on before and during configuration.

Flexera devices support the 0X03 READ commands or the 0X0B FAST READ commands. **Table 3.3** lists the SPI serial flash vendor.

Table 3.3 SPI serial flash vendor	
Vender	**Device Family**
ST Microelectronics	M25P
NexFLASH	NX25P
Silicon storage Technology	SST25VF
Macronix	MX25LXXXX
Spansion	S25FL
PMC	Pm25LV
Atmel	AT25F

Passive serial (PS)/SPI slave configuration

In the PS scheme, an external host (configuration device, embedded processor, or host PC) controls configuration.

Before configuration begins, the configuration device goes through a POR delay of up to 100 ms (maximum) to allow the power supply to stabilize. You must power the Flexera devices before or during the POR time of the enhanced configuration device. During POR, this process is similar with the AS configuration. **Figure 3.2** shows the PS/SPI slave configuration of a single Flexera device.
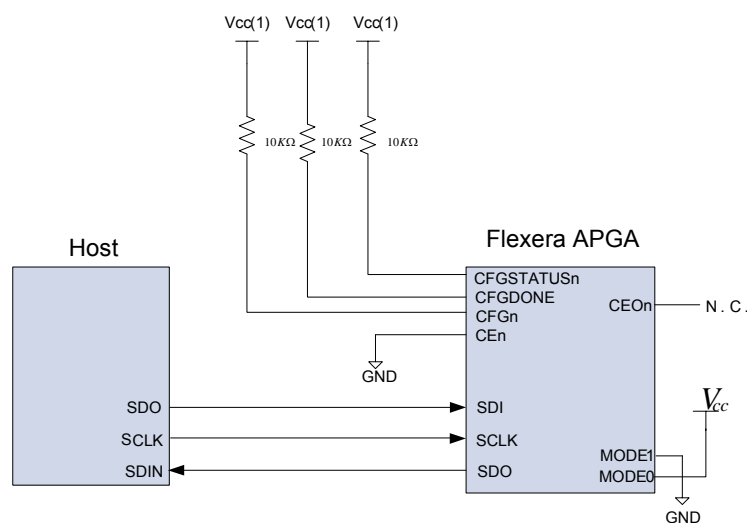
Figure 3.2 PS/SPI slave Configuration of a Single Flexera device

JTAG-Based Configuration

JTAG has developed a specification for boundary-scan testing. This boundary-scan test (BST) architecture offers the capability to efficiently test components on printed circuit boards (PCBs) with tight lead spacing. The BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. You can also use the JTAG circuitry to shift configuration data into Flexera devices.

Flexera devices are designed such that JTAG instructions have precede CEn over any device operating modes. So JTAG configuration can take place without waiting for other configuration to complete (e.g. configuration with serial or enhanced configuration devices). If you attempt JTAG configuration in Flexera devices during non-JTAG configuration, non-JTAG configuration is terminated and JTAG configuration is initiated.

A device operating in JTAG mode uses four required pins: TDI, TDO, TMS, and TCK. Flexera devices do not support the optional TRST pin. The three JTAG input pins, TCK, TDI, and TMS, have weak internal pull-up resistors, whose values are approximately 20 to $40^{k\Omega}$. All user I/O pins are tri-stated during JTAG configuration. **Table 3.4** shows each JTAG pin's function.

Table 3.4 JTAG Pin Descriptions		
Pin	**Description**	**Function**
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to VCC.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the Test Access Port (TAP) controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to VCC.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled, by connecting this pin to GND.

JTAG Configuration Using a Download Cable

During JTAG configuration, data is downloaded to the device on the board through download cable. Configuring devices through a cable is similar to programming devices in-system. See **Figure 3.3** for pin connection information.
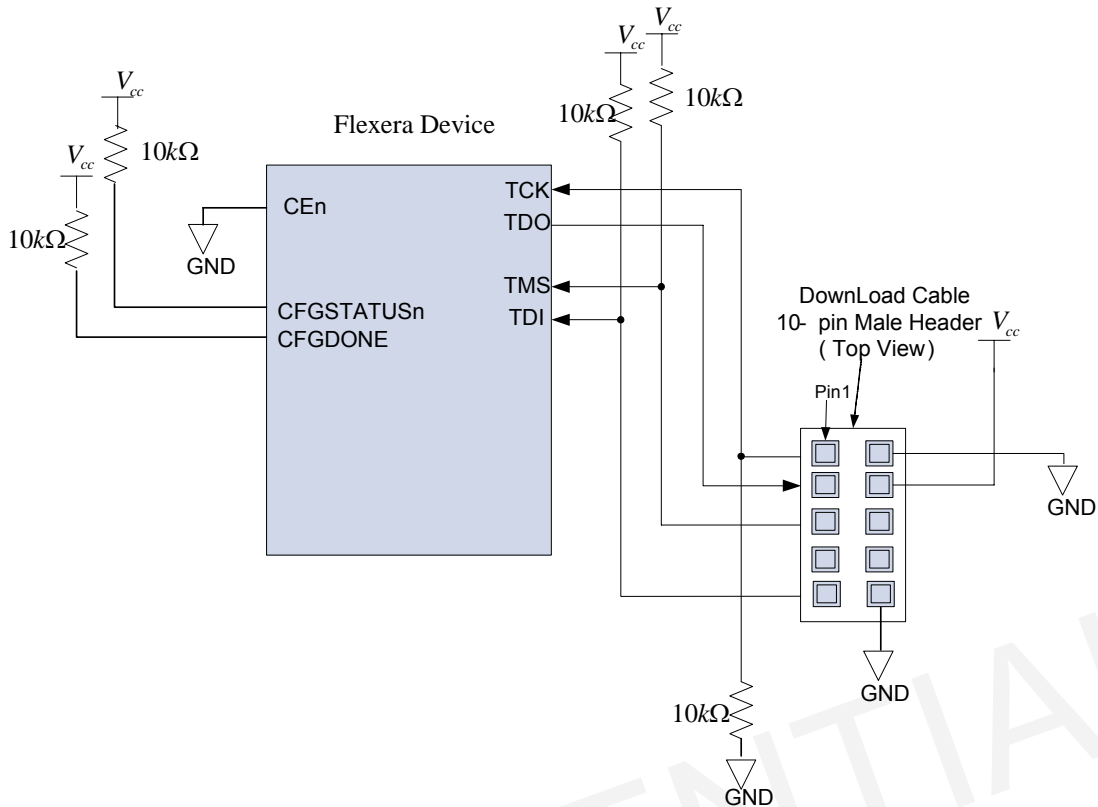
Figure 3.3 JTAG Configuration of Single Flexera device
Notes:
(1) You should connect the pull-up resistor to the same supply voltage as the
    download cable.
(2) You should connect the CFGn, MSEL0, and MSEL1 pins to support a non-JTAG
    configuration scheme. If you only use JTAG configuration, connect CFGn to VCC,
    and MSEL0 and MSEL1 to ground. Pull SDIN and SCLK to high or low.
(3) CEn must be connected to GND or driven low for successful configuration.

If V_{CCIO} is tied to 3.3-V, both the I/O pins and the JTAG TDO port drive at 3.3-V levels.

Flexera devices have dedicated JTAG pins. Not only can you perform JTAG testing on Flexera devices before and after, but also during configuration. While other device families do not support JTAG testing during configuration, Flexera devices support the BYPASS, IDCODE, and SAMPLE instructions during configuration without interrupting configuration. All other JTAG instructions may only be issued by first interrupting configuration and reprogramming I/O pins using the CONFIG_IO instruction.

The CONFIG_IO instruction allows I/O buffers to be configured via the JTAG port, and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Flexera device or waiting for a configuration device to complete configuration. OCEn configuration has been interrupted and JTAG testing is complete, the part must be reconfigured via JTAG (PULSE_CONFIG instruction) or by pulsing CFGn low.

The chip-wide reset and output enable pins on Flexera devices do not affect JTAG boundary-scan or programming operations. Toggling these pins does not affect JTAG

operations (other than the usual boundary-scan operation).

When designing a board for JTAG configuration of Flexera devices, you should consider the dedicated configuration pins. **Table 3.5** shows how you should connect these pins during JTAG configuration.

Table 3.5 Dedicated Configuration Pin Connections During JTAG Configuration	
Signal	**Description**
CEn	Drive all Flexera devices in the chain low by connecting CEn to ground, pulling it down via a resistor, or driving it low by some control circuitry. For devices in a multi-device PS and AS configuration chains, connect the CEn pins to ground during JTAG configuration or configure them via JTAG in the same order as the configuration chain.
CEnO	For all Flexera devices in a chain, the CEnO pin can be left floating or connected to the CEn pin of the next device. See CEn description above.
CFGSTATUSn	Pulled to VCC through a 10-kΩresistor. When configuring multiple devices in the same JTAG chain, pull up each CFGSTATUSn pin to VCC individually. *(1)*
CFGDONE	Pulled to VCC through a 10-kΩresistor. When configuring multiple devices in the same JTAG chain, pull up each CFGDONE pin to VCC individually. The CFGDONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize. *(1)*
CFGn	Driven high by connecting to VCC, pulling up through a resistor, or driving it high by some control circuitry.
MODE0, MODE1	Do not leave these pins floating. These pins support whichever non-JTAG configuration is used in production. If only JTAG configuration is used, you should tie these pins to ground.
SCLK	Do not leave these pins floating. Drive low or high, whichever is more convenient.
SDIN	Do not leave these pins floating. Drive low or high, whichever is more convenient.

Note:
(1) CFGSTATUSn going low in the middle of JTAG configuration indicates that an error has occurred; CFGDONE going high at the end of JTAG configuration indicates successful configuration.

Combining Configuration Schemes

This section shows you how to configure Flexera devices using multiple configuration schemes on the same board.

Active Serial/SPI & JTAG

You can combine the AS/SPI configuration scheme with JTAG-based configuration. When Setting the MODE [1...0] pins to 01, you can use JTAG interface to configure the Flexera device. The SPI serial flash also can be programmed in system using JTAG interface. When setting the MODE [1...0] pins to 01, configuration data for FP core is loaded from SPI flash.
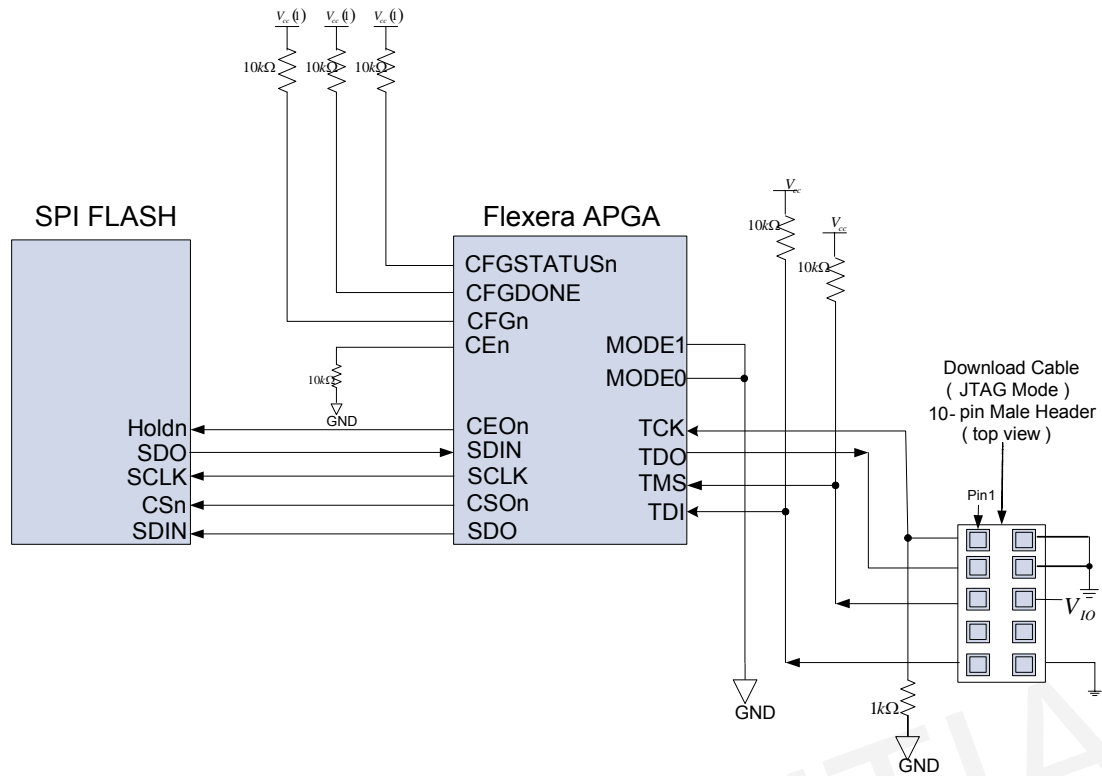
Figure 3.4 Combining AS &JTAG Configuration
Note:
(1) Connect these pull-up resistors to 3.3 V.

Device Configuration Pins

Table3.6 to **Table3.7** describes the connections and functionality of all the configuration related pins on the Flexera device. **Table 3.6** describes the dedicated configuration pins. These pins are required to be connected properly on your board for successful configuration. Some of these pins may not be required for your configuration schemes.

Table 3.6 Dedicated Flexera Device Configuration Pins				*(part i)*
Pin Name	**User Mode**	**Configuration Scheme**	**Pin Type**	**Description**
MODE1 MODE0	–	All	Input	Dedicated mode select control pins for the configuration mode for the device: 00 Reserved, 01 JATG, 10 SERIAL (ACTIVE), 11 Test Mode.
CFGn	–	All	input (Global Reset)	Dedicated configuration control pin. A low transition resets the target device; a low-to-high transition begins configuration. ALL I/O pins tri-state when CFGn is driven low .This pin can be used as Global Reset (Active Low)
SDIN	–	All	Input	Dedicated configuration data input pin. Data input. In serial configuration mode, bit-wide configuration data is presented to the target device on the SDINpin. Toggling SDINafter configuration does not affect the configured device. This pin uses Schmitt trigger input buffers
CEOn	–	All	Output	Output that drives low when device configuration is complete. During multi device configuration, this pin feeds a subsequent CEn device's CEn pin.

Table 3.6 Dedicated Flexera Device Configuration Pins   (part *ii*)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
CEn	–	All	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When CEn is low, the device is enable and high when it is disabling.
CFGSTAT USn	–	All	Bidirection al open-drain	This is a dedicated configuration status pin , not user I/O The device drives CFGSTATUSn low immediately after power-up and releases it within 5 μs. (When using a configuration device, the configuration device holds CFGSTATUSn low for up to 200 ms.) Status output. If an error occurs during configuration, CFGSTATUSn is pulled low by the target device. Status input. If an external source drives the CFGSTATUSn pin low during configuration or initialization, the target device enters an error state. Driving CFGSTATUSn low after configuration and initialization does not affect the configured device. If the design uses a configuration device, driving CFGSTATUSn low causes the configuration device to attempt to configure the FPGA, but siCEn the FPGA ignores transitions on CFGSTATUSn in user-mode, the FPGA does not reconfigure. To initiate a reconfiguration, CFGSTATUSn must be pulled low. This pin uses Schmitt trigger input buffers
CFGDON E	–	All	Bidirection al open-drain	This is a dedicated configuration status pin , not user I/O Status output. The target device drives the CFGDONE pin low before and during configuration. OCEn all configuration data is received without error and the initialization clock cycle starts, the target device releases CFGDONE. Status input. After all data is received and CFGDONE goes high, the target device initializes and enters user mode. Driving CFGDONE low after configuration and initialization does not affect the configured device. This pin uses Schmitt trigger input buffers
SCLK	–	AS	input(PS mode) , output (AS mode)	In passive serial configuration mode, SCLK is a clock input used to clock configuration data from external device source into CLD device. In active serial configuration mode, SCLK is a clock output from CLD device. (The CLD is a master in this mode). This is a dedicated pin used for configuration.
SDO	I/O in PS mode, N/A in AS mode	AS	I/O, Output	Active serial data output from the CLD device. In passive serial configuration, this pin becomes user I/O pin.
CSOn	I/O in PS mode, N/A in AS mode	AS	I/O, Output	Chip select output to enable/disable a serial configuration device. This output is using during active serial configuration mode. In passive serial configuration mode this pin become user I/O.

Table 3.7 describes the optional configuration pins. During configuration, these pins function as user I/O pins and are tri-stated with weak pull-ups.

Table 3.7 Optional Flexera Device Configuration Pins			
Pin Name	**User Mode**	**Pin Type**	**Description**
USERCLK	N/A if option is on, I/O if option is off	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as user I/O pine after configuration.
INTDONE	N/A if option is on, I/O if option is off	I/O, Output open-drain	When enable, this pin indicates the device enter the user mode. This pin can be used as a user I/O pin after configuration.
CLD_OE	N/A if the option is on, I/O if the option is off.	I/O, Input	When this pin is low all I/O are tri-stated, When it is high all I/O pins behave as define in the design.
CLD_CLRn	N/A if the option is on, I/O if the option is off.	I/O, Input	When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as define in the design. This pin can be used as Device Reset. (Active Low)

Table 3.8 describes the dedicated JTAG pins. JTAG pins must be kept stable before and during configuration to prevent accidental loading of JTAG instructions.

Table 3.8 Dedicated JTAG Pins			
Pin Name	**User Mode**	**Pin Type**	**Description**
TDI	N/A	Input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to VCC. This pin uses Schmitt trigger input buffers
TDO	N/A	Output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected.
TMS	N/A	Input	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to VCC. This pin uses Schmitt trigger input buffers
TCK	N/A	Input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to ground. This pin uses Schmitt trigger input buffers

DC Characteristics

Operating Conditions

Flexera devices are offered in both commercial and industrial grades. Commercial devices are offered in -6 (fastest), -7, -8 speed grades.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the parameter values in this chapter apply to all Flexera devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades. All parameters representing voltages are measured with respect to ground.

Table 4.1 provides information on absolute maximum ratings.

Table 4.1 Flexera Device Absolute Maximum Ratings					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
VCCINT	Supply voltage	With respect to ground	–0.5	1.8	V
VCCIO	Output supply voltage		–0.5	4.6	V
VIN	DC input voltage *(3)*		–0.5	4.6	V
IOUT	DC output current, per pin		–25	40	mA
TSTG	Storage temperature	No bias	–65	150	°C
TJ	Junction temperature	BGA packages under bias		125	°C

Notes:
(1) Conditions beyond those listed in this table cause permanent damage to a device. These are stress ratings only. Functional operation at these levels or any other conditions beyond those specified in this chapter is not implied. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device reliability.
(2) During transitions, the inputs may over shoot to the voltage based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transition, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 4.2 specifies the recommended operating conditions for Flexera devices. It shows the allowed voltage ranges for VCCINT, VCCIO, and the operating junction temperature (TJ). The LVTTL and LVCMOS inputs are powered by VCCIO only. The LVPECL input buffers on dedicated clock pins are powered by VCCINT. The SSTL, HSTL, LVDS input buffers are powered by both VCCINT and VCCIO.

Table 4.2 Recommended Operating Conditions					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
V_{CCINT}	Supply voltage for internal logic and input buffers	(1)	1.15	1.25	V
V_{CCIO} (2)	Supply voltage for output buffers, 3.3-V operation	(1)	3.135 (3.00)	3.465 (3.60) (3)	V
	Supply voltage for output buffers, 2.4-V operation	(1)	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	(1)	1.71	1.89	V
	Supply voltage for output buffers, 1.4-V operation	(1)	1.425	1.575	V
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	−40	100	°C

Notes:
(1) The maximum VCC (both VCCIO and VCCINT) rise time is 100 ms, and VCC must rise monotonically.
(2) The VCCIO range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended VCCIO range specific to each of the single-ended I/O standards is given in **Table 4.4**, and those specific to the differential standards is given in **Table 4.7**.
(3) The minimum and maximum values of 3.0 V and 3.6 V, respectively, for VCCIO only applies to the PCI and PCI-X I/O standards. See **Table 4.4** for the voltage range of other I/O standard.

Single-Ended I/O Standards

Table4.4 and **Table4.5** provide operating condition information when using single-ended I/O standards with Flexera devices. **Table 4.3** provides descriptions for the voltage and current symbols used in **Table 4.4** and **Table 4.5.**

Table 4.3 Voltage & Current Symbol Definitions	
Symbol	**Definition**
VCC I O	Supply voltage for single-ended inputs and for output drivers
VRE F	Reference voltage for setting the input switching threshold
VIL	Input voltage that indicates a low logic level
VIH	Input voltage that indicates a high logic level
VOL	Output voltage that indicates a low logic level
VOH	Output voltage that indicates a high logic level
IOL	Output current condition under which V_{OL} is tested
IOH	Output current condition under which V_{OH} is tested
VTT	Voltage applied to a resistor termination as specified by HSTL and SSTL standards

Table 4.4 Recommended Operating Conditions for User I/O Pins Using Single-Ended I/O Standards

I/O Standard	V_{CCIO}(V)			V_{REF}(V)			V_{IL} (V)	V_{IH} (V)
	Min	Typ	Max	Min	Typ	Max	Max	Min
3.3-V LVTTL	3.135	3.3	3.465				0.8	1.7
and LVCMOS								
2.5-V LVTTL	2.375	2.5	2.625				0.7	1.7
and LVCMOS								
1.8-V LVTTL and LVCMOS	1.710	1.8	1.890				$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$
1.5-V LVCMOS	1.425	1.5	1.575				$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$
PCI and PCI-X	3.000	3.3	3.600				$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$
SSTL-2 class I	2.375	2.5	2.625	1.19	1.25	1.31	$V_{REF}- 0.18$ (DC) $V_{REF}- 0.35$ (AC)	$V_{REF} + 0.18$ (DC) $V_{REF}+ 0.35$ (AC)
SSTL-2 class II	2.375	2.5	2.625	1.19	1.25	1.31	$V_{REF}- 0.18$ (DC) $V_{REF}- 0.35$ (AC)	$V_{REF} + 0.18$ (DC) $V_{REF}+ 0.35$ (AC)
SSTL-18 class I	1.7	1.8	1.9	0.833	0.9	0.969	$V_{REF}- 0.125$ (DC) $V_{REF}- 0.25$ (AC)	$V_{REF}+ 0.125$ (DC) $V_{REF}+ 0.25$ (AC)
SSTL-18 class II	1.7	1.8	1.9	0.833	0.9	0.969	$V_{REF}- 0.125$ (DC) $V_{REF}- 0.25$ (AC)	$V_{REF}+ 0.125$ (DC) $V_{REF}+ 0.25$ (AC)
1.8-V HSTL class I	1.71	1.8	1.89	0.85	0.9	0.95	$V_{REF}- 0.1$ (DC) $V_{REF}- 0.2$ (AC)	$V_{REF}+ 0.1$ (DC) $V_{REF}+ 0.2$ (AC)
1.8-V HSTL class II	1.71	1.8	1.89	0.85	0.9	0.95	$V_{REF}- 0.1$ (DC) $V_{REF}- 0.2$ (AC)	$V_{REF}+ 0.1$ (DC) $V_{REF}+ 0.2$ (AC)
1.5-V HSTL class I	1.425	1.5	1.575	0.71	0.75	0.79	$V_{REF}- 0.1$ (DC) $V_{REF}- 0.2$ (AC)	$V_{REF}+ 0.1$ (DC) $V_{REF}+ 0.2$ (AC)
1.5-V HSTL class II	1.425	1.5	1.575	0.71	0.75	0.79	$V_{REF}- 0.1$ (DC) $V_{REF}- 0.2$ (AC)	$V_{REF}+ 0.1$ (DC) $V_{REF}+ 0.2$ (AC)

Note:

(1) Nominal values (Nom) are for TA = 25° C, VCCINT = 1.2 V, and VCCIO = 1.5, 1.8, 2.5, and 3.3 V.

Table 4.5 GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VTT	Termination voltage		1.35	1.5	1.65	V
VREF	Reference voltage		0.88	1.0	1.12	V
VIH	High-level input voltage		$V_{REF}+ 0.1$			V
VIL	Low-level input voltage				$V_{REF}- 0.1$	V
VOL	Low-level output voltage	$I_{OL}= 36$ mA *(2)*			0.65	V

Table 4.6 DC Characteristics of User I/O Pins Using Single-Ended Standards

I/O Standard	Test Conditions		Voltage Thresholds	
	I_{OL}(mA)	I_{OH}(mA)	Maximum V_{OL}(V)	Minimum V_{OH}(V)
3.3-V LVTTL	4	−4	0.45	2.4
3.3-V LVCMOS	0.1	−0.1	0.2	V_{CCIO}− 0.2
2.4-V LVTTL and LVCMOS	1	−1	0.4	2.0
1.8-V LVTTL and LVCMOS	2	−2	0.45	V_{CCIO}− 0.45
1.4-V LVTTL and LVCMOS	2	−2	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$
PCI and PCI-X	1.5	−0.5	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$
SSTL-2 class I	8.1	−8.1	V_{TT}− 0.57	V_{TT}+ 0.57
SSTL-2 class II	16.4	−16.4	V_{TT}− 0.76	V_{TT}+ 0.76
SSTL-18 class I	6.7	−6.7	V_{TT}− 0.475	V_{TT}+ 0.475
SSTL-18 class II	13.4	−13.4	0.28	V_{CCIO}− 0.28
1.8-V HSTL class I	8	−8	0.4	V_{CCIO}− 0.4
1.8-V HSTL class II	16	−16	0.4	V_{CCIO}− 0.4
1.4-V HSTL class I	8	−8	0.4	V_{CCIO}− 0.4
1.5V HSTL class II	16	−16	0.4	V_{CCIO}− 0.4

Note:

(1) The values in this table are based on the conditions listed in **Table 4.2** and **Table 4.4**.
(2) This specification is supported across all the programmable drive settings available as shown in the Flexera Architecture chapter of the Flexera Device Handbook.

Differential I/O Standards

The RSDS and mini-LVDS I/O standards are only supported on output pins. The LVDS I/O standard is supported on both receiver input pins and transmitter output pins.

Figure 4.1 shows the receiver input wave forms for all differential I/O standards (LVDS, LVPECL, differential 1.4-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Single - ended waveform

Differential Waveform (Mathematical Function of Positive & Negative Channel)
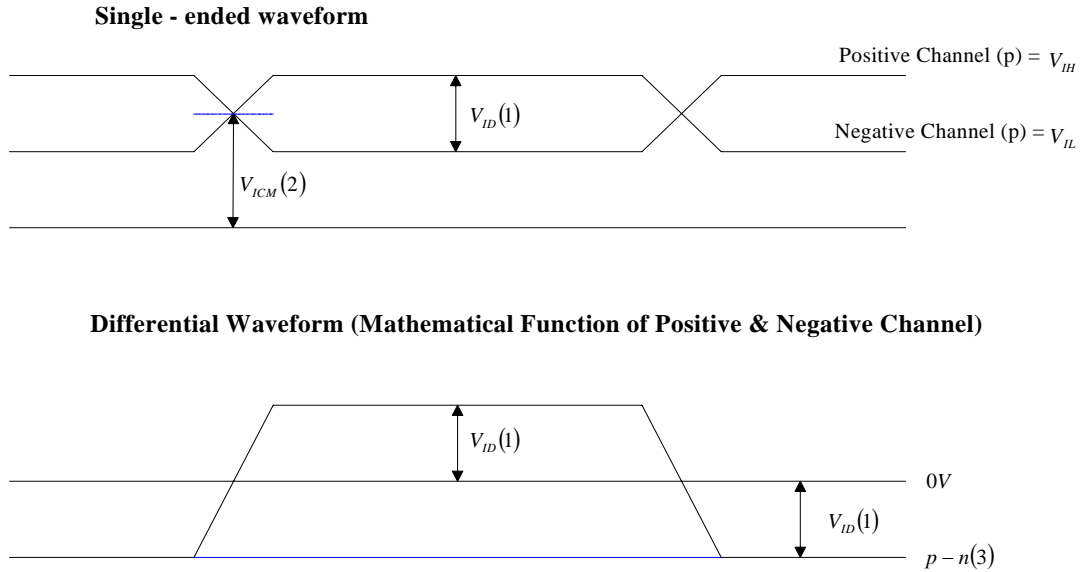
Figure 4.1Receiver Input Waveforms for Differential I/O Standards

Notes:

(1) V_{ID} is the differential input voltage. $V_{ID} = |p - n|$

(2) V_{ICM} is the input common mode voltage. $V_{ICM} = (p + n)/2$

(3) The $p - n$ waveform is a function of the positive channel (p) and the negative channel (n).

Table4.7shows the recommended operating conditions for user I/O pins with differential I/O standards.

Table 4.7 Recommended Operating Conditions for User I/O Pins Using Differential Signal I/O Standards												
I/O Standard	**Vccio(V)**			**VID(V)**			**VICM(V)**			**VIL(V)**		**VIH(V)**	
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Min**	**Max**
LVDS	2.375	2.5	2.625	0.1		0.65	0.1		2.0				
Mini-LVDS *(1)*	2.375	2.5	2.625										
RSDS *(1)*	2.375	2.5	2.625										
LVPECL *(2)*	3.135	3.3	3.465	0.1	0.6	0.95				0	2.2	2.1	2.88
Differential 1.5-V HSTL class I and II *(3)*	1.425	1.5	1.575	0.2		Vccio + 0.6	0.68		0.9		Vref − 0.1	Vref + 0.1	
Differential 1.8-V HST class I and II *(3)*	1.71	1.8	1.89								Vref − 0.1	Vref +0.1	
Differential SSTL-2 class I and II *(4)*	2.375	2.5	2.625	0.36		Vccio + 0.6	0.5 × Vccio − 0.2	0.5 × Vccio	0.5 × Vccio + 0.2		Vref − 0.1	Vref + 0.1	
Differential SSTL-18 class I and II *(4)*	1.7	1.8	1.9	0.25		Vccio + 0.6	0.5 × Vccio − 0.2	0.5 × Vccio	0.5 × Vccio + 0.2		Vref − 0.1	Vref + 0.1	

Notes:
(1) The RSDS and mini-LVDS I/O standards are only supported on output pins.
(2) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
(3) The differential 1.8-V and 1.4-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.
(4) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

Figure 4.2 shows the transmitter output waveforms for all supported differential output standards (LVDS, mini-LVDS, RSDS, differential 1.4-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Single - ended waveform

$V_{OD}(1)$

Positive Channel (p) = V_{OH}

Negative Channel (p) = V_{OL}

$V_{OCM}(2)$

Differential Waveform (Mathematical Function of Positive & Negative Channel)

$V_{OD}(1)$

$0V$

$V_{OD}(1)$

$p - n(3)$
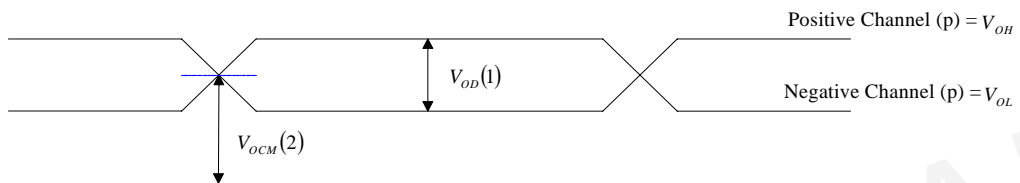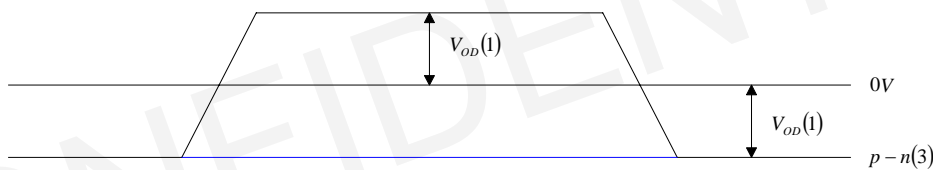
Figure 4.2 Transmitter Output Waveforms for Differential I/O Standards

Notes:
(1) V_{OD} is the differential input voltage. $V_{OD} = |p - n|$
(2) V_{OCM} is the input common mode voltage. $V_{OCM} = (p + n)/2$
(3) The $p - n$ waveform is a function of the positive channel (p) and the negative channel (n).

Table 4.8 shows the DC characteristics for user I/O pins with differential I/O standards.

Table 4.8 DC Characteristics for User I/O Pins Using Differential I/O Standards *Note (1)*											
I/O Standard	**V$_{OD}$(mV)**			**$\triangle$ V$_{OD}$(mV)**		**V$_{OCM}$(V)**			**V$_{OH}$(V)**		**VOL(V)**	
	Min	**Typ**	**Max**	**Min**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Min**	**Max**
LVDS	250		600		50	1.125	1.25	1.375				
mini-LVDS *(2)*	300		600		50	1.125	1.25	1.375				
RSDS *(2)*	100		600			1.125	1.25	1.375				
Differential 1.5-V HSTL class I and II *(3)*									V$_{CCIO}$ − 0.4			0.4
Differential 1.8-V HSTL class I and II *(3)*									V$_{CCIO}$ − 0.4			0.4
Differential SSTL-2 class I *(4)*									V$_{TT}$ + 0.57			V$_{TT}$ −0.57
Differential SSTL-2 class II *(4)*									V$_{TT}$ + 0.76			V$_{TT}$ −0.76
Differential SSTL-18 class I *(4)*						0.5 × V$_{CCIO}$ − 0.125	0.5 × V$_{CCIO}$	0.5 × V$_{CCIO}$ + 0.125	V$_{TT}$ + 0.475			V$_{TT}$ −0.475
Differential SSTL-18 class II *(4)*						0.5 × V$_{CCIO}$ − 0.125	0.5 × V$_{CC\,IO}$	0.5 × V$_{CCIO}$ + 0.125	V$_{CCIO}$ − 0.28			0.28

Notes:
(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
(2) The RSDS and mini-LVDS I/O standards are only supported on output pins.
(3) The differential 1.8-V HSTL and differential 1.4-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.
(4) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

DC Characteristics for Different Pin Types

Table 4.9 shows which types of pins that support bus hold circuitry.

Table 4.9 Bus Hold Support	
Pin Type	**Bus Hold**
I/O pins using single-ended I/O standards	Yes
I/O pins using differential I/O standards	No
Dedicated clock pins	No
JTAG	No
Configuration pins	No

Table 4.10 specifies the bus hold parameters for general I/O pins.

Table 4.10 Bus Hold Parameters		Note (1)					
Parameter	Conditions	VccioLevel					Unit
		1.8 V		2.5 V		3.3 V	
		Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN}> V_{IL}$ (maximum)	30		50		70		μ A
Bus-hold high, sustaining current	$V_{IN}< V_{IL}$ (minimum)	–30		–50		–70		μ A
Bus-hold low, overdrive current	$0\ V < V_{IN}< V_{CCIO}$		200		300		500	μ A
Bus-hold high, overdrive current	$0\ V < V_{IN}< V_{CCIO}$		–200		–300		–500	μ A
Bus-hold trip point (2)		0.68	1.07	0.7	1.7	0.8	2.0	V

Notes:

(1)   There is no specification for bus-hold at VCCIO = 1.5 V for the HSTL I/O standard.

(2)   The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

On-Chip Termination Specifications

Table 4.11 defines the specifications for internal termination resistance tolerance when using series or differential on-chip termination.

Table 4.11 Series On-Chip Termination Specifications					
Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
24-ΩRs	Internal series termination without calibration (24-Ωsetting)	VCC IO= 3.3V	±30	(2)	%
50-ΩRs	Internal series termination without calibration (50-Ωsetting)	VCC IO= 2.5V	±30	(2)	%
50-ΩRs	Internal series termination without calibration (50-Ωsetting)	VCC IO= 1.8V	±30 (1)	(2)	%

Notes:

(3)   For –8 devices, the tolerance is ±40%.

(4)   Pending characterization.

Table 4.12 shows the Flexera device pin capacitance for different I/O pin types.

Table 4.12	Device Capacitance	Note (1)		
Symbol	**Parameter**	**Typical**	**Unit**
CIO	Input capacitance for user I/O pin	6	pF
CLV D S	Input capacitance for dual-purpose LVDS/user I/O pin	6	pF
CVR EF	Input capacitance for dual-purpose VREF and user I/O pin.	21	pF
CDP CL K	Input capacitance for dual-purpose DPCLK and user I/O pin.		pF
CCL K	Input capacitance for clock pin.	5	pF

Notes:

(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflectometry (TDR). Measurement accuracy is within ±0.5 pF.

Pinout Information

Chapter 5   **Complete Datasheet**

AG1F8 is available in two package styles: TQFP144 and PQFP240. This section mainly describes the various pins on Flexera and how they connect within the supported component packages.

Pin Types

Most pins on Flexera are general-purpose, user-defined I/O pins. There are, however, up to 3 different functional types of pins on Flexera packages, as outlined in **Table 5.1**. In the package footprint drawings that follow, the individual pins are sorted according to pin type as in the table.

Table5.1 Types of Pins on Flexera (part *i* **)**			
Type	**Pin Name**	**Pin Type**	**Pin Description**
Power Supply and Voltage Reference Pins	VCCIO[1..4]	Power	I/O supply voltage pins for bank1 through bank 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O. VCCIO also supply voltage to the input buffers used for LVTTL,LVCMOS, 1.5V, 1.8V, 2.5 V and 3.3V
	VCCINT	Power	Internal voltage supply pins. It should be 1.2V
	GND	Ground	Digital Ground
	VREF[0..2]B[1..4]	I/O , Input	Input reference voltage for bank 1-4. It also can be used as I/O.
	VCCA_PLL1/2	Power	Analog power for PLLs. It should connect to 1.2V even if PLL is not used
	GNDA_PLL1/2	Ground	Analog ground for PLLs. It can connect to Ground plan on the board
	GNDG_PLL1/2	Ground	Guard ring ground for PLLs. It can connect to Ground plan on the board
Configuration and JTAG Pins	CFGDONE	Bidirectional	This is a dedicated configuration status pin , not user I/O
	CFGSTATUSn	Bidirectional	This is a dedicated configuration status pin , not user I/O
	CFGn	input (Global Reset)	Dedicated configuration control pin. A low transition resets the target device; a low-to-high transition begins configuration. ALL I/O pins tri-state when CFGn is driven low.

Table5.1 Types of Pins on Flexera (part *ii*)			
Type	Pin Name	Pin Type	Pin Description
Configuration and JTAG Pins	SCLK	input(PS mode) , output (AS mode)	In passive serial configuration mode, SCLK is a clock input used to clock configuration data from external device source into Flexera device. In active serial configuration mode, SCLK is a clock output from Flexera device. (The Flexera is a master in this mode). This is a dedicated pin used for configuration.
	SDIN	input	Dedicated configuration data input pin.
	CEn	input	Active low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When CEn is low, the device is enable and high when it is disabling.
	CEOn	output	Output that drive low when device configuration is completed. During multi device configuration, this pin feeds a subsequence device's CEn pin.
	SDO	I/O, Output	Active serial data output from the Flexera device. In passive serial configuration, this pin becomes user I/O pin.
	CSOn	I/O, Output	Chip select output to enable/disable a serial configuration device. This output is using during active serial configuration mode. In passive serial configuration mode this pin become user I/O.
	INTDONE	I/O, Output	When enable, this pin indicates the device enter the user mode. This pin can be used as a user I/O pin after configuration.
	USERCLK	I/O, input	Optional user supplied Clock input. This pin can be used as user I/O pine after configuration.
	CLD_CLRn	I/O, input	When this pin is low all registers are cleared. When it is high all registers behave as define in the design. This pin can be used as Device Reset (Active Low)
	CLD_OE	I/O, Input	When this pin is low all I/O are tri stated, when it is high all I/O pins behave as define in the design.
	MODE1/MODE0	Input	Dedicated mode select control pins for the configuration mode for the device: 00: Active Serial (Auto Configuration), 01 Passive Serial, 0X JTAG, if JTAG is selected then bits is ignored.
	TMS	Input	JTAG input pin.
	TDI	Input	JTAG input pin.
	TCK	Input	JTAG input pin.
	TDO	Output	JTAG output pin.

Table5.1 Types of Pins on Flexera (part ⅲ)			
Type	Pin Name	Pin Type	Pin Description
Clock and PLL Pins	CLOCK0	Input	Dedicated global clock input. It is also the system clk.
	CLOCK1	Input	Dedicated global clock input.
	CLOCK2	Input	Dedicated global clock input.
	CLOCK3	Input	Dedicated global clock input.
	PLL1_CLKO	I/O, Input	External clock output from PLL1.If clock output from PLL1 is not used , this pin can be user I/O.
	PLL2_CLKO	I/O,Input	External clock output from PLL2.If clock output from PLL2 is not used, this pin can be user I/O.

Package Overview

Flexera devices are available in both quad-flat pack (QFP) and ball grid array (BGA) packaging options. **Table 5.2** shows the package styles and mechanical dimensions for the Flexera family.

Table 5.2 Flexera QFP & FineLine BGA Package Sizes					
Dimension	144-Pin TQFP	240-Pin PQFP	256-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA
Pitch (mm)	0. 5	0.5	1.0	1.0	1.0
Area (mm²)	484	1,024	289	361	441
Length × width (mm × mm)	22 × 22	34.6 × 34.6	17 × 17	19 × 19	21 × 21

TQFP144:144-lead Thin Quad Flat Package

Flexera is available in the 144-lead thin quad flat package, TQFP144. **Table5.3** lists all the package pins. They are arranged in pin number and sorted by bank number. The table also shows Optional Function、Configuration Function and VREF Bank for each pin.

Table5.3 PQFP144 Package Pinout (part _i_)

Pin Number	Pin Name/ Function	Optional Function	Configuration Function	Bank Number	VREF Bank
1	INTDONE		INIT_DONE	B1	VREF0B1
2	IO2			B1	VREF0B1
3	USERCLK	IO3	USERCLK	B1	VREF0B1
4	IO4			B1	VREF0B1
5	VREF0B1	IO5		B1	VREF0B1
6	IO6			B1	VREF0B1
7	IO7			B1	VREF0B1
8	VCCIO1			B1	VREF0B1
9	GND			B1	VREF0B1
10	IO10			B1	VREF0B1
11	VREF1B1	IO11		B1	VREF1B1
12	CSOn	IO12	CSOn	B1	VREF1B1
13	SDIN		SDIN	B1	VREF1B1
14	CFGn		CFGn	B1	VREF1B1
15	VCCA_PLL1			B1	VREF1B1
16	CLOCK0			B1	VREF1B1
17	CLOCK1			B1	VREF1B1
18	GNDA_PLL1			B1	VREF1B1
19	GNDG_PLL1			B1	VREF1B1
20	CEOn		CEOn	B1	VREF1B1
21	CEn		Cen	B1	VREF1B1
22	MODE0		MODE0	B1	VREF1B1
23	MODE1		MODE1	B1	VREF1B1
24	SCLK		SCLK	B1	VREF1B1
25	SDO	IO25	SDO	B1	VREF1B1
26	PLL1CLKo	IO26		B1	VREF1B1
27	IO27			B1	VREF1B1
28	IO28			B1	VREF2B1
29	VCCIO1			B1	VREF2B1
30	GND			B1	VREF2B1
31	VREF2B1	IO31		B1	VREF2B1
32	IO32			B1	VREF2B1
33	IO33			B1	VREF2B1
34	IO34			B1	VREF2B1
35	IO35			B1	VREF2B1
36	IO36			B1	VREF2B1
37	IO37			B2	VREF0B2
38	IO38			B2	VREF0B2

Pin Number	Pin Name/ Function	Optional Function	Configuration Function	Bank Number	VREF Bank
39	IO39			B2	VREF0B2
40	IO40			B2	VREF0B2
41	IO41			B2	VREF2B
42	IO42			B2	VREF0B2
43	GND			B2	VREF0B2
44	VCCIO4			B2	VREF0B2
45	GND			B2	VREF0B2
46	VCCINT			B2	VREF0B2
47	IO47			B2	VREF0B2
48	VREF2B4	IO48		B2	VREF0B2
49	IO49			B2	VREF0B2
50	IO50			B2	VREF0B2
51	IO51			B2	VREF0B2
52	IO52			B2	VREF1B2
53	IO53			B2	VREF1B2
54	GND			B2	VREF1B2
55	VCCINT			B2	VREF1B2
56	VREF1B4	IO56		B2	VREF1B2
57	IO57			B2	VREF1B2
58	IO58			B2	VREF1B2
59	IO59			B2	VREF1B2
60	IO60			B2	VREF2B2
61	VREF0B4	IO61		B2	VREF2B2
62	IO62			B2	VREF2B2
63	GND			B2	VREF2B2
64	VCCINT			B2	VREF2B2
65	GND			B2	VREF2B2
66	VCCIO4			B2	VREF2B2
67	IO67			B2	VREF2B2
68	IO68			B2	VREF2B2
69	IO69			B2	VREF2B2
70	IO70			B2	VREF2B2
71	IO71			B2	VREF2B2
72	IO72			B2	VREF2B2
73	IO73			B3	VREF0B3
74	IO74			B3	VREF0B3
75	IO75			B3	VREF0B3
76	IO76			B3	VREF0B3
77	IO77			B3	VREF0B3

Table5.3 PQFP144 Package Pinout (part ⅱ)

Pin Number	Pin Name/ Function	Optional Function	Configuration Function	Bank Number	VREF Bank
Table5.3 PQFP144 Package Pinout (part iii)						
78	IO78			B3	VREF0B3
79	VREF2B3	IO79		B3	VREF0B3
80	GND			B3	VREF0B3
81	VCCIO3			B3	VREF0B3
82	IO82			B3	VREF0B3
83	IO83			B3	VREF0B3
84	IO84			B3	VREF0B3
85	IO85			B3	VREF0B3
86	CFGDONE		CFGDONE	B3	VREF1B3
87	CFGSTATUSn		CFGSTATUSn	B3	VREF1B3
88	TCK		TCK	B3	VREF1B3
89	TMS		TMS	B3	VREF1B3
90	TDO		TDO	B3	VREF1B3
91	GNDA_PLL2			B3	VREF1B3
92	CLOCK3			B3	VREF1B3
93	CLOCK2			B3	VREF1B3
94	VCCA_PLL2			B3	VREF1B3
95	TDI		TDI	B3	VREF1B3
96	VREF1B3	IO96		B3	VREF1B3
97	IO97			B3	VREF2B3
98	IO98			B3	VREF2B3
99	IO99			B3	VREF2B3
100	IO100			B3	VREF2B3
101	GND11			B3	VREF2B3
102	VCCIO3			B3	VREF2B3
103	IO103			B3	VREF2B3
104	VREF0B3	IO104		B3	VREF2B3
105	IO105			B3	VREF2B3
106	IO106			B3	VREF2B3
107	IO107			B3	VREF2B3
108	IO108			B3	VREF2B3
109	IO109			B4	VREF0B4
110	IO110			B4	VREF0B4
111	IO111			B4	VREF0B4
112	IO112			B4	VREF0B4
113	IO113			B4	VREF0B4
114	IO114			B4	VREF0B4
115	VCCIO2			B4	VREF0B4
116	GND12			B4	VREF0B4

Table5.3 PQFP144 Package Pinout (part ⅳ)					
Pin Number	Pin Name/ Function	Optional Function	Configuration Function	Bank Number	VREF Bank
117	VCCINT			B4	VREF0B4
118	GND13			B4	VREF0B4
119	IO119			B4	VREF0B4
120	VREF0B2	IO120		B4	VREF0B4
121	IO121			B4	VREF0B4
122	IO122			B4	VREF1B4
123	IO123			B4	VREF1B4
124	IO124			B4	VREF1B4
125	VREF1B2	IO125		B4	VREF1B4
126	VCCINT			B4	VREF1B4
127	GND15			B4	VREF1B4
128	IO128			B4	VREF1B4
129	IO129			B4	VREF1B4
130	IO130			B4	VREF2B4
131	IO131			B4	VREF2B4
132	IO132			B4	VREF2B4
133	VREF2B2	IO133		B4	VREF2B4
134	IO134			B4	VREF2B4
135	VCCINT			B4	VREF2B4
136	GND16			B4	VREF2B4
137	VCCIO2			B4	VREF2B4
138	GND17			B4	VREF2B4
139	IO139			B4	VREF2B4
140	IO140			B4	VREF2B4
141	IO141			B4	VREF2B4
142	IO142			B4	VREF2B4
143	CLD_OE	IO143	CLD_OE	B4	VREF2B4
144	CLD_CLRn	IO144	CLD_CLRn	B4	VREF2B4

PQFP240:240-lead Plastic Quad Flat Package

Flexera is available in the 240-lead plastic quad flat package, PQFP240. **Table5.4** lists all the package pins. They are arranged in pin number and sorted by bank number. The table also shows Optional Function、Configuration Function and VREF Bank for each pin.

Table5.4 PQFP240 Package Pinout (part *i*)					
Pin Number	**Pin Name/ Function**	**Optional Function**	**Configuration Function**	**Bank Number**	**VREF Bank**
1	INTDONE		INIT_DONE	B1	VREF0B1
2	IO2			B1	VREF0B1
3	USERCLK		USERCLK	B1	VREF0B1
4	IO4			B1	VREF0B1
5	VREF0B1	IO5		B1	VREF0B1
6	IO6			B1	VREF0B1
7	IO7			B1	VREF0B1
8	IO8			B1	VREFB1
9	VCCIO1			B1	VREF0B1
10	GND			B1	VREF0B1
11	IO11			B1	VREF0B1
12	IO12			B1	VREF0B1
13	IO13			B1	VREF0B1
14	IO14			B1	VREF0B1
15	IO15			B1	VREF0B1
16	IO16			B1	VREF0B1
17	IO17			B1	VREF0B1
18	IO18			B1	VREF0B1
19	IO19			B1	VREFB1
20	IO20			B1	VREF0B1
21	IO21			B1	VREF0B1
22	VCCIO1			B1	VREFB1
23	VREF1B1	IO23		B1	VREF1B1
24	CSOn	IO24	CSOn	B1	VREF1B1
25	SDIN		SDIN	B1	VREF1B1
26	CFGn		CFGn	B1	VREF1B1
27	VCCA_PLL1			B1	VREF1B1
28	CLOCK0			B1	VREF1B1
29	CLOCK1			B1	VREF1B1
30	GNDA_PLL1			B1	VREF1B1
31	GNDG_PLL1			B1	VREF1B1
32	CEOn		CEOn	B1	VREF1B1
33	CEn		Cen	B1	VREF1B1
34	MODE0		MODE0	B1	VREF1B1
35	MODE1		MODE1	B1	VREF1B1
36	SCLK		SCLK	B1	VREF1B1
37	SDO		SDO	B1	VREF1B1
38	PLL1CLKo	IO38		B1	VREF1B1

Pin Number	Pin Name/ Function	Optional Function	Configuration Function	Bank Number	VREF Bank
	Table5.4 PQFP240 Package Pinout (part ⅱ)				
39	IO39			B1	VREF1B1
40	GND			B1	VREF2B1
41	IO41			B1	VREF2B1
42	IO42			B1	VREF2B1
43	IO43			B1	VREF2B1
44	IO44			B1	VREF2B1
45	IO45			B1	VREF2B1
46	IO46			B1	VREF2B1
47	IO47			B1	VREF2B1
48	IO48			B1	VREF2B1
49	IO49			B1	VREF2B1
50	IO50			B1	VREF2B1
51	VCCIO1			B1	VREF2B1
52	GND			B1	VREF2B1
53	IO53			B1	VREF2B1
54	IO54			B1	VREF2B1
55	VREF2B1	IO55		B1	VREF2B1
56	IO56			B1	VREF2B1
57	IO57			B1	VREF2B1
58	IO58			B1	VREF2B1
59	IO59			B1	VREF2B1
60	IO60			B1	VREF2B1
61	IO61			B2	VREF0B2
62	IO62			B2	VREF0B2
63	IO63			B2	VREF0B2
64	IO64			B2	VREF0B2
65	IO65			B2	VREF0B2
66	IO66			B2	VREF0B2
67	IO67			B2	VREF2B
68	IO68			B2	VREF0B2
69	GND			B2	VREF0B2
70	VCCIO4			B2	VREF0B2
71	GND			B2	VREF0B2
72	VCCINT			B2	VREF0B2
73	IO73			B2	VREF0B2
74	VREF2B4	IO74		B2	VREF0B2
75	IO75			B2	VREF0B2
76	IO76			B2	VREF0B2
77	IO77			B2	VREF0B2

Table5.4 PQFP240 Package Pinout (part ⅱ)

Table5.4 PQFP240 Package Pinout (part ⅲ)					
Pin Number	Pin Name/ Function	Optional Function	Configuration Function	Bank Number	VREF Bank
78	IO78			B2	VREF0B2
79	IO79			B2	VREF0B2
80	IO80			B2	VREF0B2
81	IO81			B2	VREF0B2
82	IO82			B2	VREF0B2
83	IO83			B2	VREF0B2
84	IO84			B2	VREF0B2
85	IO85			B2	VREF0B2
86	IO86			B2	VREF1B2
87	IO87			B2	VREF1B2
88	IO88			B2	VREF1B2
89	GND			B2	VREF1B2
90	VCCINT			B2	VREF1B2
91	GND			B2	VREF1B2
92	VCCIO4			B2	VREF1B2
93	VREF1B4	IO93		B2	VREF1B2
94	IO94			B2	VREF1B2
95	IO95			B2	VREF1B2
96	IO96			B2	VREF1B2
97	IO97			B2	VREF1B2
98	IO98			B2	VREF1B2
99	IO99			B2	VREF1B2
100	IO100			B2	VREF1B2
101	IO101			B2	VREF1B2
102	IO102			B2	VREF2B2
103	IO103			B2	VREF2B2
104	IO104			B2	VREF2B2
105	IO105			B2	VREF2B2
106	IO106			B2	VREF2B2
107	VREF0B4	IO107		B2	VREF2B2
108	IO108			B2	VREF2B2
109	GND			B2	VREF2B2
110	VCCINT			B2	VREF2B2
111	GND			B2	VREF2B2
112	VCCIO4			B2	VREF2B2
113	IO113			B2	VREF2B2
114	IO114			B2	VREF2B2
115	IO115			B2	VREF2B2
116	IO116			B2	VREF2B2

Table5.4 PQFP240 Package Pinout (part ⅳ)

Pin Number	Pin Name/ Function	Optional Function	Configuration Function	Bank Number	VREF Bank
117	IO117			B2	VREF2B2
118	IO118			B2	VREF2B2
119	IO119			B2	VREF2B2
120	IO120			B2	VREF2B2
121	IO121			B3	VREF0B3
122	IO122			B3	VREF0B3
123	IO123			B3	VREF0B3
124	IO124			B3	VREF0B3
125	IO125			B3	VREF0B3
126	IO126			B3	VREF0B3
127	VREF2B3	IO127		B3	VREF0B3
128	IO128			B3	VREF0B3
129	GND			B3	VREF0B3
130	VCCIO3			B3	VREF0B3
131	IO131			B3	VREF0B3
132	IO132			B3	VREF0B3
133	IO133			B3	VREF0B3
134	IO134			B3	VREF0B3
135	IO135			B3	VREF0B3
136	IO136			B3	VREF0B3
137	IO137			B3	VREF0B3
138	IO138			B3	VREF0B3
139	IO139			B3	VREF0B3
140	IO140			B3	VREF0B3
141	IO141			B3	VREF0B3
142	GND			B3	VREF0B3
143	PLL2CLKo	IO143		B3	VREF0B3
144	IO144			B3	VREF0B3
145	CFGDONE		CFGDONE	B3	VREF1B3
146	CFGSTATUSn		CFGSTATUSn	B3	VREF1B3
147	TCK		TCK	B3	VREF1B3
148	TMS		TMS	B3	VREF1B3
149	TDO		TDO	B3	VREF1B3
150	GNDA_PLL2			B3	VREF1B3
151	GNDA_PLL2			B3	VREF1B3
152	CLOCK3			B3	VREF1B3
153	CLOCK2			B3	VREF1B3
154	VCCA_PLL2			B3	VREF1B3
155	TDI		TDI	B3	VREF1B3

Table5.4 PQFP240 Package Pinout (part ⅴ)

Pin Number	Pin Name/ Function	Optional Function	Configuration Function	Bank Number	VREF Bank
156	VREF1B3	IO156		B3	VREF1B3
157	VCCIO3			B3	VREF2B3
158	IO158			B3	VREF2B3
159	IO159			B3	VREF2B3
160	IO160			B3	VREF2B3
161	IO161			B3	VREF2B3
162	IO162			B3	VREF2B3
163	IO163			B3	VREF2B3
164	IO164			B3	VREF2B3
165	IO165			B3	VREF2B3
166	IO166			B3	VREF2B3
167	IO167			B3	VREF2B3
168	IO168			B3	VREF2B3
169	IO169			B3	VREF2B3
170	IO170			B3	VREF2B3
171	GND11			B3	VREF2B3
172	VCCIO3			B3	VREF2B3
173	IO173			B3	VREF2B3
174	IO174			B3	VREF2B3
175	IO175			B3	VREF2B3
176	VREF0B3	IO176		B3	VREF2B3
177	IO177			B3	VREF2B3
178	IO178			B3	VREF2B3
179	IO179			B3	VREF2B3
180	IO180			B3	VREF2B3
181	IO181			B4	VREF0B4
182	IO182			B4	VREF0B4
183	IO183			B4	VREF0B4
184	IO184			B4	VREF0B4
185	IO185			B4	VREF0B4
186	IO186			B4	VREF0B4
187	IO187			B4	VREF0B4
188	IO188			B4	VREF0B4
189	VCCIO2			B4	VREF0B4
190	GND12			B4	VREF0B4
191	VCCINT			B4	VREF0B4
192	GND13			B4	VREF0B4
193	IO193			B4	VREF0B4
194	VREF0B2	IO194		B4	VREF0B4

Table5.4 PQFP240 Package Pinout (part ⅴ)

Table5.4 PQFP240 Package Pinout (part vi)					
Pin Number	Pin Name/ Function	Optional Function	Configuration Function	Bank Number	VREF Bank
195	IO195			B4	VREF0B4
196	IO196			B4	VREF0B4
197	IO197			B4	VREF0B4
198	IO198			B4	VREF0B4
199	IO199			B4	VREF0B4
200	IO200			B4	VREF1B4
201	IO201			B4	VREF1B4
202	IO202			B4	VREF1B4
203	IO203			B4	VREF1B4
204	IO204			B4	VREF1B4
205	IO205			B4	VREF1B4
206	IO206			B4	VREF1B4
207	IO207			B4	VREF1B4
208	VREF1B2	IO208		B4	VREF1B4
209	VCCIO2			B4	VREF1B4
210	GND14			B4	VREF1B4
211	VCCINT			B4	VREF1B4
212	GND15			B4	VREF1B4
213	IO213			B4	VREF1B4
214	IO214			B4	VREF1B4
215	IO215			B4	VREF1B4
216	IO216			B4	VREF2B4
217	IO217			B4	VREF2B4
218	IO218			B4	VREF2B4
219	IO219			B4	VREF2B4
220	IO220			B4	VREF2B4
221	IO221			B4	VREF2B4
222	IO222			B4	VREF2B4
223	IO223			B4	VREF2B4
224	IO224			B4	VREF2B4
225	IO225			B4	VREF2B4
226	IO226			B4	VREF2B4
227	VREF2B2	IO227		B4	VREF2B4
228	IO228			B4	VREF2B4
229	VCCINT			B4	VREF2B4
230	GND16			B4	VREF2B4
231	VCCIO2			B4	VREF2B4
232	GND17			B4	VREF2B4
233	IO233			B4	VREF2B4

Table5.4 PQFP240 Package Pinout (part ⅶ)

Pin Number	Pin Name/ Function	Optional Function	Configuration Function	Bank Number	VREF Bank
234	IO234			B4	VREF2B4
235	IO235			B4	VREF2B4
236	IO236			B4	VREF2B4
237	IO237			B4	VREF2B4
238	IO238			B4	VREF2B4
239	CLD_OE	IO239	CLD_OE	B4	VREF2B4
240	CLD_CLRn	IO240	CLD_CLRn	B4	VREF2B4