PCI Bus Target Megafunction

Solution Brief 6 **November 1996, ver. 1**

Target Applications:
Communications
Digital Signal Processing

Family: FLEX 8000 and FLEX 10K

Vendor:

Eureka Technology

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Features

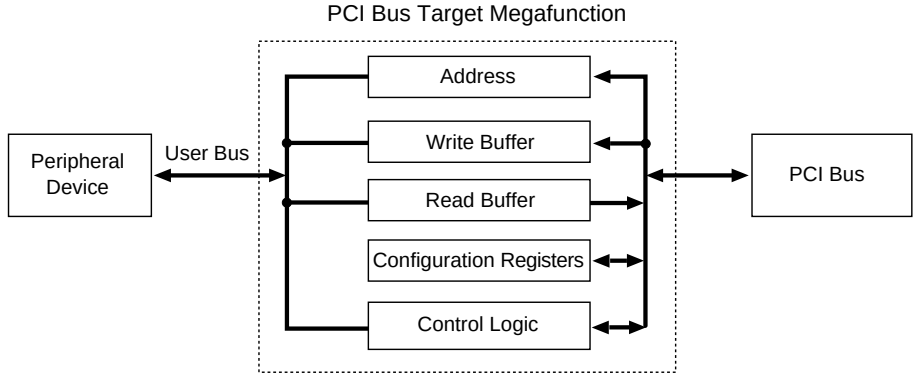
- Fully compliant with peripheral component interconnect Special Interest Group's (PCI-SIG) ***PCI Local Bus Specification***.
- Optimized for the Altera® FLEX® 8000 and FLEX 10K device architectures
- Flexible PCI bus interface to accommodate different types of peripheral devices
- Full-speed burst support (132 Mbytes per second)
- Internal write buffer to accelerate write access

General Description

A PCI bus is a processor-independent, high performance system that supports data transfers up to 132 Mbytes per second. The PCI bus implementation enables the PCI bus to support advanced features such as multiple processor architectures and automatic system configuration. The strict timing of the PCI bus makes it difficult to implement PCI interface functions in programmable logic devices (PLDs).

The PCI bus target megafunction from Eureka Technology bridges the gap between a complex PCI bus system and user peripherals. Because most peripheral devices are designed with a simple read/write bus that supports all data transfers, the megafunction, with its efficient user bus, can connect directly to any of these peripheral devices. In addition, the megafunction automatically generates or receives all PCI bus signals. See Figure 1.

Figure 1. PCI Bus Target Megafunction Connect to Peripheral Device



Functional Description

The PCI bus target megafunction has three user bus options to support peripheral devices with different data transfer characteristics. For each user bus option, the megafunction provides the byte assemble and disassemble functions to match the peripheral device bus data width with the user-bus data width. The three user bus options are described below.

- Synchronous user bus. This bus is normally used in 486-based PC systems. All transfers are fully synchronized with the system clock, and wait states can be inserted by a peripheral device any time during data transfer.
- User bus that interfaces directly with first-in first-out (FIFO) buffers. Data transfer typically requires zero-wait state transfers, unless a FIFO full or empty signal is detected.

- User bus that is similar to the industry-standard architecture (ISA) bus design. Data transfer is not required to synchronize with the system clock. In this mode, buses narrower than 32 bits are allowed.

The megafunction also includes a 32-bit write buffer that improves the speed of write operations on a user bus. As data is written into the megafunction's write buffer, the data transfer on a bus is completed simultaneously, allowing the bus to perform other write operations. The peripheral device may take as many clock cycles as needed to complete the write operation without affecting the bus performance.

The PCI bus specification requires all target devices to support several configuration registers, which are used by the system software for automatic system configuration. Special configurations, however, are required for the system to access the registers. The megafunction contains all configuration registers, and it automatically handles all configuration cycles without requiring the peripheral device to process them. Table 1 lists the required configuration parameters.

Table 1. Configurable System Parameters

Configuration Parameter	Size	Assigned By
Device ID	16 bits	User
Vendor ID	16 bits	PCI-SIG
Class code	24 bits	User
Revision ID	8 bits	User
Address range	–	User
Subsystem ID	16 bits	User
Subsystem vendor ID	16 bits	PCI-SIG

Performance

The PCI bus allows a high bandwidth data transfer. The megafunction supports burst data transfer up to 132 Mbytes per second. Once initiated, zero-wait state data transfer can be sustained between a peripheral device and a PCI bus. If slower peripheral devices are used, wait states must be inserted to accommodate slower peripheral performance. Table 2 illustrates the device utilization for a typical PCI bus implementation.

Table 2. Typical Device Utilization

Function	User Bus Option	Logic Cells
PCI bus target with burst mode	Synchronous bus	340
PCI bus target without burst mode	Synchronous bus	250

Reference

PCI Local Bus Specification. Rev. 2.1. Portland, Oregon: PCI Special Interest Group, 1995.

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