How to Upgrade an AT91M40400-based System to an AT91M40800-based System

Background

The AT91M40400 and the AT91M40800 are both members of the Atmel AT91 16/32-bit microcontroller family, which is based on the ARM7TDMI™ processor core. Their main differences are that the AT91F40400 has 4K bytes of internal SRAM and the AT91F40800 has 8K bytes of internal SRAM.

The following paragraphs outline the hardware and software operations to perform when a user would like to upgrade an AT91M40400-based system to an AT91M40800-based system.

Hardware Requirements

Microcontroller Replacement

The user must first replace the microcontroller IC. The AT91M40400 and the AT91M40800 are pin-to-pin compatible and both are packaged in 100-lead TQFP package. The user needs to install the AT91M40800 in place of the AT91M40400.

Internal Pull-up

The AT91M40400 has an internal pull-up resistor on the NRST input pin. This internal pull-up is not present in the AT91M40800. The user should verify whether an external pull-up resistor of 100kΩ on the NRST pin needs to be added.

Note Regarding 5V-tolerant I/O Lines

The AT91M40400 (rev. C) and the AT91M40800 have 5V-tolerant I/Os.

Warning Concerning First Access after a Reset

The AT91M40400 performs the first access to the memory bank connected to NCS0 10 clock cycles after the rising edge of the NRST signal. This period has been increased to 80 clock cycles on the AT91M40800 in order to conform to increased reset time requirements for nonvolatile memories containing the boot code.

AT91 ARM® Thumb® Microcontrollers

Application Note

Rev. 1731A–11/00

Software Requirements

As the core, the architecture and the peripherals of both the AT91M40400 and the AT91M40800 are all compatible, any program written for an AT91M40400-based system can run as is on the same system built with an AT91M40800.

Internal Memory Increase

The AT91M40800 internal memory size is greater than the AT91M40400. If a program has stacks allocated in internal memory, the stack start addresses can be increased from 0x1000 to 0x2000.

Power Management and Clock Controller

The AT91M40800 presents an additional power management feature: peripheral clocks can be enabled and disabled individually. This feature optimizes system power consumption depending on the application phase.

Because the AT91M40800 Power Management Controller defaults after reset to the state when all peripheral clocks are enabled, the code written for the AT91M40400 is compatible with the AT91M40800.

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1731A–11/00/0M