How to Upgrade an AT91F40416-based System to an AT91F40816-based System

Background

The AT91F40416 and AT91F40816 are members of the Atmel AT91 16/32-bit microcontroller family which is based on the ARM7TDMI™ processor core. Their main differences are that the AT91F40416 has 4K bytes of internal SRAM and the AT91F40816 has 8K bytes of internal SRAM. The clocks on the peripherals of the AT91F40416 cannot be deactivated, whereas they can be deactivated with the AT91F40816.

The following paragraphs outline the hardware and software operations to perform when a user wants to upgrade an AT91F40416-based system to an AT91F40816-based system.

Hardware Requirements

Microcontroller Replacement

As the AT91F40416 and the AT91F40816 are pin-to-pin compatible and both are packaged in 120-ball BGA, the user simply needs to install the AT91F40816 in the place of the AT91F40416 in the application.

Internal Pull-up

The AT91F40416 has an internal pull-up resistor on the NRST input pin. This internal pull-up is not present in the AT91F40816. The user should verify whether an external pull-up resistor of 100 kΩ on the NRST pin needs to be added.

Note Regarding 5V-tolerant I/O Lines

The I/O pads of the AT91F40416 are not 5V-tolerant; however, the I/O pads of the AT91F40816 are 5V-tolerant, excluding the EBI Data Bus (D0 - D15). This enables the PIO pads to interface with external 5V devices without any additional components.

Warning Concerning First Access after a Reset

The AT91F40416 performs the first access to the memory bank connected to NCS0 10 cycles after the rising edge of the NRST signal. This period has been increased to 80 clock cycles on the AT91F40816.

Software Requirements

As the core, the architecture and the peripherals of both the AT91F40416 and the AT91F40816 are all compatible, any program written for an AT91F40416-based system can run as is on the same system built with an AT91F40816.

Internal Memory Increase

The AT91F40816 internal memory size is greater than the AT91F40416. If a program has stacks allocated in internal memory, the stack start addresses can be increased from 0x1000 to 0x2000.

Power Management and Clock Controller

The AT91F40816 provides an additional power management feature: peripheral clocks can be enabled and disabled individually. This feature allows a system power consumption optimization depending on the application phase.

Because the AT91F40816 Power Management Controller defaults after reset to the state when all peripheral clocks are enabled, the code written for the AT91F40416 is compatible with the AT91F40816.

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