Interfacing a PC Card to an AT91RM9200-DK

AT91 ARM® Thumb® Microcontrollers

Application Note

Introduction

This Application Note describes the implementation of a PCMCIA interface on an AT91RM9200 Development Kit (DK) using the External Bus Interface (EBI). The hardware connections between the PCMCIA interface and the AT91RM9200 microcontroller are described. Programming examples to access a CompactFlash® Memory Card and a Hard Disk Drive are given.

Hardware Interface

This section describes the hardware interface between the PCMCIA Controller and the AT91RM9200-DK.

The PCMCIA interface consists of a daughter board to be connected to an AT91RM9200-DK. It is accessed by the AT91RM9200 microcontroller through a Chip Select of the Static Memory Controller (SMC). The NWAIT feature of the SMC gives PC cards the possibility of using the WAIT# signal to extend normal access timing and to maintain control of the access length.

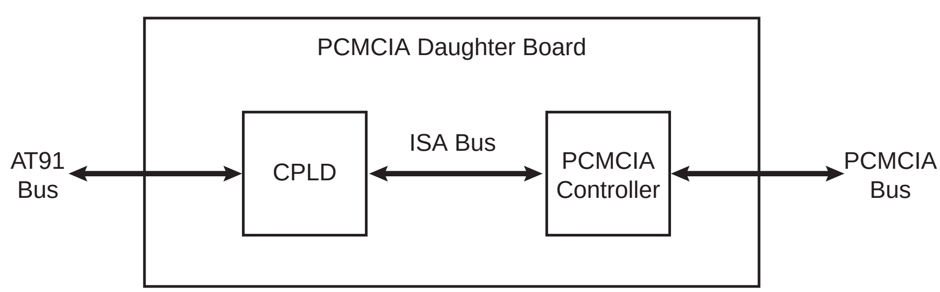
The PCMCIA daughter board is based on an Intel®PD6710 device. This is a PC card socket controller designed to be connected to a PC ISA bus.

The AT91 processor cannot generate all ISA bus access features. For this reason, a CPLD has been inserted between the PD6710 and the AT91RM9200 to convert the SMC access protocol to the ISA bus access protocol.

The AT91RM9200 A24 address bit (programmed as a PIO line) is used to decode the accesses to the two memory spaces defined in the ISA bus standard (Memory and IO).

The PD6710 device embeds buffers on all PCMCIA slot signals. This ensures the PCMCIA device's live insertion facility.

Figure 1. PCMCIA Interface Block Diagram



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EBI<->ISA CPLD AC Characteristics

This section gives information on the timing requirements in order to access the PCM CIA daughter board.

In the following table, t_{MCK} is the AT91RM9200 Master Clock period and t_{CLOCK} is the period of the clock provided by the AT91RM9200 PCK0 output or by the crystal oscillator, Y1, fitted on the daughter board.

Clock frequency must be as close as possible to 25 MHz (frequency required by the PD6710 device).

Table 1. EBI<->PCMCIA Signals Relative to MCK and CLOCK

Symbol	Parameter	Min	Max	Units
PCM1	NRST_CMD generated reset pulse width	500		ns
PCM2	Clock active before end of reset(1)	500		ns
PCM3	End of NRST_CMD generated reset to NCS low	500 $-4t_{CLOCK}$		ns/t_{CLOCK}
PCM4	NCS falling to PWAIT active	1	2	t_{CLOCK}
PCM5	PWAIT falling to NWE inactive	4	7	t_{MCK}
PCM6	PWAIT falling to NOE inactive	4.5	7.5	t_{MCK}
PCM7	NOE inactive pulse width	4.5	6.5	t_{MCK}
PCM8	NWE inactive pulse width	5	7	t_{MCK}
PCM9	Data hold after NOE High	0	0.5	t_{CLOCK}
PCM10	PWAIT Minimum Pulse Width when CPLD access is inactive(2) on Memory mode	10		t_{CLOCK}
PCM11	PWAIT Minimum Pulse Width when CPLD access is inactive(2) on IO mode	9		t_{CLOCK}
PCM12	PWAIT Minimum Pulse Width when CPLD access is active(2) on Memory mode	24		t_{CLOCK}
PCM13	PWAIT Minimum Pulse Width when CPLD access is active(2) on IO mode	22		t_{CLOCK}

Notes:
1. Clock input must be active for a minimum of 500 ns before NRST_CMD goes active to allow internal circuitry to be initialized correctly.
2. CPLD access is active when the 16-bit wide AT91 data bus is selected and the card connected to the device supports only 8-bit wide accesses.

Figure 2. Reset Timing

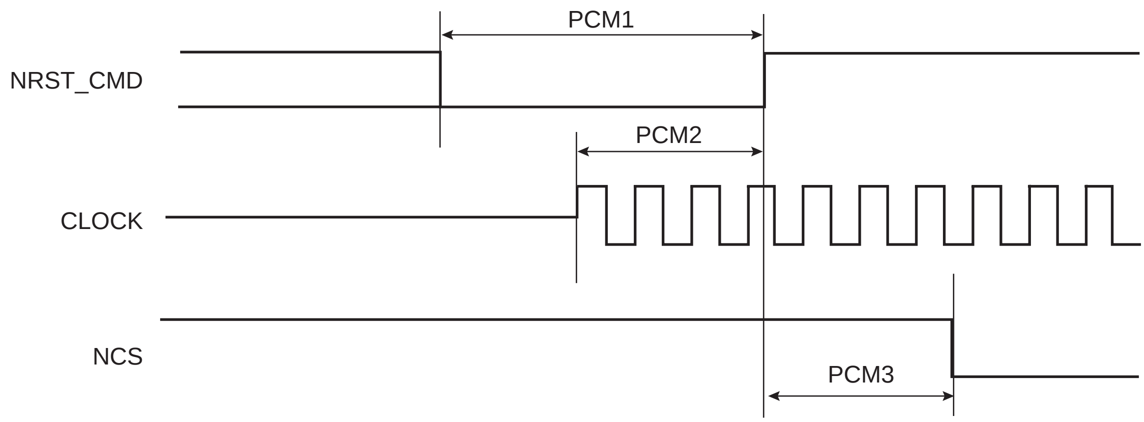
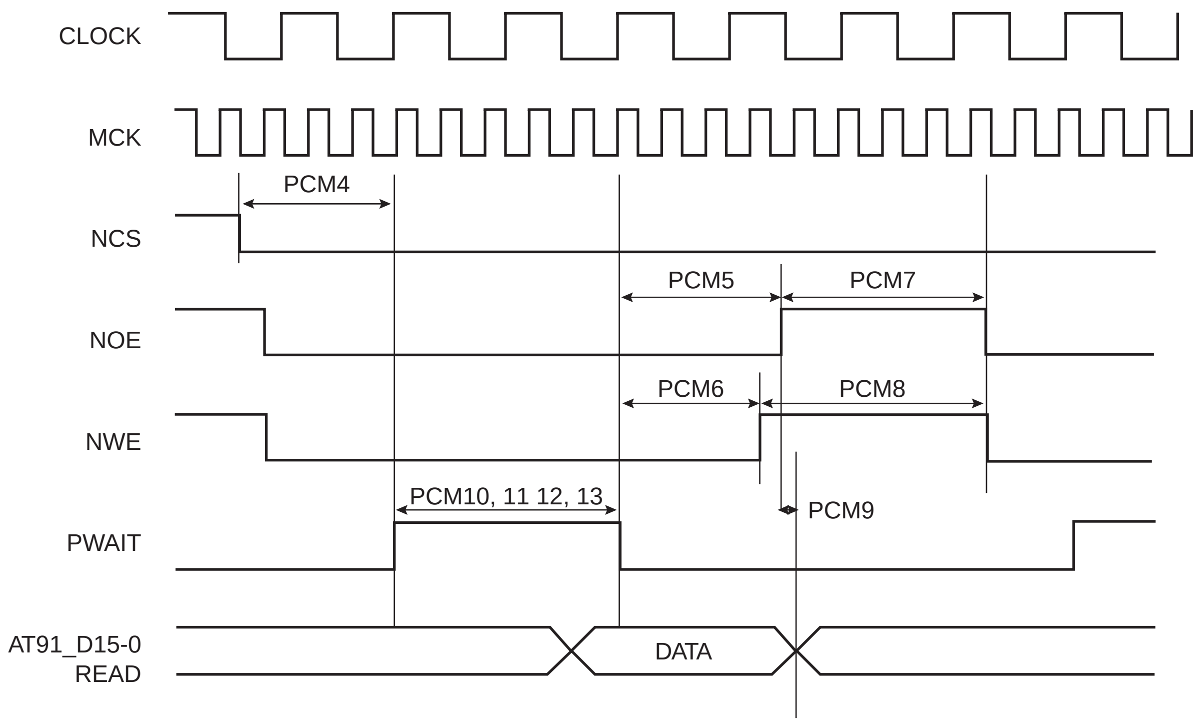


Figure 3. Bus Timing



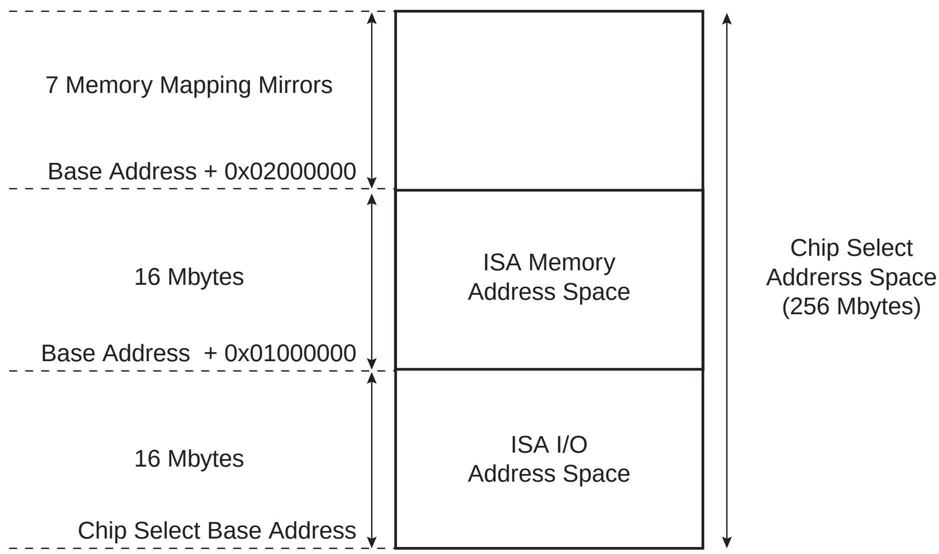
Software Interface

Memory Address Space

The ISA bus standard specifies two access modes (Memory and I/O), each involving a different set of control signals. The A24 EBI address line (programmed as a PIO line) has been used to emulate these access modes by dividing the area defined by the chip select used.

The resulting memory mapping is shown in Figure 4 below.

Figure 4. Memory Mapping



PD6710 Windowing Capabilities

For full compatibility with existing software, and to ensure compatibility with future memory cards and software, the PD6710 provides five programmable memory windows and two programmable I/O windows. The programmable memory windows can only be accessed by the AT91RM9200 through the ISA memory address space, whereas the programmable I/O windows can only be accessed through the ISA I/O address space.

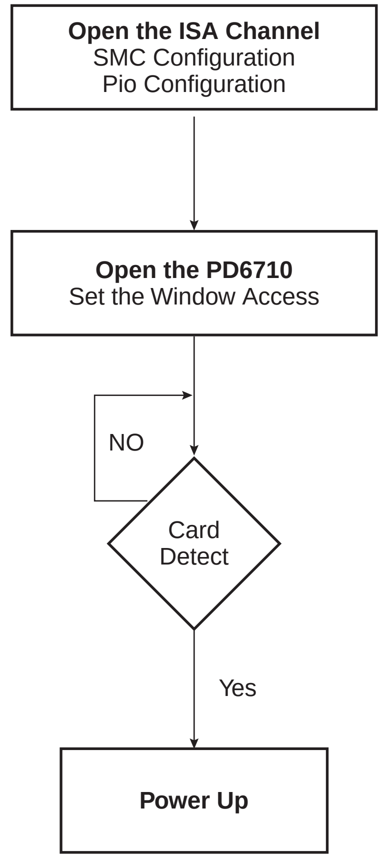
Having five memory windows allows a memory-type card to be accessed through four memory windows programmed for common memory access (allowing PC-type expanded memory-style management), leaving the fifth memory window available to be programmed to access the card's attribute memory without disrupting the common memory in use (refer to the PD6710/'22 ISA-to-PC-Card (PCMCIA) Controllers datasheet).

The source code given as an example with this application note shows how to do the following.

- Initialize the Interface
- Access a CompactFlash
- Access a Hard Disk Drive

Flow Chart

Figure 5. Initialization of the Interface



SMC Configuration

In this example, the EBI Chip Select chosen to access the daughter board is NCS7 and master clock frequency is 60 MHz, clock frequency is 24 MHz, issued from PCK0.

The Chip Select register programming, in compliance with Table 1, "EBI<->PCMCIA Signals Relative to MCK and CLOCK," on page 2, is as follows:

1. Configure NWS with the number of standard wait states to access the PC Card (6 MCK).
2. Set WSEN to enable standard wait states.
3. Configure RWHOLD for read and write signal hold time (4 MCK).
4. Configure RWSETUP for read and write signal setup time (0 MCK).
5. Configure DBW and BAT to set the data bus size as 16-bit or 8-bit.
6. Configure Address to Chip Select Setup in standard mode.

PIO and Peripheral Configuration

1. Set AT91C_PC13_NCS7 as peripheral.
2. Set AT91C_PB27_PCK0 as peripheral.
3. Program PCK0 as PLLB output divided by 4 (24Mhz).
4. Set NWAIT/PC6 as peripheral.
5. Set PC8_A24 as PIO.
6. Reset the PD6710 device by asserting the NRST_CMD signal with timings compliant to PCM1 (see Table 1 on page 2).

Programming Example

CompactFlash Accesses

CompactFlash Memory Mode Accesses

1. Set the card to Memory Mode.
2. Read Card Information Structure.
3. Issue Identify Drive AT command (ECH).

CompactFlash I/O Mode Accesses

1. Set the card to I/O mode.
2. Write to a memory block (30H).
3. Read back from a memory block (20H).
4. Issue Identify Drive AT command (ECH).

The model of CompactFlash memory card used in this example is a SanDisk® 8-MB CompactFlash Memory Card.

HDD ATA Mode Accesses

1. Set the card in I/O mode.
2. Set the PD6710 device in ATA mode.
3. Reset the HDD.
4. HDD Access Test
   – Writing
   – Reading
   – Verifying

The model of HDD storage used in this example is a Toshiba®MK1003GAL 10GO.

All datasheets, schematics, board design description and source codes relevant to this application note can be downloaded from the Atmel web site. http://www.atmel.com/

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