## Interfacing a Hard Disk Drive to an AT91RM9200 Microcontroller

## Scope

This Application Note describes the hardware and software interface for a hard disk drive. The AT91RM9200 embeds a CompactFlash<sup>™</sup> Glue Logic that can be adapted to support such a peripheral.

## **Reference Documents**

The following table gives the references of the documents and their denominations in this Application Note.

### Table 1. Reference Document Table

Owner - Reference	Denomination
Atmel Literature number 6015	AT91RM9200 Errata Sheet
Atmel ABP-MPD-EBI-010	EBI Programmer Datasheet,14-Mar-2003
	AT Attachment Interface Document, American National Standards Institute, X3.221-1994



AT91 ARM<sup>®</sup> Thumb<sup>®</sup> Microcontrollers

## **Application Note**

6023A-ATARM-11-Dec-03





## **Hardware Interface**

# External Bus Interface Signals

The External Bus Interface integrates circuitry to interface with CompactFlash devices using Attribute, Memory and I/O modes. Most of these signals can be used to connect a hard disk drive to the AT91RM9200.

- Note: For a full description of external bus interface signals, refer to the EBI Programmer Datasheet. This document only contains information relevant to accessing a hard disk drive.
- Note: The External Bus Interface does not allow DMA accesses.

EBI Name	HDD Name	Function	Туре	Active Level	
CFIOR	_IOR	HDD I/O Read Signal	Output	Low	
CFIOW	_IOW	HDD I/O Write Signal	Output	Low	
CFRNW		HDD Read Not Write	Output		
CFCS		HDD Chip select	Output	Low	
A0-A2	A0-A2	Address Bus	Output		
D0-D15	D0-D15	Data Bus	Input/Output		
NWAIT	IORDY	HDD Ready Signal	Input	High	

### Table 2. EBI Signals for HDD Support

## Other AT91RM9200 Signals

In addition to the External Bus interface signal, the hard disk drive requires the signals shown in Table 3.

Table 3. Other AT91RM9200 Signals for HDD Support

AT91RM9200 Name	HDD Name	Function	Туре	Active Level
PC11-PC12	_CS0CS1	HDD Chip Select	Output	Low
PC5 <sup>(1)</sup>	_RESET	HDD Reset	Output	Low

Note: 1. Or any free PIO.

Other HDD signals are not handled by the AT91RM9200 microcontroller.

## **HDD Application Example**

## Figure 1. HDD Application Example







## **Software Interface**

External Bus Interface Signal Handling	The EBI CompactFlash Glue Logic integrates a fourth memory space that can be accessed through NCS4 (i.e., between 0x5000 0000 and 0x5FFF FFFF).				
	This memory space, True IDE Mode Space, is intended to access CompactFlash in True IDE Mode (Hard Disk Drive, so). <b>Table 4.</b> Address Map				
			I/O Mode Space		
	Offset 0x0080.0000				
	Offset 0x0040.0000	Common Memory Mode Space			
		Attribute Memory Mode Space			
	Offset 0x0000.0000				
	To use the CompactFlash Glue Logic feature, the following PIOs must be set as peripherals:				
	<ul> <li>PC6 that enables NWAI</li> </ul>	Т			
	<ul> <li>PC7 that enables A23</li> </ul>				
	<ul> <li>PC9 that enables A25_CFRNW</li> </ul>				
	<ul> <li>PC10 that enables NCS</li> </ul>	4_CFCS			
	Moreover, the CompactFlash Glue Logic must be activated via the Chip Select 4 Assignment Field in the EBI User Interface.				
Handling Other AT91RM9200 Signals	In Attribute, Memory and I/O mo CS1 HDD signals are used by th and lower-byte access on the da	odes, PC11 - PC12 signals that are connected to CS0 - le EBI to manage CFCE1 - CFCE2 to enable upper-byte ata bus of the CompactFlash.			
	As this behavior is not compatible with IDE accesses, these signals must be configured				

as PIOs, i.e., PC11 and PC12. PC11 and PC12 levels must be set by software before the access to the HDD.

Data Bus Width must be set depending on the access needed. See Table 5.

 Table 5.
 Signals Depending on Access Type

Access	PC11	PC12	Offset	D[15:8]	D[7:0]	SMC_CSR4 (DBW)
Byte R/W Task File Register Access	0	1	1 - 7h	Don't Care/High Z	Odd/Even Byte	8-bit
Half-word R/W Task File Data Register Access	0	1	0h	Odd Byte	Even Byte	16-bit
Byte W Control Register Byte R Alt Status Register Byte R/W Drive Access Register	1	0	6 - 7h	Don't Care/High Z	Odd/Even Byte	8-bit

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## Timings

The SMC2\_CSR4 Chip Select is to be programmed depending on the HDD timing accesses. Typical values are listed in Table 6.

 Table 6.
 Timing Parameter Values

Parameter	Value
NWS	10
TDF	0
RWS	5
RWH	3

**Software Example** An example HDD driver describing signal management with the AT91 software package can be downloaded from the Atmel web site http://www.atmel.com.

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