AT91M55800A Clock Switching Considerations using Advanced Power Management Controller

AT91 ARM® Thumb® Microcontrollers

Application Note

Introduction

The AT91M55800A is designed for ultra low-power applications and features an Advanced Power Management Controller peripheral (APMC) allowing optimization of power consumption. The APMC allows the Master Clock (MCK) to be selected between the Slow Clock, the output of the Main Oscillator or the output of the PLL. This Application Note describes the clock switching considerations to safely switch the Master Clock frequency MCK to one of the different clock sources of the AT91M55800A. It also provides a software driver for the clock switching according to these considerations.

Associated Software File

The ZIP file “clock_switching_driver.zip” should be downloaded from the Software section of the AT91 pages on Atmel’s web site and unzipped. It gives the software described in this application note.

Warranty

Rev. 1797A–ATARM–08/02

Terminology

This Application Note employs typographic conventions intended to improve its ease of use. Table 1 summarizes this dedicated terminology:

Table 1. Typographic Conventions

Category	Code	Description
Related to Numeric Base	0b	Binary Number
	0x	Hexadecimal Number
Related to AT91M55800A Clock Source	SLCK	Low Frequency Oscillator (32.768 kHz)
	MO	Main Oscillator
	PLL	Internal Phase Locked Loop
Related to AT91M55800A Internal Registers	MOSCEN	APMC_CGMR Field used to enable MO
	MUL	Phase Locked Loop Factor in APMC_CGMR
	CSS	APMC_CGMR Field used to select Clock Source. See Table 2.
	MOSCS	Status Bit in APMC_SR concerning MO
	LOCK	Status Bit in APMC_SR concerning PLL

AT91M55800A Clock Sources

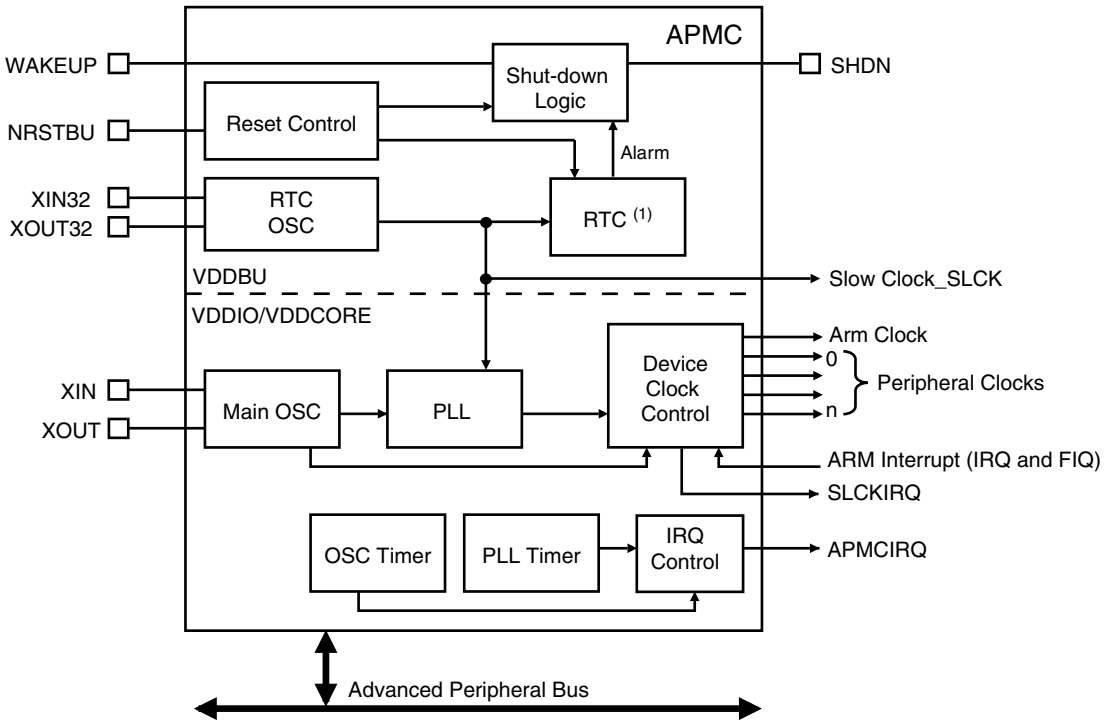
The AT91M55800A has two oscillators:

1. The Slow Clock (SLCK) oscillator is a very low power 32 kHz oscillator powered by the backup battery voltage supplied on the VDDBU pins. The XIN32 and XOUT32 pins must be connected to a 32.768 kHz crystal. The Slow Clock is the only clock considered permanent in an AT91M55800A-based system and is essential in the operations of the APMC.
2. The Main Oscillator (MO) provides a clock that depends on the frequency of the crystal connected between pins XIN and XOUT. The Main Oscillator is designed for a wide frequency range (3 MHz to 20 MHz fundamental crystal). Unlike the Slow Clock, the Main Oscillator may have a transient function, controlled by the bit MOSCEN. By using this field the application programmer is able to manage, under software control, the power supply to the Main Oscillator, for an improved power management in the application. The Main Oscillator frequency drives the Phase Locked Loop (PLL), which multiplies the frequency of its input signal by a number up to 64. This number is programmed in the MUL field of APMC_CGMR and the multiplication ratio is the programmed value plus one (MUL+1). If a null value is programmed into MUL, the PLL is automatically disabled to save power.

AT91M55800A Advanced Power Management Controller

The AT91M55800A features an Advanced Power Management Controller, which optimizes the power consumption of the device and the complete system. The APMC controls the clocking elements such as the oscillators and the PLL, the ARM7TDMI™ core and the peripheral clocks, and has the capability to control the system power supply. See Figure 1. The APMC is a state machine running from the 32.768 kHz clock source, therefore the low frequency oscillator must be running continuously.

Figure 1. APMC module



The APMC can generate interrupt events in two cases:

1. When the oscillator counter reaches 0. OSCOUNT specifies the number of 32.768 kHz divided by 8 clock cycles for the Main Oscillator start-up timer to count before the Main Oscillator is stabilized, after the oscillator has been enabled. The Main Oscillator counter is a down-counter which is pre-loaded with the OSCOUNT value when the MOSCEN bit in the Clock Generator Mode register (CGMR) is set.
2. When the PLL counter reaches 0. PLLCOUNT specifies the number of 32.768 kHz clock cycles for the PLL lock timer to count before the PLL is locked, after the PLL is started. The PLL counter is a down-counter which is preloaded with the PLLCOUNT value when the MUL field in the Clock Generator Mode register (CGMR) is modified.

The APMC also features the Slow Clock interrupt SLCKIRQ, allowing the user to detect when the Master Clock has actually switched to the Slow Clock. Switching from the Slow Clock to a higher frequency is generally performed safely, as the processor is running slower than the target frequency. However, switching from a high frequency to the Slow Clock implies the high frequency to be valid during the switch time. The Slow Clock interrupt permits the user to know exactly when the switch has been achieved, thus, when the Main Oscillator or the PLL can be disabled.

AT91M55800A Master Clock Selection

The MCK (Master Clock) can be selected through the CSS field in APMC_CGMR between the Slow Clock, the output of the Main Oscillator or the output of the PLL as shown in Table 2.

Table 2. Clock source selection

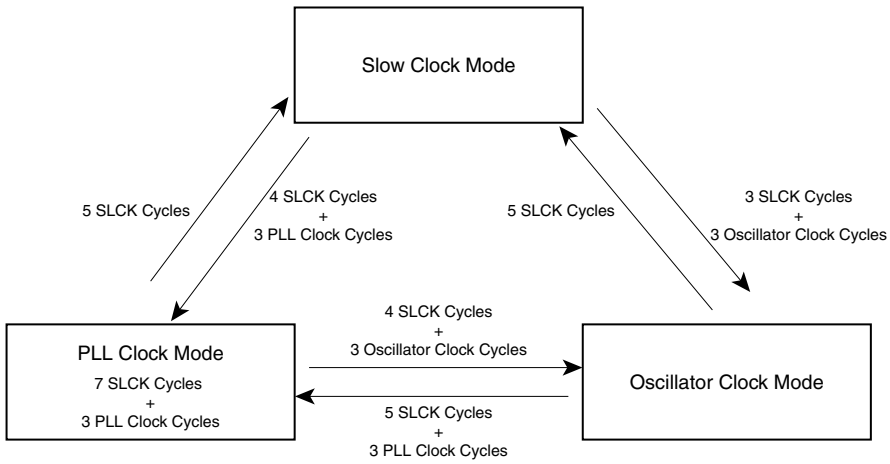
CSS Bit Combination		Clock Source Selection
0	0	Low Frequency Clock (SLCK)
0	1	Main Oscillator (MO)
1	0	Phase Locked Loop Output (PLL)
1	1	Reserved

Writing CSS to the following values, and under the following conditions is forbidden, and the write operation of APMC_CGMR is not taken into account in these cases:

- Deselect the Slow Clock if the Main Oscillator is disabled or its output is not stabilized
- Disable the PLL without having first selected the Slow Clock or the Main Oscillator clock
- Select the PLL clock and, in the same register write, disable the PLL
- Select either the Main Oscillator or the PLL clocks and, in the same register write, disable the Main Oscillator
- Disable the Main Oscillator without having first selected the Slow Clock

This clock switch is performed in a certain number of Slow Clock and PLL or Main Oscillator clock cycles as described in the state machine diagram Figure 2.

Figure 2. Clock Switching



Clock Switching Considerations

The clock switching from one source to another must be achieved by using the dedicated interrupt named SLCKIRQ. The difficulty in clock switching is due to the fact that Advanced Power Management Controller operations are performed at 32 kHz in contrast to a faster clock for the software application (driven by a clock derived from the Main Oscillator or PLL output). The SLCKIRQ indicates when the Low Frequency Oscillator is used as the Master Clock.

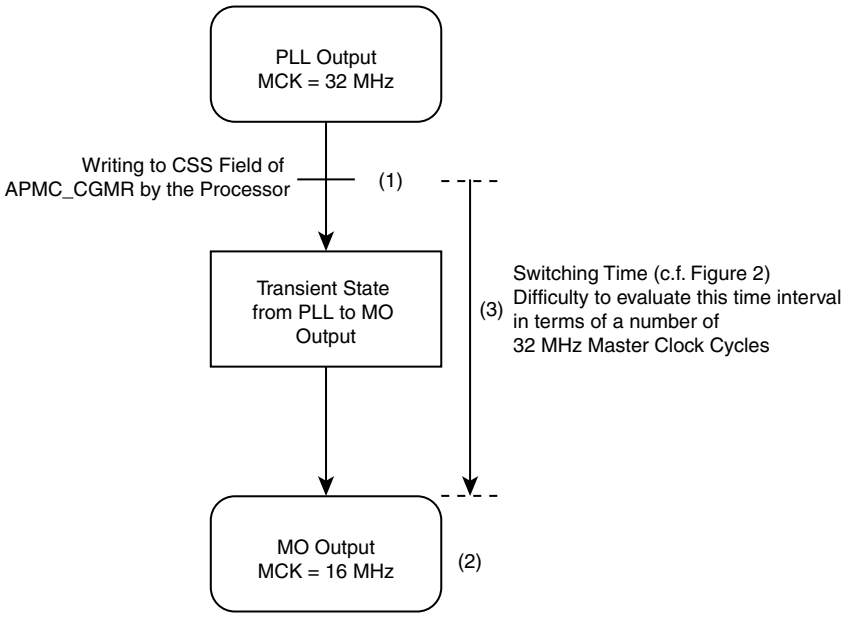
Example

The Main Oscillator is connected to a crystal oscillator of 16 MHz and the PLL is used to reach a frequency of 32 MHz.

Considering that the MCK clock is the PLL output at 32 MHz, the user wants to switch the MCK clock to the MO output at 16 MHz in order to reduce the power consumption in the application. To do this, the user sets the CSS field to the corresponding value (defined in Table 2) to select the MO output. Writing the CSS value is done at MCK = 32 MHz.

As previously described, the APMC is running at 32 kHz. The MCK frequency relative to the speed rate of the APMC state machine, is higher by a factor of 1000. In Figure 3, between (1) and (2), a number of 32.768 kHz clock cycles are needed for the APMC to switch the clock source, but related to the Master Clock, in this case 32 MHz, this time is very long. There is no flag informing the user when the APMC switch is finished, therefore the software application does not know when the APMC switch has been achieved.

Figure 3. Master Clock switching from PLL output to MO output.



Clock Switching Sequence Difficulties in a User Application

As described above, the clock source used to supply the internal Master Clock is selected according to the CSS field setting. To switch between the three different clock sources, the user must only write in the CSS field the corresponding choice to the targeted clock (see Table 2).

Each switching sequence is performed in a certain number of Slow Clock periods while the processor continues its work. During this period, the processor works at initial clock (see Figure 3, in step (3)).

The difficulty arises during this period when:

- the user wants to decrease the clock frequency and, for power saving considerations, wants to shu tdown the initial clock source as quickly as possible,
- or the user wants to switch between two high-frequency clock sources.

As described in “Clock Switching Considerations” on page 5, between the MCK clock frequency and the Slow Clock which drives the APMC state machine, it is possible to have a ratio of 1000 (between 32 Mhz and 32 kHz for example).

Without adequate precautions some problems can occur in the application, namely:

- the shutdown of the initial clock source can be performed during the step (3) (see Figure 3) while the processor is still working from it,
- errors in using other peripherals which work from the MCK (USART, Timer/Counter. etc.)

Clock Switching Sequence

The difficulty described above, when the application requires a clock frequency decreasing and a shutdown of the affected sources, can be easily resolved by using the interrupt called SLCKIRQ.

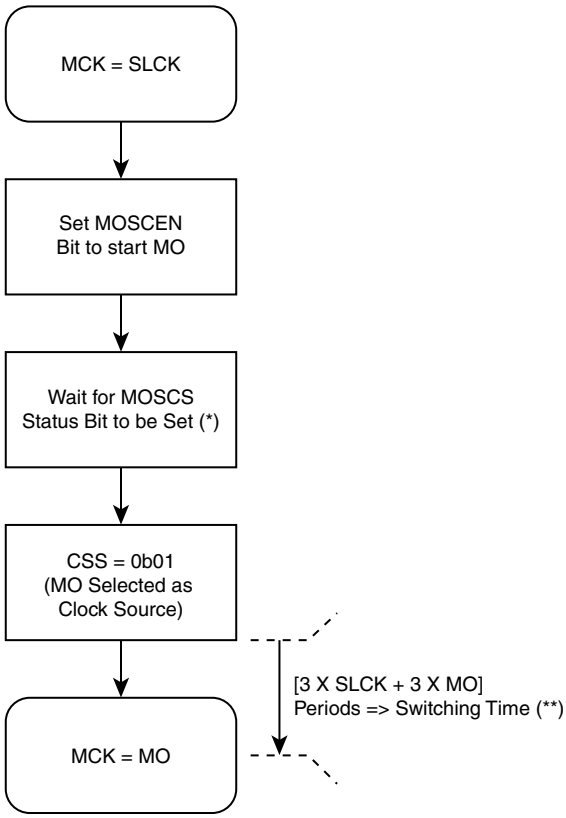
The recommended method is to carry out all switching while the Master Clock runs from the same source clock as the APMC i.e. 32.728 kHz.

The act of working from the Slow Clock allows the PLL or the Main Oscillator to be shut down safely.

In Figure 4 to Figure 9 are defined the different clock switching sequences using the method described above. There are three clock sources and therefore six switching sequences.

Note: In all following diagrams, we assume that the OSCOUNT and PLLCOUNT values have been correctly set according to, respectively, the Main Oscillator startup time and the PLL lock time.

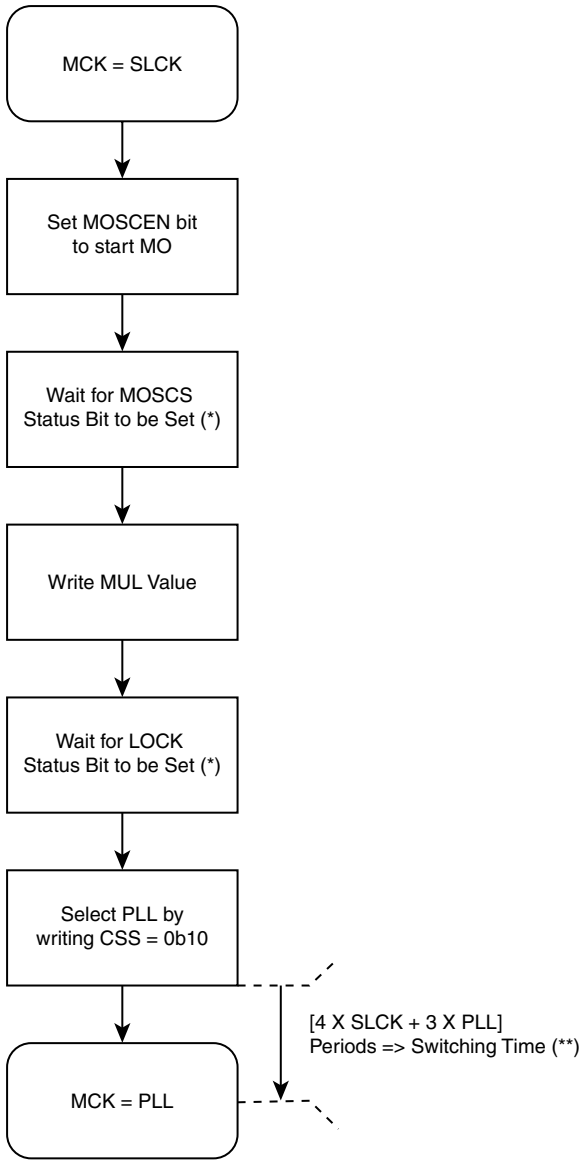
Figure 4. Switch MCK from Slow Clock oscillator output to MO output



(*) The AT91M55800A allows this event to be managed in interrupt mode (see AT91M55800A Datasheet)

(**) The processor runs at 32 kHz. Four machine code cycles are enough to overlay the necessary delay to achieve the switching.

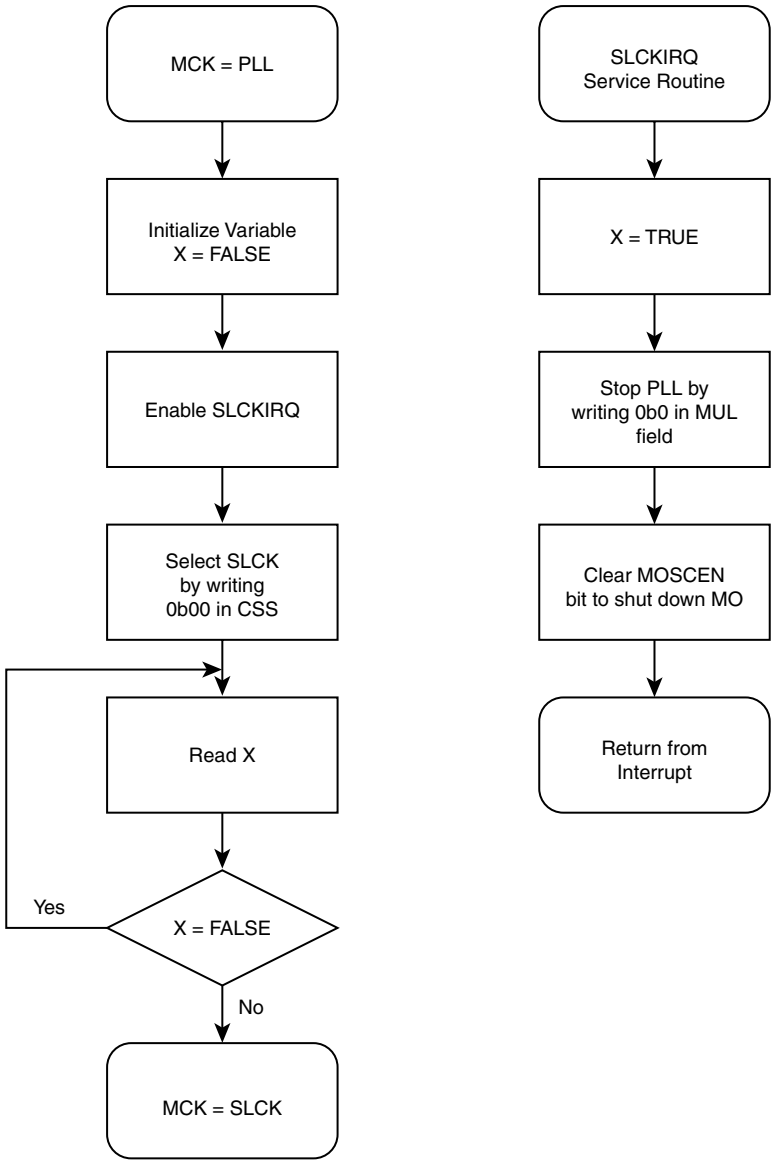
Figure 5. Switch MCK from Slow Clock oscillator output to PLL output



(*) The AT91M55800A allows these events to be managed in interrupt mode (see AT91M55800A Datasheet)

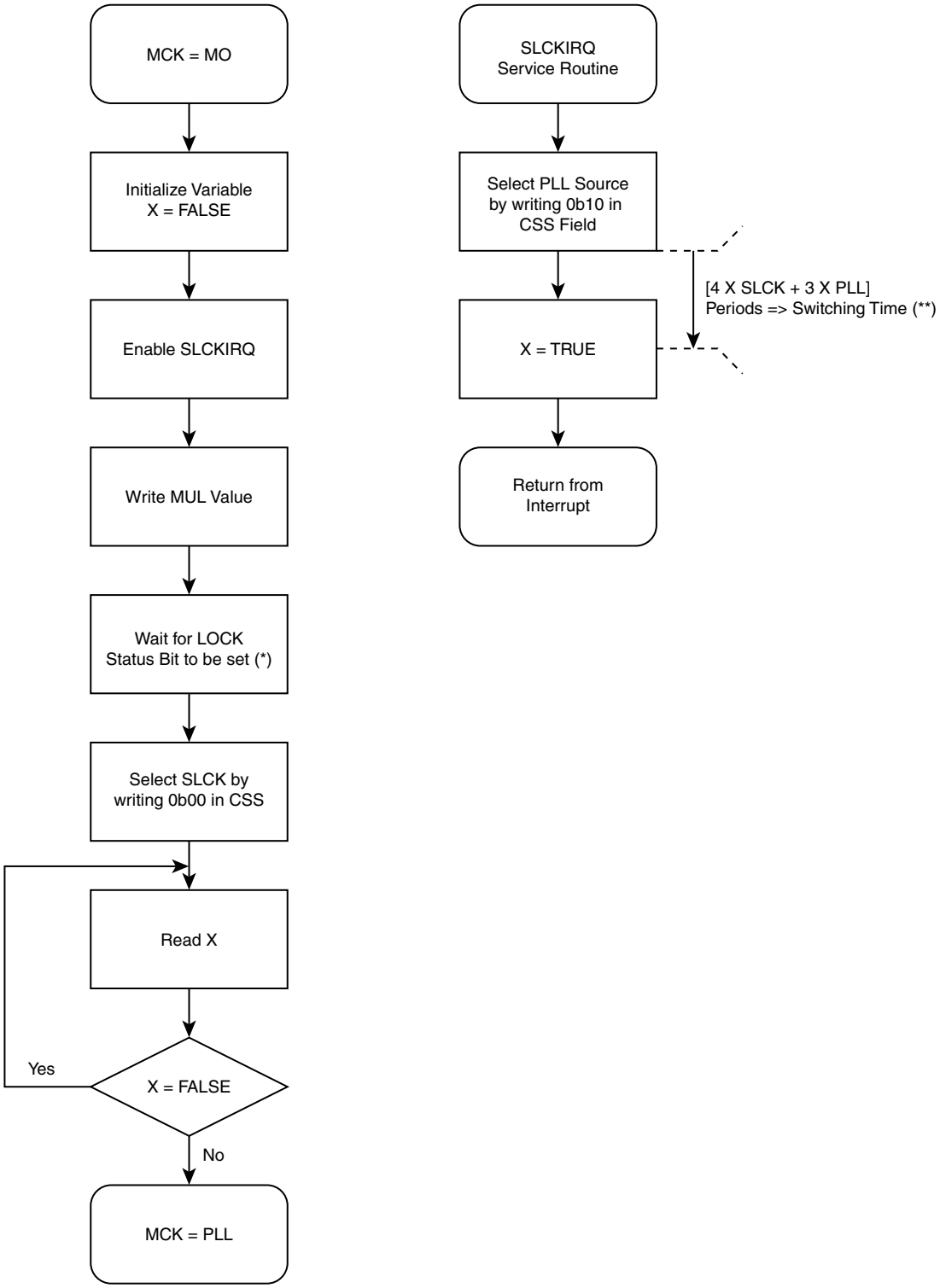
(**) The processor runs at 32kHz. Five machine code cycles are enough to overlay the necessary delay to achieve the switching.

Figure 6. Switch MCK from PLL output to Slow Clock oscillator output



The above transition works by using the SLCKIRQ interrupt. This is the reason why there are two sequences: one for the main sequence and other describing the interrupt subroutine.

Figure 7. Switch MCK from MO output to PLL output

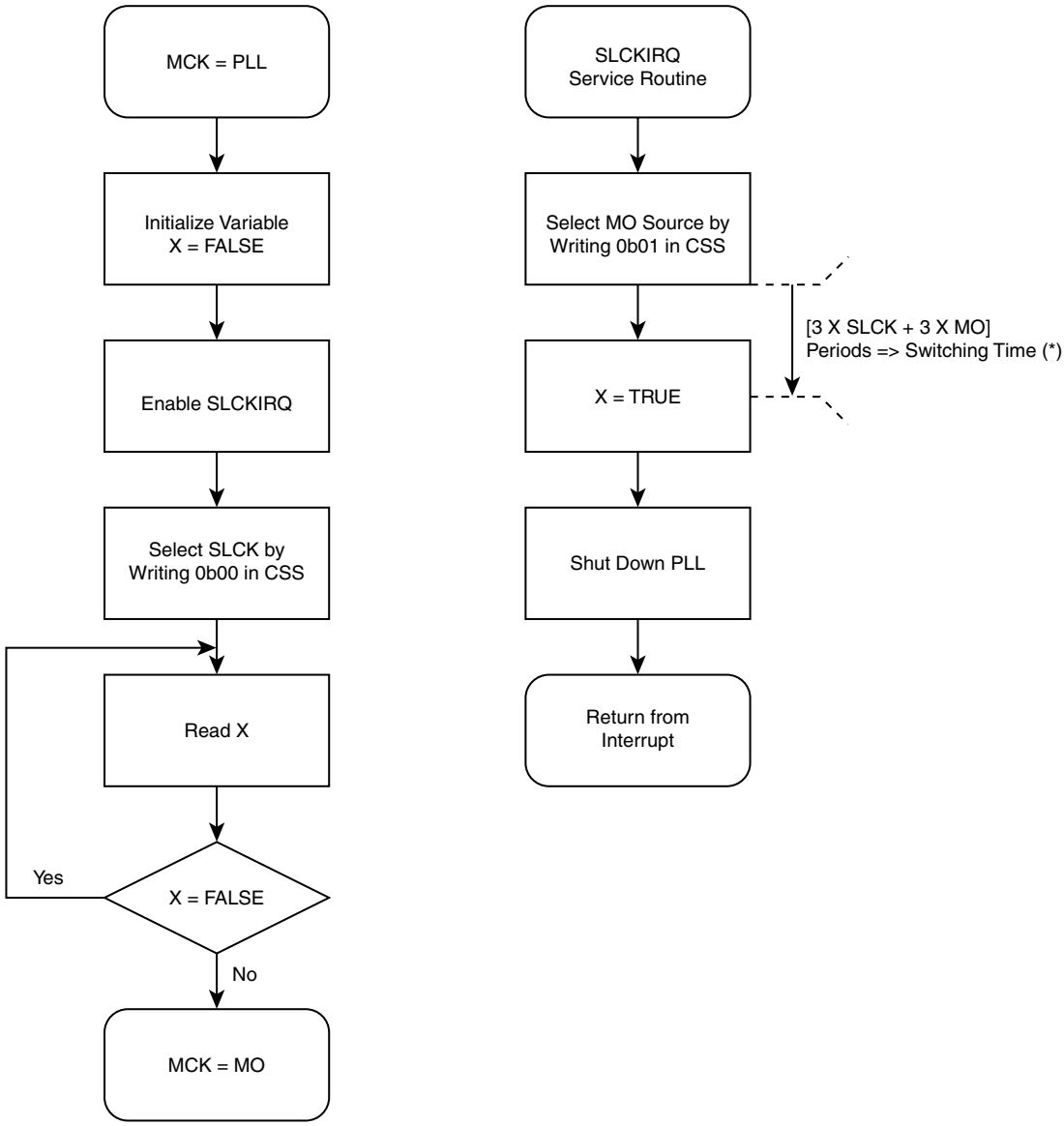


The above transition works by using the SLCKIRQ interrupt. This is the reason why there are two sequences: one for the main sequence and other describing the interrupt subroutine.

(*) The AT91M55800A allows this event to me managed in interrupt mode (see AT91M55800A Datasheet)

(**) In the SLCKIRQ subroutine, the processor runs at 32 kHz. In this case, some C code creates the necessary delay to achieve the switching.

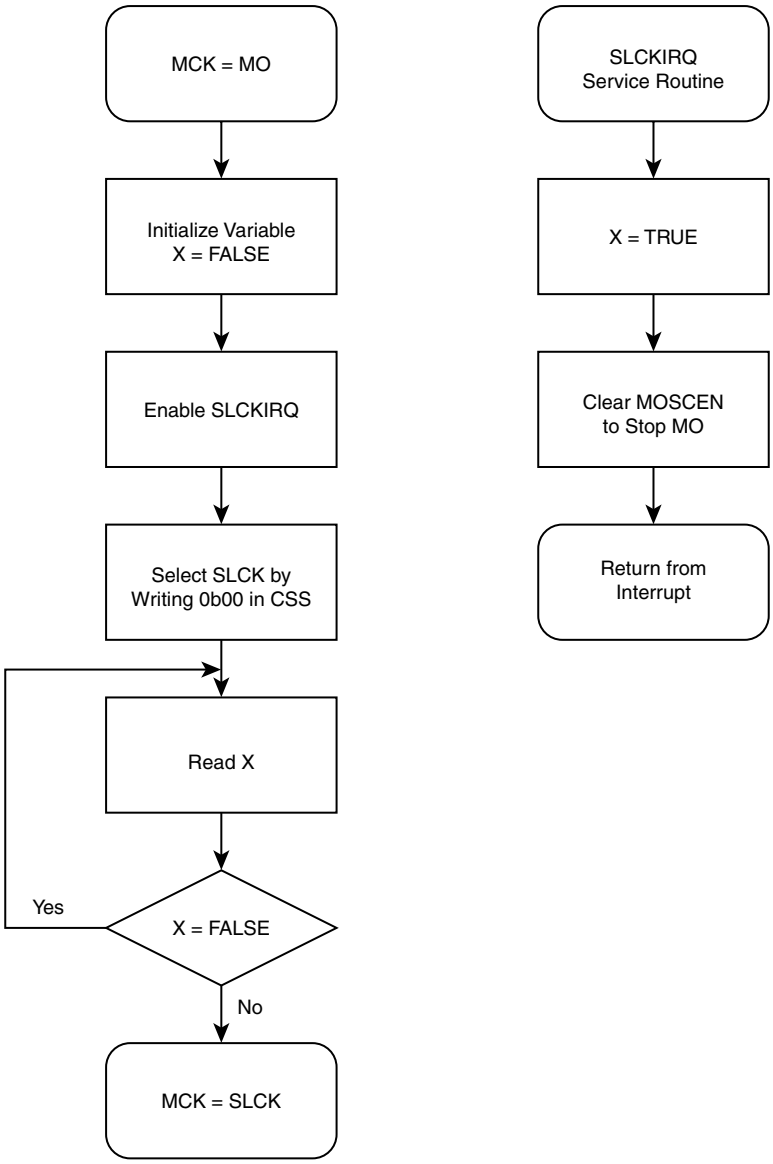
Figure 8. Switch MCK from PLL output to MO output



The above transition works by using the SLCKIRQ interrupt. This is the reason why there are two sequences: one for the main sequence and other describing the interrupt subroutine.

(*) The processor runs at 32 kHz. Four machine code cycles are enough to create the necessary delay to achieve the switching.

Figure 9. Switch MCK from MO output to Slow Clock oscillator output



The above transition works by using the SLCKIRQ interrupt. This is the reason why there are two sequences: one for the main sequence and other describing the interrupt subroutine.

Software Driver

Following the methods described in previous sections of this document, Atmel has developed a software driver to help the user to switch the Master Clock (MCK) of the AT91M55800A to the clock source selected: Slow Clock oscillator (SLCK), Main Oscillator (MO) or PLL.

This software is built around a C source file named *clock_switching_driver.c* and its corresponding header file, *clock_switching_driver.h*.

The user interface is defined by two functions, *mck_clock_speed()* and *at91_clock_generator_state()* defined in the *clock_switching_driver.c* module.

Examples

1. The user wants to select the Main Oscillator output. The required function call is:

```
mck_clock_speed (TO_HF_OSCILLATOR , 0 ) ;
```

where the parameters are:

TO_HF_OSCILLATOR: is a constant defined in the header file and used to select the targeted clock source (the MO in this example),

0: The PLL factor.

2. The user wants to select the Low Frequency Oscillator output. The required function call is:

```
mck_clock_speed (TO_LF_OSCILLATOR , 0 ) ;
```

where the parameters are:

TO_LF_OSCILLATOR: is a constant defined in the header file and used to select the targeted clock source (the SLCK in this example),

0: The PLL factor.

3. 3) The user wants to select the PLL output. The required function call is:

```
mck_clock_speed (TO_PLL_OSCILLATOR , Frequency_multiplier ) ;
```

where the parameters are:

TO_PLL_OSCILLATOR: is a constant defined in the header file and used to select the targeted clock source (the PLL in this example),

Frequency_multiplier: The PLL factor.

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