Crystal Oscillator and PLL Considerations for AT91M42800A and AT91M55800A

AT91 ARM® Thumb® Microcontrollers

Application Note

Crystal oscillators use an external crystal to generate clock signals for designs that require high stability at a precise frequency. Phase-locked-loops are used to multiply the crystal output frequency to higher values. This application note describes the use of Crystal Oscillator and PLLs in the context of the AT91M42800A and AT91M55800A ARM-based microcontrollers.

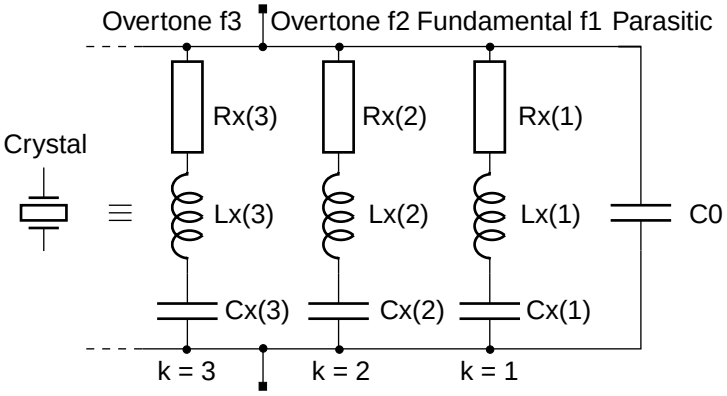
Associated Spreadsheet File

The ZIP file “Automatic_Calculation_xls.zip” should be downloaded from the Software section of the AT91 pages on Atmel’s web site and unzipped. It gives a spreadsheet that is programmed to perform the calculations described in this application note.

Crystal Theory

The mechanical impedance of a crystal for one particular series resonant frequency *k* (the fundamental and its overtones) can be electrically modelled by a series RLC resonant circuit. See Figure 1.

Figure 1. Electrical Model of the Mechanical Impedance of a Crystal



The parasitic capacitance of the crystal’s electrodes and the package are modelled by the capacitor C_0. Together with the motional inductance *Lx(k)* this capacitor forms resonant circuits that also produce parallel resonant frequencies *fp(k)*. They cannot be used for oscillation with the type of oscillators presented here.

Rev. 1740A–09/01

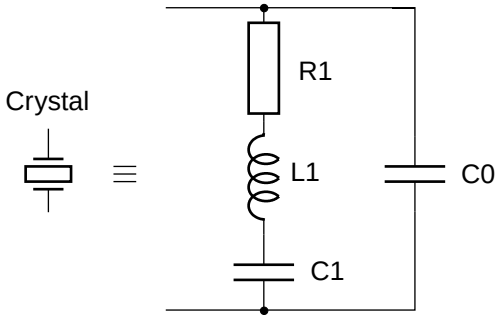
For a realistic crystal model, the quality factor *Q(k)* for the series resonators decreases for the overtone frequencies:

$$Q(k) = \frac{1}{2\pi \cdot fx(k) \cdot Cx(k) \cdot Rx(k)}$$

$$Q(k+1) < Q(k)$$

So if the crystal is used in its fundamental mode (k = 1) or for an overtone, the other modes (overtones) can be neglected and the crystal can be modelled by only one single series RLC resonant circuit. See Figure 2.

Figure 2. Electrical Model Simplified (k = 1)



This model can be associated to the crystal manufacturers' parameters. SeeTable 1.

Table 1. Crystal Parameters

Parameter	Symbol	Unit
Nominal Frequency	F	kHz or MHz
Load Capacitance	C_L	pF
Motional Inductance	L_1	H
Motional Capacitance	C_1	fF
Motional Resistance	R_1	Ω or kΩ
Shunt Capacitance	C_0	pF

Using the electrical model, the main parameters of a crystal can be extracted:

Resonant Frequency *fx*:

$$fx = \frac{1}{2\pi\sqrt{Cx \cdot Lx}}$$

Quality Factor *Qx*:

$$Qx = \frac{1}{2\pi \cdot fx \cdot Cx \cdot Rx}$$

Mechanical Impedance $\underline{Zx}$:

$$\underline{Zx} = Rx + j\frac{1}{2\pi \cdot fx \cdot Cx}\left(\frac{f}{fx} - \frac{fx}{f}\right)$$

The critical parameter for frequency stability of any oscillation is the frequency pulling *P*, which is defined as the relative drift of the current frequency *f* from the resonant frequency *fx*:

Frequency Pulling *Px*:

$$Px = \frac{f - fx}{fx}$$

$$\underline{Zx} = Rx + j\frac{2Px}{2\pi \cdot f \cdot Cx}$$

Oscillator Theory

Because a crystal has natural losses, which are expressed by the resistance *Rx* in the model, it is impossible for the crystal itself to build up an oscillation. An oscillator circuit has to be used to apply an impedance *Zc* to the crystal that compensates *Rx*. The critical condition for oscillation can be achieved by comparing the real components of the impedance of crystal and oscillator:

$$-Re[Zc] = Rx$$

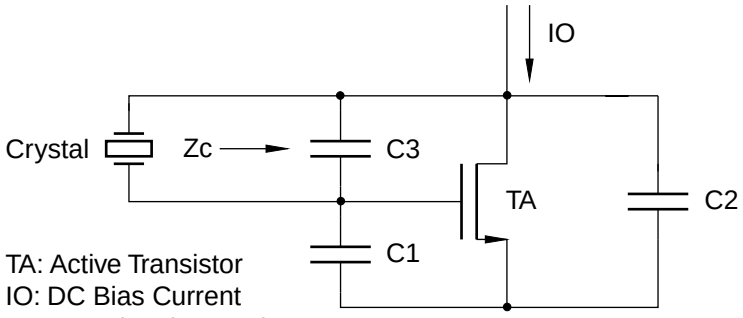
As soon as *-Re[Zc]* is larger than *Rx*, an oscillation builds up exponentially in the crystal, until its amplitude is limited by non-linearity or additional regulation circuitry. The time constant *T* for oscillation to build up depends on both the crystal and the oscillator impedance:

$$T = \frac{-Lx}{Re[Zc] + Rx} = -\frac{1}{\omega^2 Cx(Re[Zc] + Rx)}$$

Pierce Three-point Oscillator

The typical oscillator circuit for a crystal is the Pierce Three-point Oscillator. The negative resistance is obtained by one active transistor and two functional capacitances. The basic circuit with its connections to the crystal is shown in Figure 3.

Figure 3. Basic Three-point Oscillator Circuit



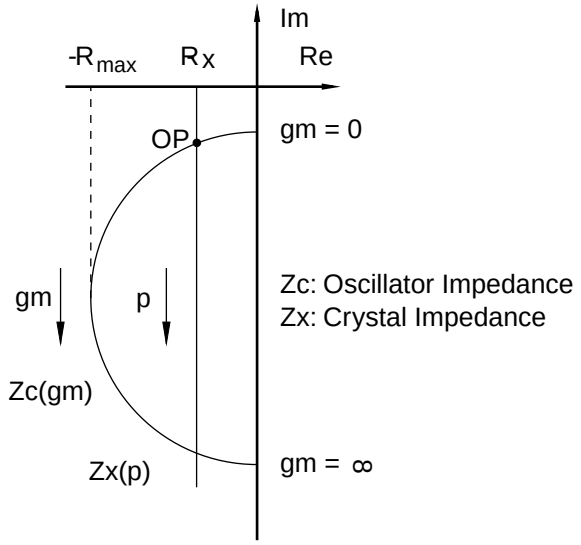
C_3 is a parasitic capacitance that includes package capacitance of the crystal (C_0), board capacitance and internal parasitic of the oscillator circuit such as the Miller

Capacitance of the active transistor. C_1 and C_2 are the functional capacitances, also containing external parasitic. The possible range of the transconductance *gm* of the transistor is determined by the bias current I0 and the aspect ratio of the transistor. The active transistor can be replaced by a CMOS inverter that does not need additional bias circuitry, which is often required for high frequency oscillators. The impedance *Zc* is obtained as follows:

$$-Re[Zc] = \frac{gmC_1C_2}{(gmC_3)^2 + \varpi^2(C_1C_2 + C_1C_3 + C_2C_3)^2}$$

$$-Im[Zc] = \frac{gm^2C_3 + \omega^2(C_1 + C_2)(C_1C_2 + C_1C_3 + C_2C_3)^2}{\omega((gmC_3)^2 + \omega^2(C_1C_2 + C_1C_3 + C_2C_3)^2)}$$

Figure 4. Complex Plane Representation of the Impedances *Zc* and *Zx*



The complex plane representations of *Zc* as a function of *gm* and of the crystal impedance *Zx* as a function of its frequency pulling *P* are shown in Figure 4. The formula for the real and imaginary parts of *Zc* are also given. The two intersections of *Zc* and *Zx* are the possible operating points of the circuitry, according to the critical condition for oscillation.

However, it has been shown that the point labeled OP is the only solution with stable conditions and therefore the only operating point. As already explained, for a safe startup of oscillation the real part *-Re[Zc]* has to be larger than *Rx*. Normally a value of *2*Rx* is chosen for the worst case condition.

If the parasitic capacitance C_3 is negligible, the formula for *Zc* can be simplified.

If C_1, $C_2 >> C_3$:

$$-Re[Zc] = \frac{gmC_1C_2}{(gmC_3)^2 + (\omega C_1C_2)^2}$$

$$-Im[Zc] = \frac{gm^2C_3 + \omega^2(C_1 + C_2)C_1C_2}{\omega((gmC_3)^2 + (\omega C_1C_2)^2)}$$

If $C_3 = 0$:

$$-Re[Zc] = \frac{gm}{\omega^2 C_1 C_2}$$

$$-Im[Zc] = \frac{C_1 + C_2}{\omega C_1 C_2}$$

The complex plane representation also shows that there is a maximum negative resistance R_{MAX} for *Rx*. Above this value no operating point can be achieved because the two curves no longer intersect:

$$-R_{MAX} = \frac{1}{2\omega C_3\left(1 + C_3\frac{C_1 C_2}{C_1 + C_2}\right)}$$

In the range from *Rx* to R_{MAX} the frequency pulling depends only on the capacitances of the circuitry and can be decreased by an increase of the two functional capacitances C_1 and C_2:

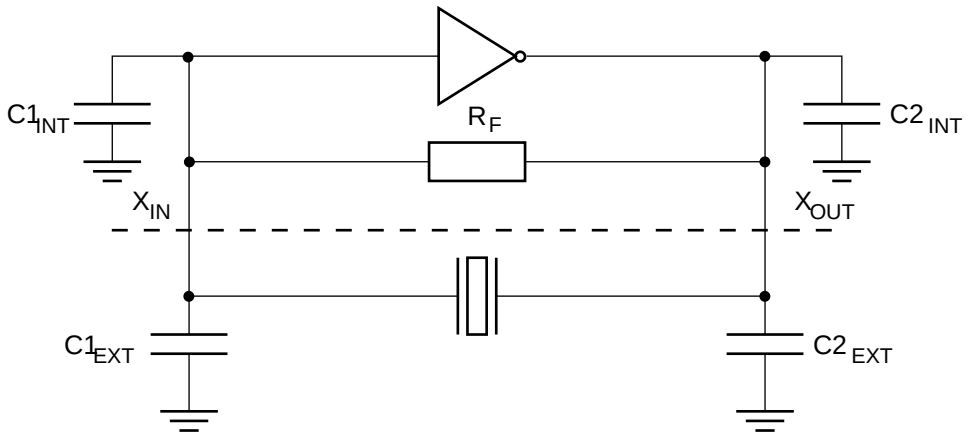
$$Px = \frac{Cx}{2\left(C_3 + \frac{C_1 C_2}{C_1 + C_2}\right)}$$

Implementation

Figure 5 shows schematically the implementation of the Pierce oscillator circuit. It can be used to calculate the necessary external capacitances, the impedance *Zc* and all other values using the electrical parameters of the cell and the crystal. The oscillator cells of the AT91M42800A and AT91M55800A are implemented as normal three-point circuits, using one active transistor to obtain the negative resistance.

The functional capacitors $C1_{INT}$ and $C2_{INT}$ are implemented in the cells on-chip. The bias resistor R_F is an internal resistance required to force the transistor into its active mode. Its value is very high to avoid degrading the frequency stability and increasing the current.

Figure 5. Pierce Oscillator Overview



Frequency Considerations

We can define two types of frequency considerations that depending on the way the circuit is connected externally:

- the frequency accuracy
- the frequency stability.

The accuracy is the oscillator's capacity to run at a specific frequency. Generally, it demands that the oscillator characteristics (principally the load capacitance) are matched according to the crystal manufacturer's specifications.

The stability is the oscillator's capacity to keep this frequency stable. This means that the previous rule stays true during the operating cycle.

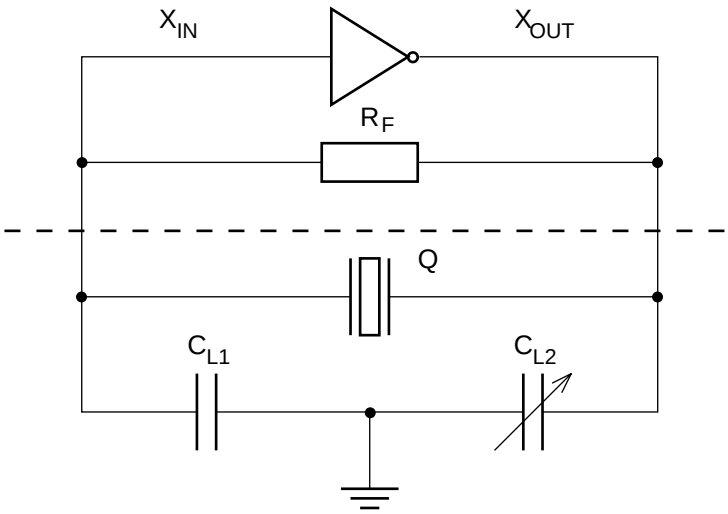
In order to have the minimum variation on the output frequency ($\Delta f/f$), the parasitic capacitances on the PCB (X_{IN} - GND, and X_{OUT} - GND) should be estimated or measured. If they are significant less external capacitance should be added.

For example, suppose that two parasitic capacitances of 3 pF have been found on the PCB, the crystal has a load capacitance of 12.5 pF. Thus, two 22 pF external capacitances on X_{IN} - GND, and on X_{OUT} - GND should be used to compensate the mismatch.

Add a capacitance in the feedback path of oscillator (in parallel with the crystal) also to compensate the mismatch, but derate the performance of this capacitance, rather than adding two external capacitors as above. The start-up time will increase in both cases, but not in the same proportions. Moreover, the crystal oscillator could possibly not start, or start on another harmonic of the 32.768 kHz oscillator.

One of the two external capacitors could be trimmed in order to have exactly the nominal frequency. See Figure 6.

Figure 6. Variable Load Capacitance



The resultant load capacitance C_L is given from C_{L1} and C_{L2} by the following formula:

$$C_L \cong \frac{(C_{L1}C_{L2})}{(C_{L1} + C_{L2})}$$

where:

C_{L1} is the equivalent load capacitance seen on X_{IN} pin (with all stray capacitances),

C_{L2} is the equivalent load capacitance seen on X_{OUT} pin (with all stray capacitances) and

C_L is the resultant load capacitance.

C_L specifies the load capacitance that must be placed across the crystal pins in order for the crystal to oscillate at its specified frequency.

Any change in the load capacitance of the oscillator circuit will have an effect on the frequency of the oscillator. In general, using a crystal with a C_L larger than the load capacitance of the oscillator circuit will cause the oscillator to run faster than the specified nominal frequency of the crystal. Inversely, using a crystal with C_L smaller than the load capacitance of the oscillator circuit will cause the oscillator to run slower than the specified nominal frequency of the crystal.

Approximately, the real running frequency f_L with a given capacitance is given by the following formula:

$$f_L = f_S\left(1 + \frac{C_1}{2(C_L + C_0)}\right)$$

where:

C_L is the real load capacitance on the crystal (with stray capacitance),

C_0 is the shunt capacitance and

f_S is the serial resonance frequency.

Noise and Crystal Guidelines

If one or both oscillator inputs have very high impedance (about 10^8 Ω), the crystal acts like an antenna, coupling high frequency signals from the rest of the system. If this signal is coupled onto the crystal pins, it can either cancel out or add pulses. The 32.768 kHz oscillator is the most critical.

In some applications where most of the signals on a board have frequency higher than the 32.768 kHz crystal, the high frequency signals add pulses where none are wanted. These noise pulses are counted as extra clock “ticks” and make the clock appear to run faster.

It is also possible for noise to be coupled onto the crystal pins, thus care must be taken when placing the crystal on the PCB layout. It is very important to follow a few basic layout guidelines concerning the connection of the crystal on the PCB layout to insure that extra clock “ticks” are not coupled onto the crystal pins. These are as follows:

1. It is important to place the crystal as close as possible to the X_{IN} and X_{OUT} pins. Keeping the track lengths between the crystal and the oscillator as short as possible reduces the probability of noise by reducing the length of the antenna. Keeping the track lengths short also decreases the amount of stray capacitance.
2. Keep the crystal bond pads and track width to the X_{IN} and X_{OUT} pins as narrow as possible. Increased width of these bond pads and tracks causes increased coupling with noise from adjacent signals.

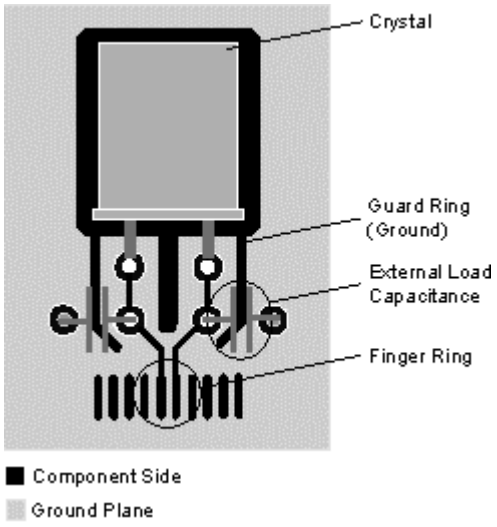
3. If possible, place a guard ring (tied to ground) around the crystal. This helps to isolate the crystal from noise coupled from adjacent signals. See Figure 7 for an illustration of using a guard ring around a crystal.

   Try to insure that no signals on other PCB layers run directly below the crystal or below the tracks to the X_{IN} and X_{OUT} pins. Isolating the crystal from other signals on the board decreases the noise that is coupled.

4. It may also be helpful to place a local ground plane on the PCB layer immediately below the crystal guard ring. This helps to isolate the crystal from noise coupling from signals on other PCB layers. Note that the ground plane needs to be in the vicinity of the crystal only and not on the entire board. See Figure 7 for an illustration of a local ground plane. Note that the perimeter of the ground plane does not need to be larger than the outer perimeter of the guard ring.

5. It is important to uncouple on the PCB the supply of the crystal oscillator from the noise of digital supplies (I/O, core), and from switching noise.

Figure 7. Board Design Example (Top View)



Low Power Considerations

The AT91 ARM-based microcontrollers can have one or two on-chip oscillators. The AT91M42800A has one low frequency oscillator (typically 32.768 kHz) and the AT91M55800A has two oscillators, the low frequency oscillator (same as AT91M42800A) and a high frequency oscillator (3 to 20 MHz).

These oscillators are used for specific functions. See Table 2.

Table 2. Oscillator Functions

Oscillator	Function
Low Frequency	RTC Clock Source
High Frequency	CPU and Peripheral Clock Source

The AT91M55800A Advanced Power Management Controller allows optimization of power consumption. The APMC enables/disables the clock inputs of most of the peripherals and the ARM core. Moreover, the main oscillator, the PLL and the analog peripherals can be put in standby mode allowing minimum power consumption to be obtained.

In standby mode, the RTC is still active and all others clock are disabled. This provides a typical power consumption below than 1µA. This is useful for battery powered applications.

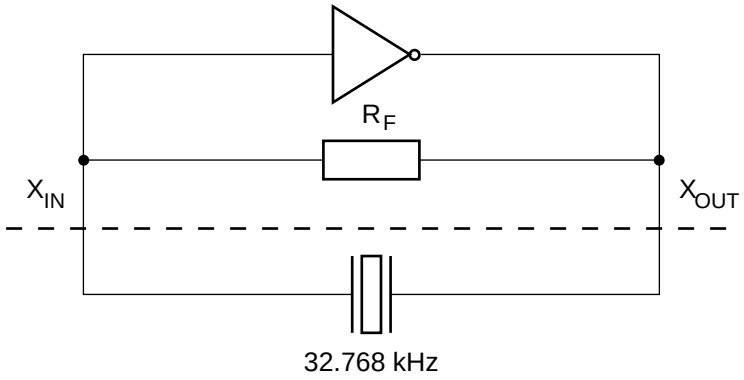
The AT91M42800A has one on-chip oscillator, at low frequency. The high frequency clock is provided by frequency multiplication using PLLs. The Power Management Controller optimizes the power consumption of the device. The PMC controls the clocking elements such as the oscillator, PLLs, system and the peripheral clocks

Typical Applications for the AT91M42800A Oscillator

The AT91M42800A's on-chip oscillator has a typical running frequency of 32.768 kHz (38.4 kHz crystal) and its power consumption is approximately 9 µA. Figure 8 shows the typical oscillator connection. The internal load capacitance is 10 pF (20 pF on each pin). For the Crystal Oscillator Characteristics, See "AT91M42800A Crystal Oscillator Characteristics" on page 16.

If needed the load capacitance can be adjusted with two external capacitances. See Figure 9.

Figure 8. AT91M42800A Oscillator

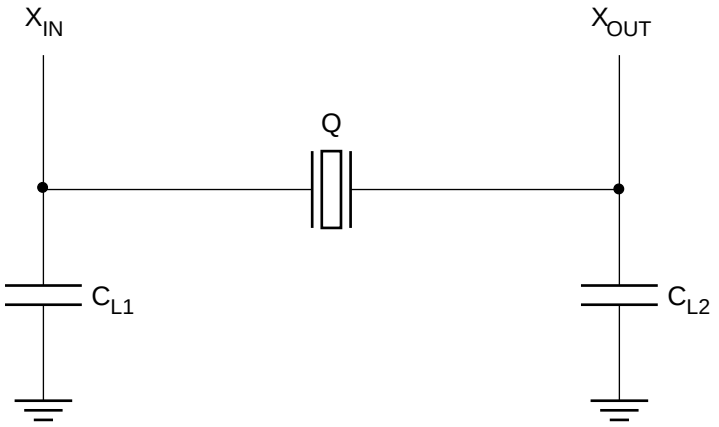


Typical Applications for the AT91M55800A Oscillators

The AT91M55800A has two on-chip oscillators, a low frequency oscillator (refer to AT91M42800A oscillator) and a main oscillator with a frequency range from 3 to 20 MHz. The low frequency oscillator has a typical power consumption less than 1 µA and its internal load capacitance is 6 pF (12 pF on each pins). The main oscillator has a typical power consumption of 200 µA and its internal load capacitance is 12.5 pF (25 pF on each pin).

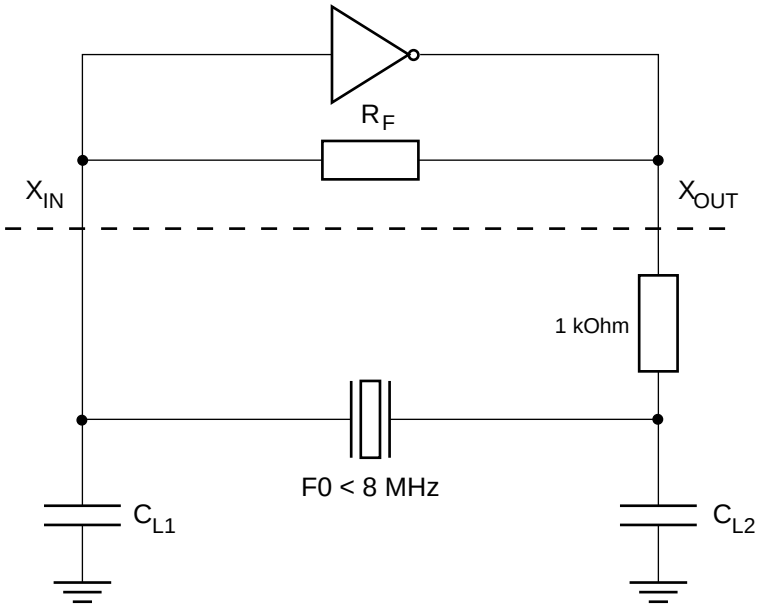
The load capacitance can also be adjusted if needed. See Figure 9. For the Crystal Oscillator Characteristics, See "AT91M55800A Crystal Oscillator Characteristics" on page 16.

Figure 9. Capacitance Adjustment



Note: For applications using a crystal that has a fundamental frequency of less than 8 MHz, a resistor of 10 kΩ must be connected to the X_{OUT} pin as shown in Figure 10.

Figure 10. Main Oscillator with Frequency Less Than 8 MHz



PLL Overview

Phase-locked-loop cells are designed to synchronize an internal chip clock signal with an input reference clock. All Atmel PLL cells require an external RC filter.

PLL Theory

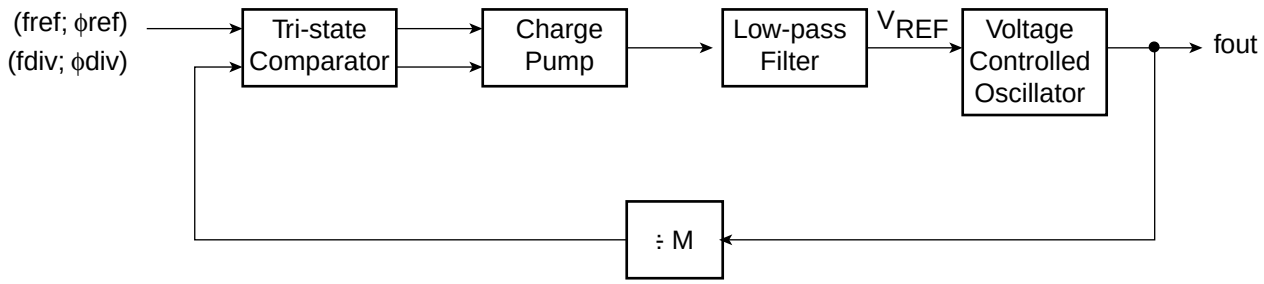
An Atmel PLL is made up of four blocks:

- Phase comparator, which measures the phase difference between two clocks, one of which is the reference clock, provided externally. The phase comparator also provides phase difference information through the lock pin.
- Charge pump and loop filter, which convert the phase comparison result into a command for the VCO.
- VCO, which creates the derived clock.

- The divider, which creates a divided clock from the derived clock. This divided clock is compared with the reference clock.

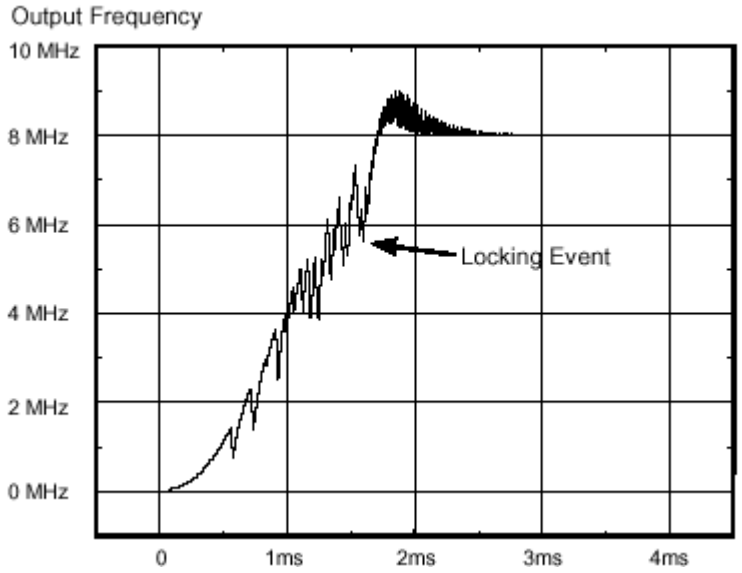
The schematic in Figure 11 represents the internal structure of the PLL.

Figure 11. PLL Block Diagram



The VCO frequency evolves as a function of the phase comparison operation. The goal is to reach the desired frequency quickly with minimal skew with regard to the reference clock. Thus a PLL is a system which adjusts two variables (phase and frequency) according to a single error measurement (phase difference). The decision to accelerate or to reduce the frequency is made on the basis of a phase comparison. This process continues until a stable cycle is achieved. The result is an oscillatory process, which should converge around the target value if loop stability is ensured. This converging process can be split into two steps. Before locking, the overall behavior of the PLL is chaotic and no exact prediction can be made. After locking, the PLL behaves on average like a linear system and general system theories can be used to predict its behavior. See Figure 12.

Figure 12. Transient Response of a Charge-PLL



As a result of the oscillatory process as described above, during the lock period of the PLL the derived clock frequency may vary significantly with respect to the target fre-

quency. It is possible to reduce the frequency variance by tuning the loop filter within certain limits imposed by simplicity of the RC filter, range of the VCO, reasonable convergence time, stability, noise immunity and range of target derived frequencies to be supported.

PLL Block Descriptions

Phase Frequency Comparator and Lock Detector (PFLD)

The Atmel Phase Frequency Comparator is a three-state digital comparator. This block makes the comparison between the reference clock and the output clock to detect the phase skew between them:

$$\varphi_e = \varphi_{ref} - \varphi_{div}$$

Charge Pump (CP)

The Charge Pump is the driver of the external filter. It injects charges into the external RC filter. In this way, the charge pump controls the reference voltage V_{ref} that monitors the Voltage Controlled Oscillator (VCO): when a positive current injects charges into the filter, V_{ref} and the VCO frequency increase; when a negative current extracts charges from the filter, V_{ref} and the VCO frequency decrease.

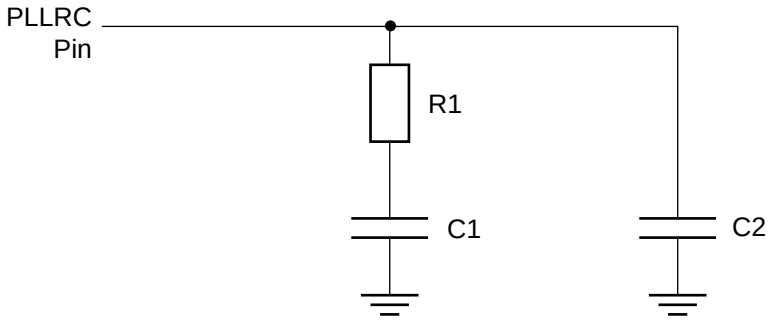
$$\frac{I_d}{\varphi_e} = \frac{I_p}{2\pi} = K_d$$

where K_d is the PFLD/CP group gain and I_p is the peak current delivered by the charge pump into the filter.

Loop Filter

The Loop Filter is an external part of the chip. The typical RC network that must be connected to the PLLRC pin is a single capacitor in series with a resistor connected to ground. In order to reduce ripples, an additional capacitor C_2 is added in parallel to the RC network. The values of these components impact on the stability of the PLL, the lock-in time and the output jitter (variation of duration of a clock period). See Figure 13.

Figure 13. Loop Filter



The filter's purpose is to transform the $I_d(t)$ current issued from PFLD/CP block into a voltage $V_{ref}(t)$:

$$\frac{V_{ref}(t)}{i_d(t)} = f(t)$$

where $f(t)$ is the filter gain.

Voltage Controlled Oscillator (VCO)

The built-in Voltage Controlled Oscillator is the local oscillator that is controlled by the voltage V_{ref} produced by the Charge Pump. The linearity hypothesis on the Voltage-frequency characteristic of the VCO gives the relationship:

$$f_{out} = K_0 V_{ref}(t) + f_{v0}$$

with K_0 the VCO gain or sensibility expressed in Hz/V and f_{v0} the frequency at origin.

Filter Component Calculation

Due to the disparity of certain parameters like:

- I_p Charge Pump current
- K_0 VCO gain

and also due to the non-linearity of the response before locking, this Application Note estimates values of the R_1, C_1 and C_2 components in order to have stable behavior of the Phase-locked-loop.

Determination of C_1 and C_2

This approximation can be made if the natural oscillation loop:

$$\omega_n = 2\pi f_n$$

respects the following inequality:

$$\omega_n < \frac{\omega_{ref}}{20}$$

with:

$$\varpi_{ref} = 2\pi f_{ref}$$

and:

$$\omega_n = \sqrt{\frac{K_0 I_p}{M(C_1 + C_2)}}$$

This gives the system a good stability margin:

$$C_1 + C_2 \geq \frac{K_0 I_p}{M\left(\frac{\omega_{ref}}{20}\right)^2}$$

We choose the case where:

$$C_1 + C_2 = \frac{K_0 I_p}{M\left(\frac{\omega_{ref}}{20}\right)^2}$$

Note: This choice is made by supposing a second order behavior, so the value of the C_2 capacitance should be chosen so that:

$$C_2 \leq \frac{C_1}{10}$$

We choose the value:

$$C_2 = \frac{C_1}{10}$$

Determination of R_1

In the conditions defined above we can compare the behavior of the PLL as a second order system loop. In this case, R_1 has an influence on the dumping factor ζ:

$$\zeta = \frac{R_1 C_1}{2} \cdot \sqrt{\frac{K_0 I_p}{M(C_1 + C_2)}}$$

The optimum response filter is obtained when:

$$0.4 \leq \zeta \leq 1$$

with an optimum value of:

$$\frac{\sqrt{2}}{2}$$

Example for $\zeta = 1$:

$$R_1 = \sqrt{\frac{4M(C_1 + C_2)}{K_0 I_p C_1^2}}$$

The numeric values of K_0 and I_p for the AT91M42800A and AT91M55800A microcontrollers are specified later. See “AT91M42800A PLL Characteristics” on page 17. Also See “AT91M55800A PLL Characteristics” on page 17.

Automatic Calculation of R_1, C_1 and C_2

The AT91 Application Group has developed Excel files to compute the external components for the PLL loop filter. Spreadsheets “Automatic Calculation (AT91M42800A).xls” and “Automatic Calculation (AT91M55800A).xls” are available on the AT91 CD-ROM and can be downloaded from the Software section of the AT91 pages of Atmel’s web site, from the file “Automatic_Calculation_xls.zip”. To use these the user needs to complete the following fields:

- Oscillator frequency
- Target frequency
- Choose PLLA or PLLB for the AT91M42800A

The spreadsheet then computes the R_1, C_1 and C_2 component values, the multiplier ratio to put in the MUL bits (defined below) and the delay time for the PLL count register.

AT91M42800A and AT91M55800A PLLs

The AT91M42800A and AT91M55800A microcontrollers contain two types of PLL:

- The PLLA to reach a clock frequency up to 16 MHz
- The PLLB to reach a clock frequency up to 33 MHz

The AT91M42800A has two PLLs, PLLA and PLLB whereas the AT91M55800A has only one PLL, PLLB. For both parts, there is a dedicated pin for the PLL Loop filter. This dedicated pin is an output for the Charge Pump and also an input for the VCO.

Note: It is possible to not use the PLL, but the dedicated pin must be set to the reference voltage (to avoid stray oscillations from the VCO).

The AT91 PLLs’ purpose is to provide an easy way to modify the internal clock frequency by changing a value contained in a single register of the microcontroller.

For the AT91M42800A, this value is defined by the MUL bits of PMC_CGMR register (see Datasheet, “Power Management Controller”) and for the AT91M55800A, the MUL bits in APMC_CGMR register (see Datasheet, “Advanced Power Management Controller” in the Datasheets section of the Complex ASIC Cores pages of Atmel’s web site).

PLL Set-up Time

The PLL transient behavior before mathematical locking (phase error between the reference signal and derived signal less than ±2π), is complex and difficult to describe using simple mathematical expressions. Thus, there is no general formula giving the set-up time for any step-response transient behavior that unlocks the loop. Nevertheless, this set-up time can be approximated by a simple loop filter capacitor charging time T_{setup} in the worst case:

$$T_{setup} \leq \alpha \cdot \left[\frac{C_1 + C_2}{I_p}\right] \cdot \frac{VDDPLL}{2}$$

where:

C_1 and C_2 are the loop filter capacitors,

I_p the charge pump current,

α is a margin factor, set it to 3 or 4 as a minimum and

VDDPLL/2 (approximately equal to 1.6V) is chosen because the PLL's VCO operates linearly.

This formula over-estimates the required time, but gives an easy way to approximate this set-up time.

AT91M42800A Crystal Oscillator Characteristics

Table 3. Low Frequency Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$1/(t_{CPRTC})$	Crystal Oscillator Frequency			32.768		kHz
C_{L1}, C_{L2}	Internal Load Capacitance ($C_{L1} = C_{L2}$)			20		pF
C_L	Equivalent Load Capacitance	$C_{L1} = C_{L2} = 12$ pF		10		pF
	Duty Cycle	Measured at MCK0 output pin	45	50	55	%
t_{ST}	Startup Time	$V_{DDBU} = 1.8V$ no capacitor connected to the RTC oscillator pins (X_{IN32}, X_{OUT32})			1.5	s

AT91M55800A Crystal Oscillator Characteristics

Table 4. RTC Oscilator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$1/(t_{CPRTC})$	Crystal Oscillator Frequency			32.768		kHz
C_{L1}, C_{L2}	Internal Load Capacitance (C_{L1} - C_{L2})			12		pF
C_L	Equivalent Load Capacitance	$C_{L1} = C_{L2} = 12$ pF		6		pF
	Duty Cycle	Measured at MCK0 output pin	45	50	55	%
tST	Startup Time	$V_{DDBU} = 1.8V$ No capacitor connected to the RTC oscillator pins (X_{IN32}, X_{OUT32})			240	ms

Table 5. Main Oscillator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$1/(t_{CPRTC})$	Crystal Oscillator Frequency		3	16	20	MHz
C_{L1}, C_{L2}	Internal Load Capacitance (C_{L1} - C_{L2})			25		pF
C_L	Equivalent Load Capacitance	$C_{L1} = C_{L2} = 25$ pF		12.5		pF
	Duty Cycle	Measured at MCK0 output pin	45	50	55	%
tST	Startup Time	$V_{DDBU} = 2.7V$ $1/(t_{CPMAIN}) = 3$ MHz No capacitor connected to the RTC oscillator pins (X_{IN32}, X_{OUT32})			1.8	ms

AT91M42800A PLL Characteristics

Table 6. PLLA Characteristics (PLL020M1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
K_0	VCO Gain		16	60	70	MHz/V
I_p	CHP Current		50(1)	350(1)	800(1)	µA

Note: 1. These values are obtained for average F_{OUT} between 5 MHz and 20 MHz

Table 7. PLLB Characteristics (PLL080M1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
K_0	VCO Gain		65(1)	105(1)	172(1)	MHz/V
I_p	CHP Current		50	350	800	µA

Note: 1. These values are obtained for average F_{OUT} between 20 MHz and 80 MHz

AT91M55800A PLL Characteristics

Table 8. PLLB Characteristics (PLL080M1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
K_0	VCO Gain		65(1)	105(1)	172(1)	MHz/V
I_p	CHP Current		50	350	800	µA

Note: 1. These values are obtained for average F_{OUT} between 20 MHz and 80 MHz

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Product Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Atmel Heilbronn
Theresienstrasse 2
POB 3535
D-74025 Heilbronn, Germany
TEL (49) 71 31 67 25 94
FAX (49) 71 31 67 24 23

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 0 2 40 18 18 18
FAX (33) 0 2 40 18 19 60

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-357-000
FAX (44) 1355-242-743

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

1740A–09/01/0M