Pulse Width Modulation Generation Using the AT91 Timer/Counter

Introduction

This application note describes how to generate a Pulse Width Modulation (PWM) signal, tunable in frequency and duty cycles, by using the AT91 Timer/Counter (TC).

Timer/Counter Overview

The AT91 series of microcontrollers feature a Timer Counter block which includes three identical 16-bit timer counter channels. Each channel can be independently programmed, through its two operating modes, to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing, pulse width modulation and interrupt generation.

Each Timer Counter channel has 3 external clock inputs, 5 internal clock inputs, and 2 multi purpose input/output signals, which can be configured by the user. Each channel drives an internal interrupt signal, which can be programmed to generate processor interrupts via the Advanced Interrupt Controller (AIC). The three Timer Counter channels are independent and identical in operation. Each Timer Counter channel is organized around a 16-bit counter. The value of the counter is incremented at each positive edge of the selected clock. When the counter has reached the value 0xFFFF and passes to 0x0000, an overflow occurs and the bit COVFS in TCx_SR (Status Register) is set.

The current value of the counter is accessible in real-time by reading TCx_CV. A trigger can reset the counter. In this case, the counter value passes to 0x0000 on the next valid edge of the selected clock.

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Timer/Counter Operating Modes

Each Timer Counter channel can operate independently in two different modes:

- Capture Mode provides measurement on signals.
- Waveform Mode provides wave generation.

The Timer Counter Operating Mode is programmed with the WAVE bit in the TC Channel Mode Register (TCx_CMR). In Capture Mode, TIOA and TIOB are configured as inputs. In Waveform Mode, TIOA is always configured to be an output and TIOB is an output if it is not selected to be the external trigger.

Trigger

A trigger resets the counter and starts the counter clock. Three types of triggers are common to both modes, and a fourth external trigger is available to each mode.

Common Triggers

The following triggers are common to both operating modes:

- Software Trigger: Each channel has a software trigger, available by setting SWTRG in TCx_CCR.
- SYNC: Each channel has a synchronization signal SYNC. When asserted, this signal has the same effect as a software trigger. The SYNC signals of all channels are asserted simultaneously by writing TC_BCR (Block Control) with SYNC set.
- Compare RC Trigger: RC is implemented in each channel and can provide a trigger when the counter value matches the RC value if CPCTRG is set in TCx_CMR.

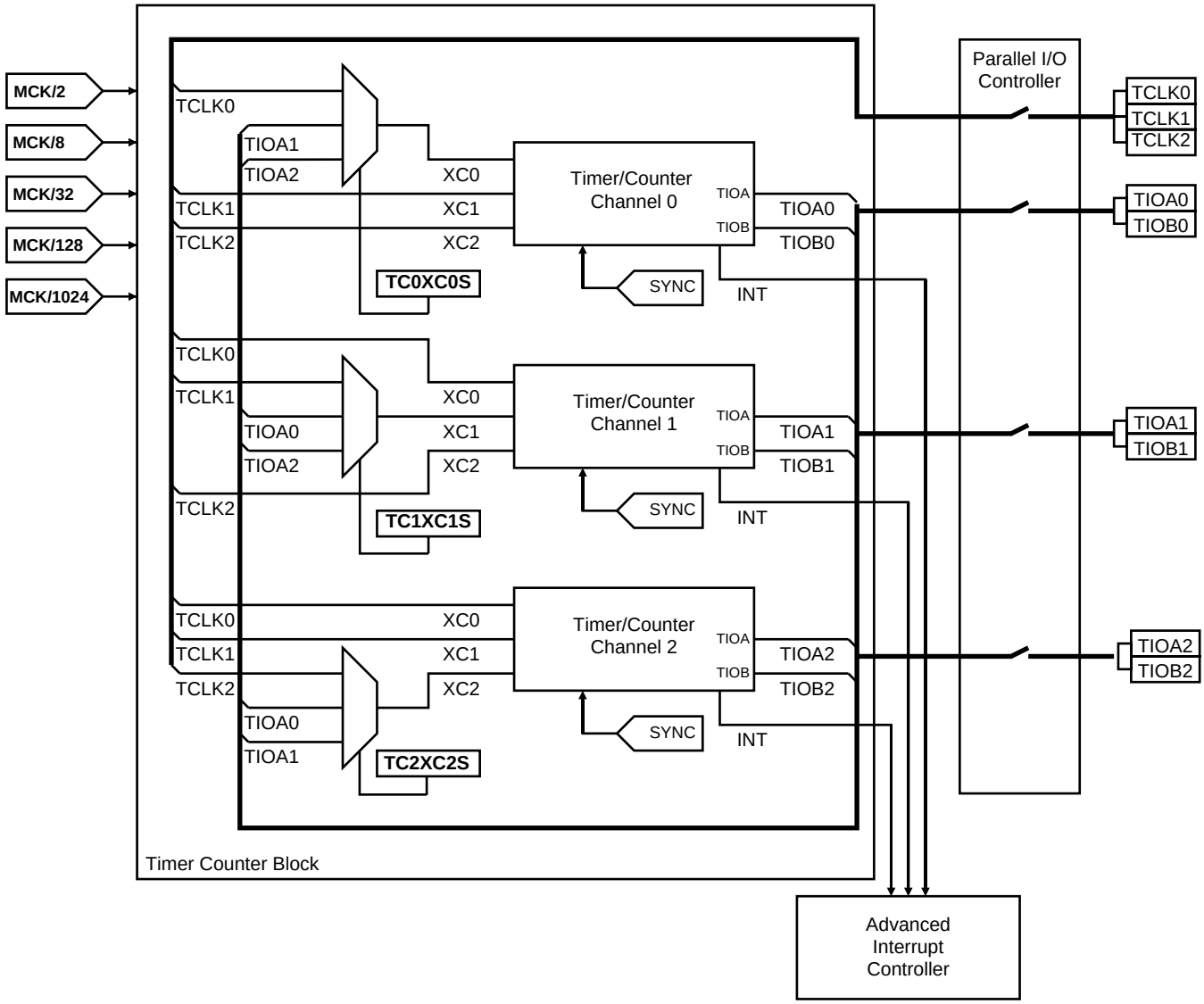
External Trigger

The Timer Counter channel can also be configured to have an external trigger. In Capture Mode, the external trigger signal can be selected between TIOA and TIOB. In Waveform Mode, an external event can be programmed on one of the following signals: TIOB, XC0, XC1 or XC2. This external event can then be programmed to perform a trigger by setting ENETRG in TCx_CMR.

If an external trigger is used, the duration of the pulses must be longer than the system clock (MCK) period in order to be detected.

Timer/Counter Block Diagram

Figure 1. Timer/Counter Block Diagram



Clock Source

Each channel can independently select an internal or external clock source for its counter:

- Internal clock signals: MCK/2, MCK/8, MCK/32, MCK/128, MCK/1024
- External clock signals: XC0, XC1 or XC2

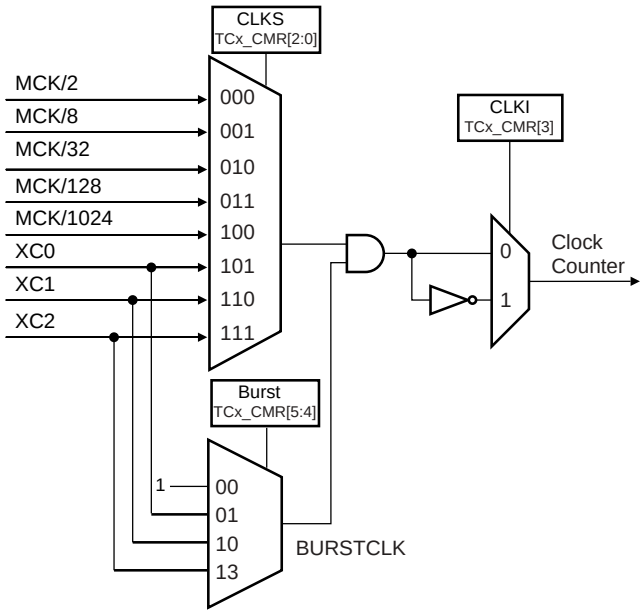
The three-bit TCCLKS field of the mode register TCx_CMR determines whether the counter is clocked by one of the five internal clock sources (MCK/x) or one of the three external clock sources (TCLKx).

The selected clock can be inverted with the CLKI bit in TCx_CMR (Channel Mode Register). This enables counting on the opposite edges of the clock.

The burst function allows the clock to be validated when an external signal is high. The BURST parameter in the Mode Register defines this signal (none, XC0, XC1, XC2).

Note: In all cases, if an external clock is used, the duration of each of its levels must be longer than the system clock (MCK) period. The external clock frequency must be at least 2.5 times lower than the system clock (MCK).

Figure 2. Timer/Counter Clock Source



The maximal counter duration when an internal clock is used is determined by the internal clock MCK and the prescaler number:

maximal counter duration (seconds) = $2^{16} / F_{TC}$ where F_{TC} is in Hz.

counter resolution = $1 / F_{TC}$

Table 1. Maximum Counter Duration for MCK

MCK	5 MHz	10 MHz	20 MHz	33 MHz	66 MHz
MCK/2	26.21ms	13.10ms	6.55ms	3.97ms	1.98ms
MCK/8	104.8ms	52.4ms	26.22ms	14.89ms	7.45ms
MCK/16	419.4ms	209.7ms	104.86ms	63.86ms	31.98ms
MCK/128	1.68s	838.8ms	420.4ms	254.2ms	127.1ms
MCK/1024	13.42s	6.71s	3.36ms	2.03s	1.02s

Pulse Width Modulation Generation

The waveform mode is entered by setting the bit WAVE (bit 15 in the Mode Register) to 1. It forces TIOA as an output pin. TIOB can be used either as an output (dual waveform mode) or as an input (single waveform mode). Waveform Operating Mode allows the TC Channel to generate 1 or 2 PWM signals with the same frequency and independently programmable duty cycles, or to generate different types of one-shot or repetitive pulses.

In Waveform Operating Mode, RA, RB and RC are all used as compare registers. The compare registers can generate a counter reset (RC) or a waveform modification (RA, RB and RC) when the counter reaches the value programmed in them.

RA Compare is used to control the TIOA output. RB Compare is used to control the TIOB (if configured as an output). RC Compare can be programmed to control TIOA and/or TIOB outputs. RC Compare can also generate a trigger if bit CPCTRG = 1. A trigger resets the counter so that RC can control the period of PWM waveforms. Each of these events can be programmed to set, clear or toggle the output as defined in the corresponding parameter in TCx_CMR.

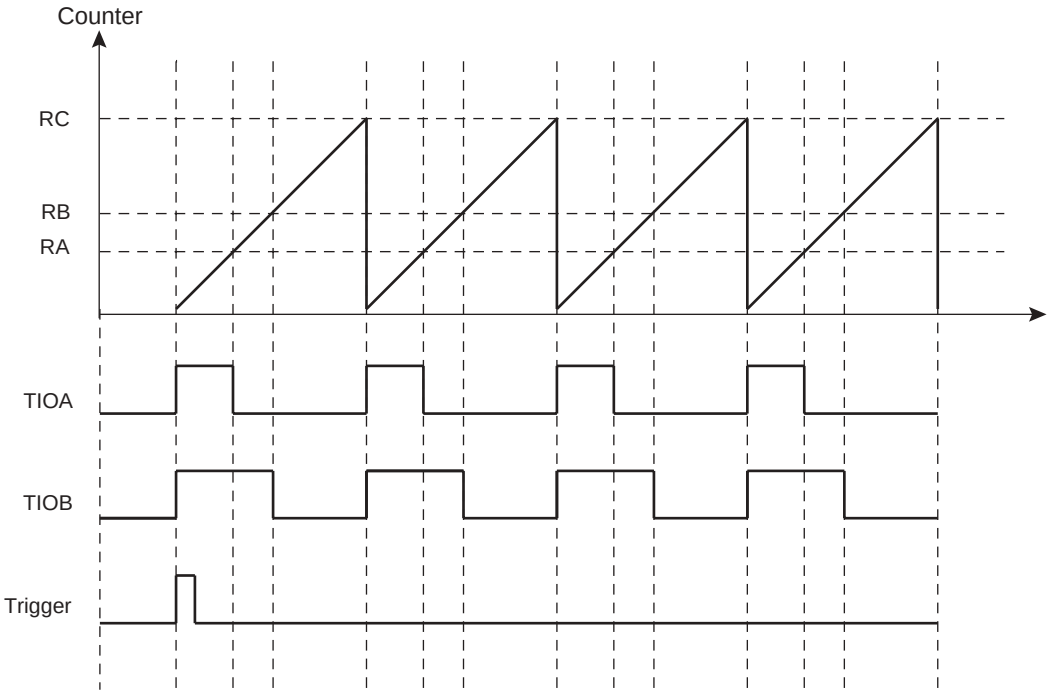
Application Example

Use the AT91 Timer/Counter for the generation of two 1 kHz frequency PWM with 30% duty cycle on TIOA and 50% duty cycle on TIOB. This application example is based on the AT91EB40A Evaluation Board but applicable to all AT91 products.

Timer configuration

The RC compare can generate a trigger if bit CPCTRG in the TC Mode Register is set to 1. A trigger resets the counter so the PWM signal period can be controlled by the RC Compare register. The duty cycle on TIOA and TIOB is controlled by the RA and RB Compare registers respectively. The trigger event sets TIOA and TIOB then TIOA is toggled by RA and RC, TIOB by RB and RC as shown below in Figure 3.

Figure 3. Dual Pulse Width Modulation Generation



The Master Clock MCK on the AT91EB40A Evaluation Board is 66 MHz. The value needed in the compare register C to assure a timer period of 1ms (1kHz PWM frequency) must be established. The PWM frequency is controlled by the compare register RC:

The minimal prescaler value required to select the timer clock F_{TC} must first be determined. The maximal counter value is 0xFFFF (65535):

$$DIV_{min} = t \times \frac{MCK}{65535} = 0.001 \times \frac{66000000}{65535} = 1.007$$

The value ≥ 1.007 is DIV = 2. Therefore, the timer clock F_{TC} must be at least MCK/2 (33000000Hz) to have a RC compare period of 1ms.

In an application, the required compare register values must be calculated using the following equation:

$$\text{Compare Value} = (t \times F_{TC}) - 1$$

Where

t = desired timer compare period (second)

F_{TC} = timer clock frequency(Hertz)

Compare register RC:

$$RC = \frac{F_{TC}}{Fpwm} - 1 = \frac{MCK/2}{1000} - 1 = \frac{33000000}{1000} - 1 = 32999 = 0x80E7$$

30% duty cycle on TIOA, compare register RA:

$$(RA + 1) = 30\% \cdot (RC + 1)$$

$$\Rightarrow RA = \frac{30 \times (32999 + 1)}{100} - 1 = 9899 = 0x26AB$$

50% duty cycle on TIOB, compare register RB:

$$(RA + 1) = 50\% \cdot (RC + 1)$$

$$\Rightarrow RA = \frac{50 \times (32999 + 1)}{100} - 1 = 16499 = 0x4073$$

Software Code

The following software code example generates a dual 1kHz PWM with 30% duty cycle on TIOA and 50% duty cycle on TIOB by using the Timer/Counter 1 in waveform mode on the AT91EB40A Evaluation Board and is applicable to the entire AT91 series.

```
//*-----------------------------------------------------------------------------------------------------------
//*The software is delivered "AS IS" without warranty or condition of any kind, either express, implied or
statutory. This includes
//*without limitation any warranty or condition with respect to merchantability or fitness for any particular
purpose, or against the
//*infringements of intellectual property rights of others.
//*-----------------------------------------------------------------------------------------------------------
//* File Name      : wave_pwm.c
//* Object         : AT91EB40A - Timer Counter - Dual PWM generation
//* Author         : AT91 Application Group
//*-----------------------------------------------------------------------------------------------------------
//* Configure the channel 1 of the Timer Counter(TC) of the AT91EB40A to aim dual waveform generation :
//* - PWM frequency = 1kHz
//* - clock selected = MCK / 2
//* - Register A compare toggle TIOA1 when reached
//* - Register B compare toggle TIOB1 when reached
//* - Register C compare toggle TIOA1 and TIOB1 when reached
//*-----------------------------------------------------------------------------------------------------------

#define    TC1_CCR    ((volatile unsigned int *) 0xFFFE0040)
#define    TC1_CMR    ((volatile unsigned int *) 0xFFFE0044)
#define    TC1_RA     ((volatile unsigned int *) 0xFFFE0054)
#define    TC1_RB     ((volatile unsigned int *) 0xFFFE0058)
#define    TC1_RC     ((volatile unsigned int *) 0xFFFE005C)

#define    PIO_PDR    ((volatile unsigned int *) 0xFFFF0004)

//* TC_CMR: Timer Counter Channel Mode Register Bits Definition
#define    TC_CLKS_MCK20x0
#define    TC_EEVT_XC0                0x400
#define    TC_CPCTRG                  0x4000
#define    TC_WAVE                    0x8000
#define    TC_ACPA_TOGGLE_OUTPUT      0x30000
#define    TC_ACPC_TOGGLE_OUTPUT      0xC0000
#define    TC_ASWTRG_SET_OUTPUT       0x400000
#define    TC_BCPB_TOGGLE_OUTPUT      0x3000000
#define    TC_BCPC_TOGGLE_OUTPUT      0xC000000
#define    TC_BSWTRG_SET_OUTPUT       0x40000000

//* TC_CCR: Timer Counter Control Register Bits Definition
#define    TC_CLKEN            0x1
#define    TC_CLKDIS           0x2
#define    TC_SWTRG            0x4

//* PIO Controller
```

```
#define    PIOTIOA1            4          /* Timer 1 Signal A */
#define    PIOTIOB1            5          /* Timer 1 Signal B */

//*-----------------------------------------------------------------------------------------------------------
//* Function Name    : main
//* Object: Timer Counter 1 configuration to generate Dual PWM generation
//*-----------------------------------------------------------------------------------------------------------
int main ( void )
//* Begin
    {
*TC1_CCR = TC_CLKDIS ;                          /* Disable the Clock Counter */

    *PIO_PDR = (1<<PIOTIOA1) | (1<<PIOTIOB1) ;      /* Define TIOA1 and TIOB1 as peripheral */

    //* Timer/Counter 1 mode configuration
    *TC1_CMR =
              TC_BSWTRG_SET_OUTPUT          |       /* BSWTRG      : software trigger set TIOB  */
              TC_BCPC_TOGGLE_OUTPUT         |       /* BCPC       : Register C compare toggle TIOB  */
              TC_BCPB_TOGGLE_OUTPUT         |       /* BCPB       : Register B compare toggle TIOB  */
             TC_ASWTRG_SET_OUTPUT           |       /*  ASWTRG      : software trigger set TIOA */
             TC_ACPC_TOGGLE_OUTPUT          |       /*  ACPC         : Register C compare toggle TIOA */
             TC_ACPA_TOGGLE_OUTPUT          |       /*  ACPA         : Register A compare toggle TIOA */
              TC_WAVE                       |      /* WAVE         : Waveform mode */
               TC_CPCTRG                    |      /* CPCTRG        : Register C compare trigger enable */
              TC_EEVT_XC0                   |      /*  EEVT         : XC0 as external event (TIOB=output) */
              TC_CLKS_MCK2 ;                        /* TCCLKS       : MCK / 2 */

//* Compare registers initialization
    *TC1_RC = 0x80E8 ;                  /* 1kHz PWM generation */
    *TC1_RB = 0x4073 ;                  /* 30% duty cycle on TIOB1 */
    *TC1_RA = 0x26AB ;                  /* 50% duty cycle on TIOA1 */

    *TC1_CCR = TC_CLKEN ;                /* Enable the Clock counter */
    *TC1_CCR = TC_SWTRG ;               /* Trig the timer */

    for (;;)
    {
    }//* End for

    return(0) ;
}//*End
```

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Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

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Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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