Features

- **High-performance, Low-power AVR® 8-bit Microcontroller**
- **Advanced RISC Architecture**
  - **90 Powerful Instructions – Most Single-clock Cycle Execution**
  - **32 x 8 General-purpose Working Registers**
  - **Fully Static Operation**
- **Nonvolatile Program and Data Memories**
  - **1K bytes In-System Programmable Flash Program Memory**
    Endurance: 1,000 Write/Erase Cycles
  - **64 bytes EEPROM**
    Endurance: 100,000 Write/Erase Cycles
  - **Programming Lock for Flash Program Data Security**
- **Peripheral Features**
  - **Interrupt and Wakeup on Pin Change**
  - **Two 8-bit Timer/Counters with Separate Prescalers**
  - **One150 kHz, 8-bit High-speed PWM Output**
  - **4 channel 10-bit ADC**
    One Differential Voltage Input with Optional Gain of 20x
  - **On-chip Analog Comparator**
  - **Programmable Watchdog Timer with On-chip Oscillator**
- **Special Microcontroller Features**
  - **In-System Programmable via SPI Port**
  - **Enhanced Power-on Reset Circuit**
  - **Programmable Brown-out Detection Circuit**
  - **Internal, Calibrated 1.6 MHz Tuneable Oscillator**
  - **Internal 25.6 MHz Clock Generator for Timer/Counter**
  - **External and Internal Interrupt Sources**
  - **Low-power Idle and Power-down Modes**
- **I/O and Packages**
  - **8-pin PDIP/SOIC: 6 Programmable I/O Lines**
- **Operating Voltages**
  - **2.7V - 5.5V (ATtiny15L)**
- **Internal 1.6 MHz System Clock**
- **Commercial and Industrial Temperature Ranges**

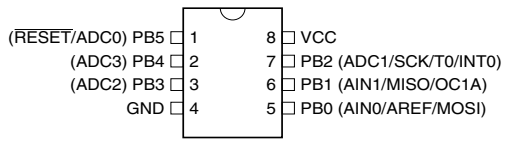
Description

The ATtiny15L is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single-clock cycle, the ATtiny15L achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

(continued)

Pin Configuration

PDIP/SOIC



8-bit AVR® Microcontroller with 1K Bytes Flash

ATtiny15L

Advance Information

Rev. 1187BS–03/00

Note: This is a summary document. For the complete 70-page document, please visit our web site at *www.atmel.com* or e-mail at *literature@atmel.com* and request literature #1187B.

The AVR core combines a rich instruction set with 32 general-purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

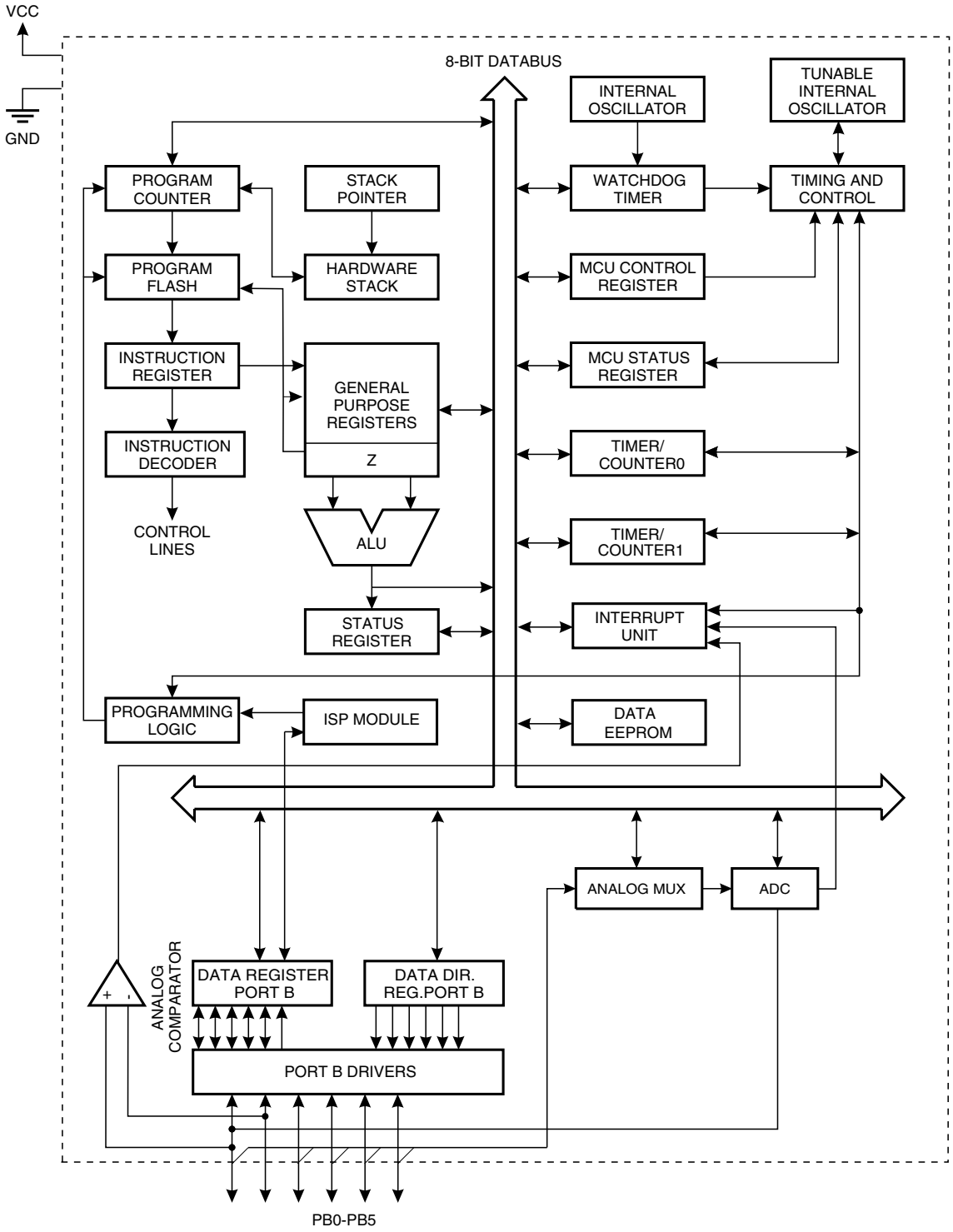
The ATtiny15L provides 1K bytes of Flash, 64 bytes EEPROM, 6 general-purpose I/O lines, 32 general-purpose working registers, two 8-bit timer/counters, one with high speed PWM output, internal oscillators, internal and external interrupts, programmable Watchdog Timer, 4-channel 10-bit Analog to Digital Converter with one differential voltage input with optional 20x gain, and three software-selectable power-saving modes. The Idle mode stops the CPU while allowing the ADC, analog comparator, timer/counters and interrupt system to continue functioning. The ADC Noise Reduction mode facilitates high-accuracy ADC measurements by stopping the CPU while allowing the ADC to continue functioning. The Power-down mode saves the register contents but freezes the oscillators, disabling all other chip functions until the next interrupt or hardware reset. The wake-up or interrupt on pin change features enable the ATtiny15L to be highly responsive to external events, still featuring the lowest power consumption while in the power-saving modes.

The device is manufactured using Atmel's high density nonvolatile memory technology. By combining an enhanced RISC 8-bit CPU with Flash on a monolithic chip, the Atmel ATtiny15L is a powerful microcontroller that provides a highly-flexible and cost-efficient solution to many embedded control applications. The peripheral features make the ATtiny15L particularly suited for battery chargers, lighting ballasts, and all kinds of intelligent sensor applications.

The ATtiny15L AVR is supported with a full suite of program and system development tools including macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Block Diagram

Figure 1. The ATtiny15L Block Diagram



Pin Descriptions

VCC

Supply voltage pin.

GND

Ground pin.

Port B (PB5..PB0)

Port B is a 6-bit I/O port. PB4..0 are I/O pins that can provide internal pull-ups (selected for each bit). PB5 is input or open-drain output. The use of pin PB5 is defined by a fuse and the special function associated with this pin is external Reset. The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also accommodates analog I/O pins. The Port B pins with alternate functions are shown in Table 1:

Table 1. Port B Alternate Functions

Port Pin	Alternate Function
PB0	MOSI (Data Input Line for Memory Downloading) AREF (ADC Voltage Reference) AIN0 (Analog Comparator Positive Input)
PB1	MISO (Data Output Line for Memory Downloading) OC1A (Timer/Counter PWM Output) AIN1 (Analog Comparator Negative Input)
PB2	SCK (Serial Clock Input for Serial Programming) INT0 (External Interrupt0 Input) ADC1 (ADC Input Channel 1) T0 (Timer/Counter0 External Counter Input)
PB3	ADC2 (ADC Input Channel 2)
PB4	ADC3 (ADC Input Channel 3)
PB5	$\overline{\text{RESET}}$ (External Reset Pin) ADC0 (ADC Input Channel 0)

Analog Pins

Up to four analog inputs can be selected as inputs to Analog to digital converter (ADC).

Internal Oscillators

The internal oscillator provides a clock rate of nominally 1.6 MHz for the system clock CK. Due to large initial variation (0.8 MHz -1.6 MHz) of the internal oscillator, a tuning capability is built in. Through an eight bit control register OSCCAL, the system clock rate can be tuned with less than 1% steps of the nominal clock.

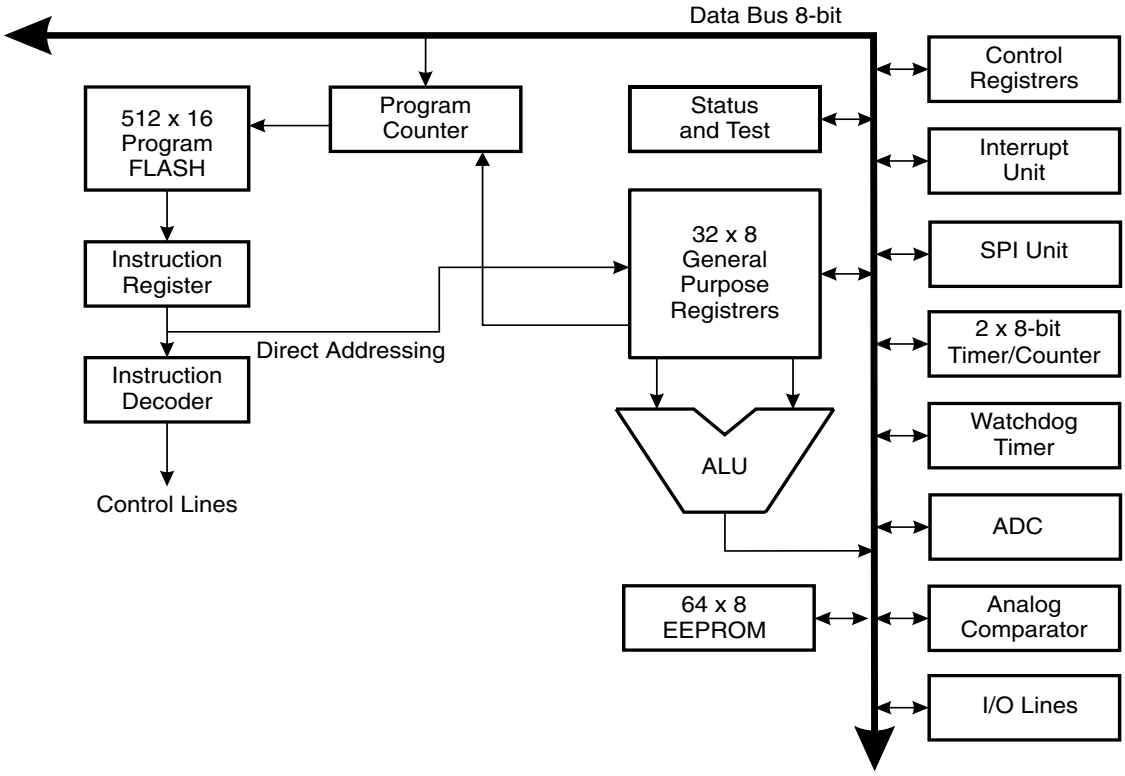
There is an internal PLL that provides a 16x clock rate locked to the system clock (CK) for the use of the Peripheral Timer/Counter1. The nominal frequency of this peripheral clock, PCK, is 25.6 MHz.

ATtiny15L Architectural Overview

The fast-access register file concept contains 32 x 8-bit general-purpose working registers with a single-clock-cycle access time. This means that during one single-clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file – in one clock cycle.

Two of the 32 registers can be used as a 16-bit pointer for indirect memory access. This pointer is called the Z-pointer, and can address the register file, IO file, and the Flash program memory.

Figure 2. The ATtiny15L AVR RISC Architecture



The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single-register operations are also executed in the ALU. Figure 2 shows the ATtiny15L AVR RISC microcontroller architecture. The AVR uses a Harvard architecture concept with separate memories and buses for program and data memories. The program memory is accessed with a two-stage pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system programmable Flash memory.

With the relative jump and relative call instructions, the whole address space is directly accessed. All AVR instructions have a single 16-bit word format, meaning that every program memory address contains a single 16-bit instruction.

During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is a 3 level deep hardware stack dedicated for subroutines and interrupts.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, and other I/O functions. The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All the different interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

ATtiny15L Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F	SREG	I	T	H	S	V	N	Z	C	11
$3E	Reserved									
$3C	Reserved									
$3B	GIMSK	-	INT0	PCIE	-	-	-	-	-	19
$3A	GIFR	-	INTF0	PCIF	-	-	-	-	-	19
$39	TIMSK	-	OCIE1A	-	-	-	TOIE1	TOIE0	-	20
$38	TIFR	-	OCF1A	-	-	-	TOV1	TOV0	-	20
$37	Reserved									
$36	Reserved									
$35	MCUCR	-	PUD	SE	SM1	SM0	-	ISC01	ISC00	21
$34	MCUSR	-	-	-	-	WDRF	BORF	EXTRF	PORF	17
$33	TCCR0	-	-	-	-	-	CS02	CS01	CS00	26
$32	TCNT0	Timer/Counter0 (8-Bit)								27
$31	OSCCAL	Oscillator Calibration Register								23
$30	TCCR1	CTC1	PWM1	COM1A1	COM1A0	CS13	CS12	CS11	CS10	28
$2F	TCNT1	Timer/Counter1 (8-Bit)								29
$2E	OCR1A	Timer/Counter1 Output Compare Register A (8-Bit)								29
$2D	OCR1B	Timer/Counter1 Output Compare Register B (8-Bit)								31
$2C	SFIOR	-	-	-	-	-	FOC1A	PSR1	PSR0	25
$2B	Reserved									
$2A	Reserved									
$29	Reserved									
$28	Reserved									
$27	Reserved									
$26	Reserved									
$25	Reserved									
$24	Reserved									
$23	Reserved									
$22	Reserved									
$21	WDTCR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	32
$20	Reserved									
$1F	Reserved									
$1E	EEAR	-	-	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	33
$1D	EEDR	EEPROM Data Register (8-Bit)								34
$1C	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	34
$1B	Reserved									
$1A	Reserved									
$19	Reserved									
$18	PORTB	-	-	-	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	46
$17	DDRB	-	-	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	46
$16	PINB	-	-	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	46
$15	Reserved									
$14	Reserved									
$13	Reserved									
$12	Reserved									
$11	Reserved									
$10	Reserved									
$0F	Reserved									
$0E	Reserved									
$0D	Reserved									
$0C	Reserved									
$0B	Reserved									
$0A	Reserved									
$09	Reserved									
$08	ACSR	ACD	ACBG	ACO	ACI	ACIE	-	ACIS1	ACIS0	36
$07	ADMUX	REFS1	REFS0	ADLAR	-	-	MUX2	MUX1	MUX0	42
$06	ADCSR	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	43
$05	ADCH	ADC Data Register High Byte								43
$04	ADCL	ADC Data Register Low Byte								43
…	Reserved									
$00	Reserved									

ATtiny15L Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd⊕Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← $FF - Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← $00 - Rd	Z,C,N,V,H	1
SBR	Rd, K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd, K	Clear Bit(s) in Register	Rd ← Rd • (FFh - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd⊕Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← $FF	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd, Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2
CP	Rd, Rr	Compare	Rd - Rr	Z, N,V,C,H	1
CPC	Rd, Rr	Compare with Carry	Rd - Rr - C	Z, N,V,C,H	1
CPI	Rd, K	Compare Register with Immediate	Rd - K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1 / 2
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1 / 2
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1 / 2
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1 / 2
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half-carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half-carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2

ATtiny15L Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
DATA TRANSFER INSTRUCTIONS					
LD	Rd, Z	Load Register Indirect	Rd ← (Z)	None	2
ST	Z, Rr	Store Register Indirect	(Z) ← Rr	None	2
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
LPM		Load Program Memory	R0 ← (Z)	None	3
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P, b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P, b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half-carry Flag in SREG	H ← 1	H	1
CLH		Clear Half-carry Flag in SREG	H ← 0	H	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	3
WDR		Watch Dog Reset	(see specific descr. for WDR/timer)	None	1

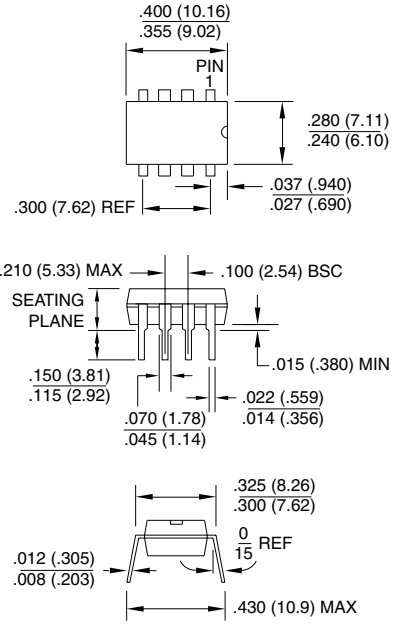
Ordering Information

Power Supply	Speed (MHz)	Ordering Code	Package	Operation Range
2.7 - 5.5V	1.6	ATtiny15L-1PC ATtiny15L-1SC	8P3 8S2	Commercial (0°C to 70°C)
		ATtiny15L-1PI ATtiny15L-1SI	8P3 8S2	Industrial (-40°C to 85°C)

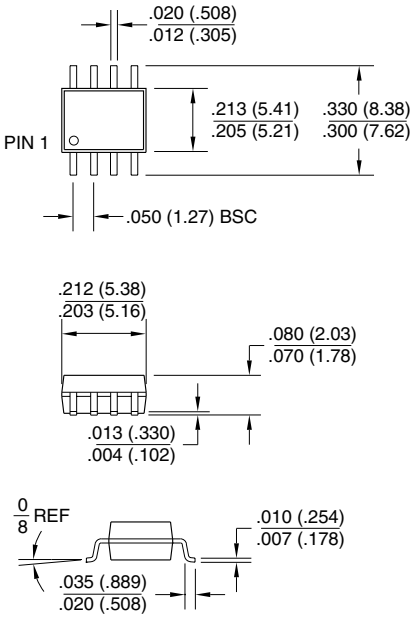
Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)

Packaging Information

8P3, 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



8S2, 8-lead, 0.210" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Dimensions in Inches and (Millimeters)



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