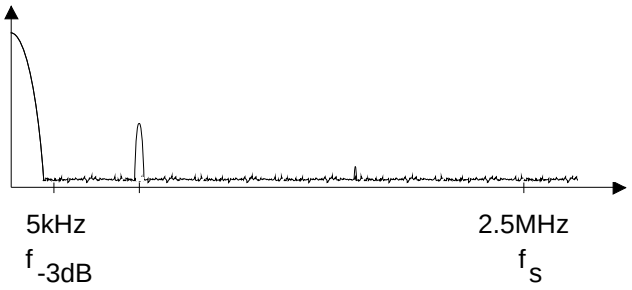
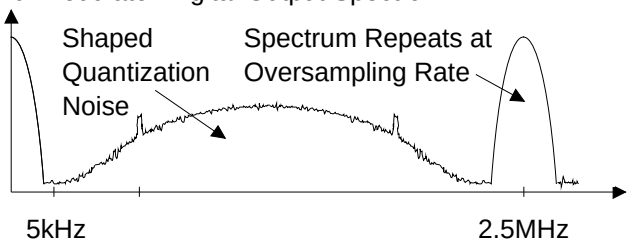
Application Note

Delta Sigma A/D Conversion Technique Overview

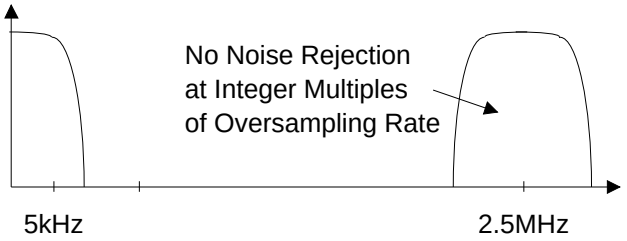
a. Analog Input Spectrum



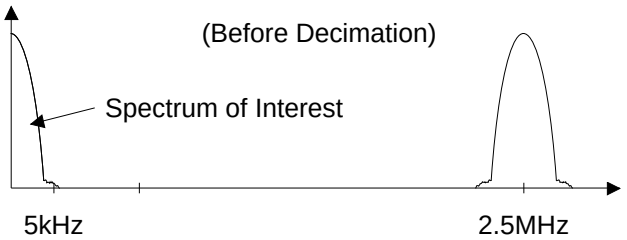
b. Modulator Digital Output Spectrum



c. Digital Filter Response



d. Digital Filter Output Spectrum



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DELTA-SIGMA MODULATION

Delta-sigma modulation utilizes oversampling and digital filtering to achieve high performance A/D conversion and filtering at low cost. The advent of commercial delta-sigma converters is due in most part to advances in mixed analog-digital VLSI technology. Precision analog circuitry can now be integrated on the same chip with powerful digital filters.

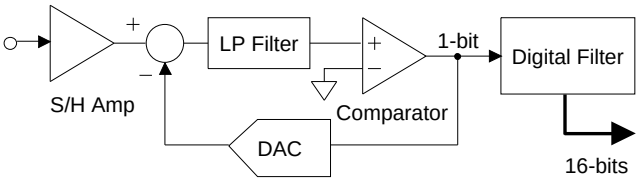


Figure 1. Delta-Sigma ADC

In a delta-sigma ADC, the same digital filter used in the A/D conversion process can perform system-level filtering with performance unachievable in analog form. Delta-sigma converters have been targeted at applications demanding high-performance filtering (high-end modems, digital audio, geophysical exploration, etc).

This application note uses the CS5317 voice band A/D converter for examples. See the end of this application note for implementation details for the CS5317, CS5501, CS5335 A/D converters.

Fundamentals

A delta-sigma ADC consists of two basic blocks: an analog modulator and a digital filter (see Figure 1). The fundamental principle behind the modulator is that of a single-bit A/D converter embedded in an analog negative feedback loop with high open loop gain. The modulator loop oversamples and processes the analog input at a rate much higher than the bandwidth of interest. The modulator's output provides small packages of information (that is, 1-bit) at a very high rate and in a format that the digital filter can process to extract higher resolution (such as 16-bits) at a lower rate.

The delta-sigma converter's basic operation can be analyzed in either the time domain, or (more conventionally) in the frequency domain.

Time-Domain Analysis

The basic operation of a delta-sigma modulator can be understood more intuitively by demonstration. A simple, first-order modulator (that is, a conventional voltage-to-frequency converter) is shown in Figure 2. (Note: a modulator's order indicates the number of orders of analog filtering - or integration - in the loop). Full-scale inputs are $\pm$ 1V and three nodes are labeled V_1, V_2, and V_3. The output of the comparator, node V_3, is the output of the loop and is also converted by the 1-bit DAC into plus or minus full-scale (+1V or -1V).

At the differential amplifier, the +1V or -1V is subtracted from the analog input voltage. The result, the voltage at node V_1, is input to the integrator. The integrator acts as an analog accumulator; ie. the input voltage at node V_1 is added to the voltage on node V_2 which becomes the new voltage on node V_2. Node V_2 is then compared to ground. If it is greater than ground, node V_3 becomes +1V; if it is less than ground, V_3 becomes -1V. Each operation occurs once during each clock cycle.

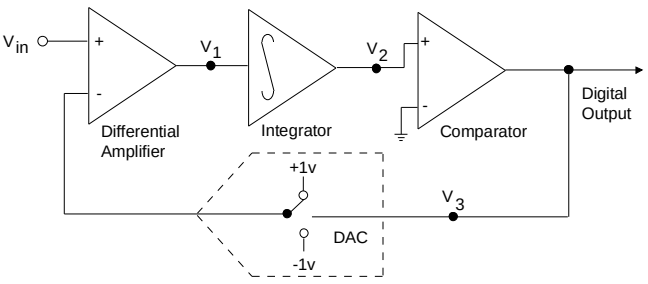


Figure 2. 1st-order Delta-Sigma Modulator

In the example shown in Table 1, all nodes are initially set to zero, and the analog input voltage is assumed to be 0.6V. Since all nodes are identical in clock cycles two and seven, the period defined by cycles two to six will repeat if the analog input remains unchanged. The average value of modulator outputs (at node V_3) during that period, 0.6, yields a numerical representation of the analog input.

Clock Period	V_1	V_2	V_3	Period Avg
0	0	0	0	
1	0.6	0.6	1	
2	-0.4	0.2	1	
3	-0.4	-0.2	-1	
4	1.6	1.4	1	0.6
5	-0.4	1.0	1	
6	-0.4	0.6	1	
7	-0.4	0.2	1	
8	-0.4	-0.2	-1	

Table 1. Modulator Walk-Through

With conventional voltage-to-frequency converters a digital counter is used to extract the information in the VFC's 1-bit output. Pulses are counted over a specified period, effectively creating a digital averaging (or integrating) filter. The final count represents the average analog input value during the integrating period.

Advanced delta-sigma converters use higher-order modulators and more powerful digital filters. The CS5317, one of the first commercially-available delta-sigma converters uses a second-order modulator. The pattern of transitions in its 1-bit output provides more useful information regarding higher resolution at higher frequencies.

However, a more sophisticated digital filter than a counter is needed to interpret that information. A digital FIR filter is basically a rolling, weighted average of consecutive samples (see the section on digital filtering). An averaging filter weights all samples equally. By applying a more sophisticated weighting function to the 1-bit signal, a digital FIR filter can assemble an N-bit output (with 2^N possible values) *without having to wait for 2^N samples.*

The Charge-Balance Name

Delta-sigma ADC's are also known by other names - sigma delta and charge-balance are two examples. The *Charge-Balance* name derives from the fact that the modulator tries to *balance* the analog input with the DAC's output in the negative feedback loop. The charge injected onto the integrator's capacitor from sampling the analog input (see Figure 2) is therefore balanced by the charge injected by the DAC's output. Modulators have been implemented in both switched-capacitor and continuous-time form.

Frequency-Domain Analysis

Since filtering plays a key role in a delta-sigma ADC, it is easier to understand the converter's operation by analyzing it in the frequency domain.

Overview

An A/D converter's resolution determines its dynamic range (or signal-to-noise ratio). Conversely, one can improve a converter's signal-to-noise ratio and thereby increase its effective resolution. The fundamental concept behind delta-sigma converters is to perform a simple, low-resolution A/D conversion and reduce the resulting "quantization noise" (without affecting the frequency band of interest) using analog and digital filtering.

Quantization Noise

The comparator in the delta-sigma modulator loop plays the role of a 1-bit A/D converter. Any A/D converter can represent a continuous analog

input by one of only a *finite* number of codes, giving rise to an uncertainty, or quantization error, of up to ± 1/2 LSB. For a consecutive sequence of samples in a waveform, these quantization effects can be modeled as a random noise source under conditions commonly encountered in signal processing applications. (These conditions hold true for delta-sigma modulators). The rms value of the noise source relative to a full-scale input can be shown to equal - (6.02 N + 1.76) dB, for an N-bit resolution converter. Since this error "signal" is totally random (or uncorrelated with the input) it can be assumed to be white, with its energy spread uniformly over the band from dc to one-half the sampling rate.

As a 1-bit ADC, the comparator in a delta-sigma modulator offers (an almost comical) 7.78 dB signal-to-noise ratio. However, the input signal is grossly oversampled (2.5 MHz in the CS5317), thus spreading the quantization noise over a wide bandwidth (1.25 MHz). The noise density in the bandwidth of interest (5 kHz) is therefore reduced.

Noise Shaping

Analog filtering is used in the modulator loop to further reduce noise density in the frequency band of interest by shaping the quantization noise spectrum. The spectrum of the input signal, meanwhile, remains unaltered. Figure 3 shows a modulator loop with analog and digital circuit differences ignored. The comparator is simply shown as a (quantization) noise source, and the analog filtering, which is simply an integrator, assumes the filter response H(f). If the analog input equals zero, then

$$D_{out} = Q(n) - H(f)\, D_{out}$$

$$D_{out} = \frac{Q(n)}{1 + H(f)}$$

The quantization noise at the output is reduced by the open-loop gain of the integrator. At low

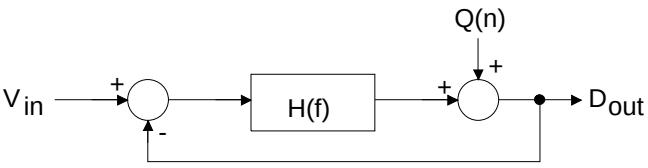


Figure 3. Analog Modulator Model

frequency, the integrator is designed for high open-loop gain, so that quantization noise is reduced. As shown in Figure 4b, the integrator effectively pushes the quantization noise out of the bandwidth of interest and into higher frequencies. Digital lowpass filtering then removes the quantization noise at the higher frequencies without affecting the low-frequency spectrum of interest.

The spectral characteristics of the analog loop filtering dictates the delta-sigma converter's resolution/bandwidth ratio. Higher-order integrators improve noise shaping and allow for higher resolutions at wider bandwidths. The CS5317 uses a second-order modulator for superior noise shaping.

Digital Filtering

The spectral characteristics of the back-end digital filtering also affects the delta-sigma converter's resolution/bandwidth ratio. Faster roll-off and greater stopband rejection reduces residual quantization noise. The digital filter section of this application note offers a detailed explanation of the theory behind digital filtering.

Anti-Alias Requirements

As shown in Figure 4, the input and digital filtering spectrum of any ADC repeats around integer multiples of its sampling rate. A delta-sigma ADC thus does not provide noise rejection in the region around integer multiples of the sampling rate (± 5 kHz around 2.5 MHz, 5 MHz, 7.5 MHz...). If noise exists in the system in these narrow bands, analog filtering is needed to re-

move it at the converter's input otherwise it will alias and pass unfiltered to the converter's output.

Since delta-sigma ADC's are grossly oversampled, anti-alias filtering requirements are often trivial. For instance, the CS5317 provides a factor of 500 of oversampling (2.5 MHz/5 kHz). A single-pole, passive RC filter at the CS5317's input is therefore sufficient in most applications.

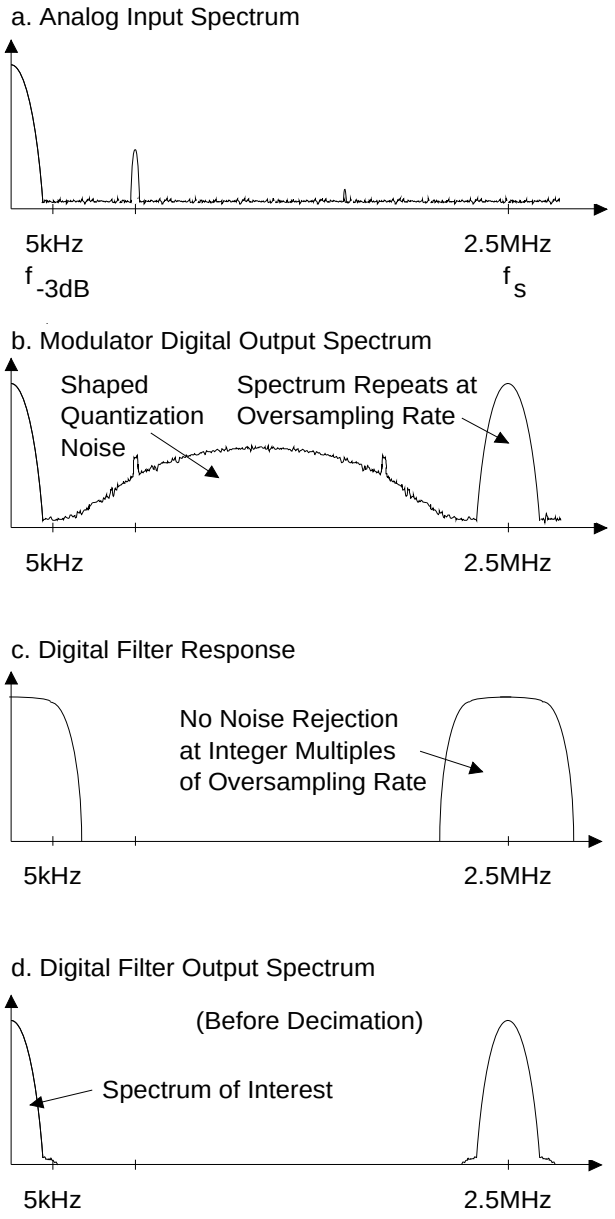


Figure 4. Delta-Sigma Spectral Analysis (Using frequencies taken from the CS5317 A/D Converter)

Decimation

Even though the delta-sigma ADC oversamples and processes analog samples at a frequency well above the bandwidth of interest, it will generally offer its high-resolution output at a much-lower system sampling rate. Any reduction in sampling rate is termed *decimation*. The output can be further decimated at the system level by selectively reading a fraction of the available samples (for instance, every tenth sample). Independent of the decimation ratio, the converter's noise performance (and effective resolution) remains unchanged.

Conversion Accuracy/Performance

Like integrating ADC's and V/F converters, a delta-sigma ADC does not contain any source of nonmonotonicity and thereby offers "theoretically perfect" DNL with no missing codes. The ADC in the modulator is simply a comparator, and the DAC is the positive and negative voltage references. No precision ratio matching is needed as in other medium- or high-speed A/D conversion techniques such as successive-approximation. Useful resolution is limited only by residual quantization noise which, in turn, is determined by coarse analog and high-performance digital filtering.

Linearity error is limited only by imperfections in the input sample/hold. The CS5317 achieves typical nonlinearity of just ± 0.003 % through the use of high-quality on-chip silicon dioxide capacitors with low capacitor voltage coefficient.

DIGITAL FILTERING

A conventional analog filter implements a mathematical equation using reactive components (capacitors and inductors). A digital filter can implement the same filter equation using two fundamental arithmetic operations: multiplication and addition (or accumulation). A digital filter considers a consecutive sequence of digitized samples a "waveform." It analyzes the relationship between samples, processes the data, and outputs an adjusted waveform.

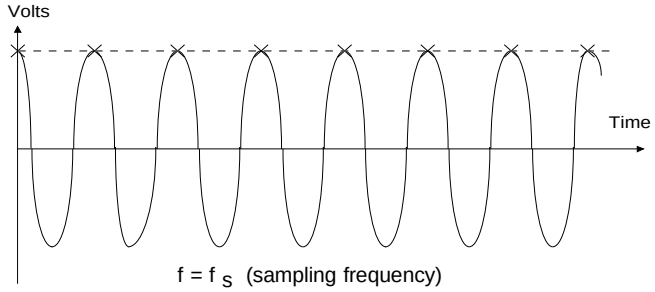
Digital filters offer ideal stability, repeatability, and potentially perfect performance (linear phase, etc.). Digital filters also remain impervious to environmental conditions, thus providing superior reliability over time and temperature. The major difference compared to analog filters, though, is that digital filters operate on a signal in sampled form.

Sampled-Data Theory

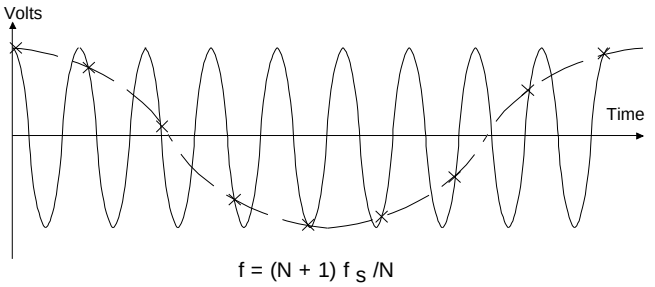
A fundamental phenomenon in sampled-data systems is an effect called "aliasing." Basically, *once an analog signal is sampled, its frequency components are no longer uniquely distinguishable.* Figure 5a shows a special case called "dc aliasing." If a signal is sampled precisely at its fundamental frequency, it will always be sampled at the same point on the waveform. It thus becomes indistinguishable from a dc input. Likewise, a signal at twice the sampling frequency (or any integer multiple of f_S) would appear as dc as well. Figure 5b illustrates a more general case of aliasing. Again, two signals at different frequencies become indistinguishable once sampled.

The effect of aliasing in the frequency domain is illustrated in Figure 6. The baseband spectrum (dc to one-half the sampling rate) also "appears" around integer multiples of the sampling rate, *and vice-versa*. In signal processing applications, anti-alias filtering is used to bandlimit the analog signal before it is sampled. This removes out-of-band components which could be mistaken for important information in the band of interest.

Aliasing is critical in digital filtering. A digital filter is incapable of distinguishing signals in its passband from signals aliasing from around its sampling frequency. Its passband spectrum therefore repeats

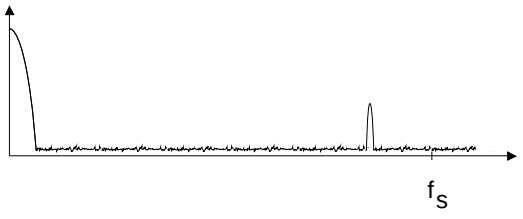


a. dc Aliasing

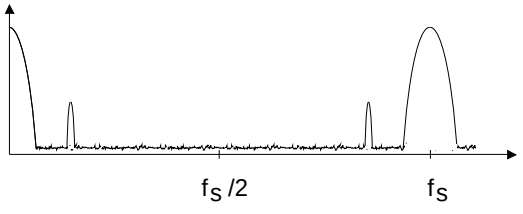


b. General Aliasing

Figure 5. Aliasing in Sampled-Data Systems



a. Continuous-Time Input Spectrum



b. Sampled-Data Spectrum

Figure 6. Sampled-Data Spectrum

around integer multiples of the sampling frequency. Take for instance the case of dc aliasing shown in Figure 5a. A digital low-pass filter would treat the signal at f_S as a dc input and pass it with no attenuation. Similarly, if the filter would attenuate the lower-frequency signal in Figure 5b by 10 dB, the higher-frequency signal would receive the same 10 dB of attenuation. The higher-frequency signals in both cases could be selectively filtered only by analog anti-alias filtering *before the signal is sampled*.

Sampling rates are usually set high enough that analog anti-alias requirements become trivial (or perhaps eliminated). Higher oversampling ratios offer greater bandwidth to roll off between the passband and sampling frequency. Noise in the digital domain can be analyzed just as it is in the analog domain. Limiting a system's bandwidth will reduce noise and improve dynamic range.

Digital Filtering

The most popular digital filtering technique is averaging. A sequence of digital samples are simply collected and averaged to produce an output. This reduces noise by limiting the effective noise bandwidth. Averaging yields a (sin x)/x (or sinc) filter response as shown in Figure 7. The zeroes of infinite rejection (at f_S/N, $2f_S/N$, $3f_S/N$, etc.) can be strategically placed by selecting f_S and the number of samples averaged, N, to average over an integral number of periods of critical frequencies (50 Hz, 60 Hz, etc.). Of course, this same principle lies at the heart of integrating ADC's, but the averaging is done in analog form. In both cases greater dynamic range (or resolution) can be achieved by increasing integration time. The trade-off is bandwidth.

FIR Filters

Averaging is an elementary example of FIR, or *Finite Impulse Response*, digital filtering. Finite Impulse Response indicates that the filter considers only a *finite* number of inputs to calculate each output. The number of samples determines the *impulse response duration*. For example, a filter which averages ten samples has an impulse response duration of ten. Longer durations indicate more information is considered for each calculation, resulting in a more powerful filter response.

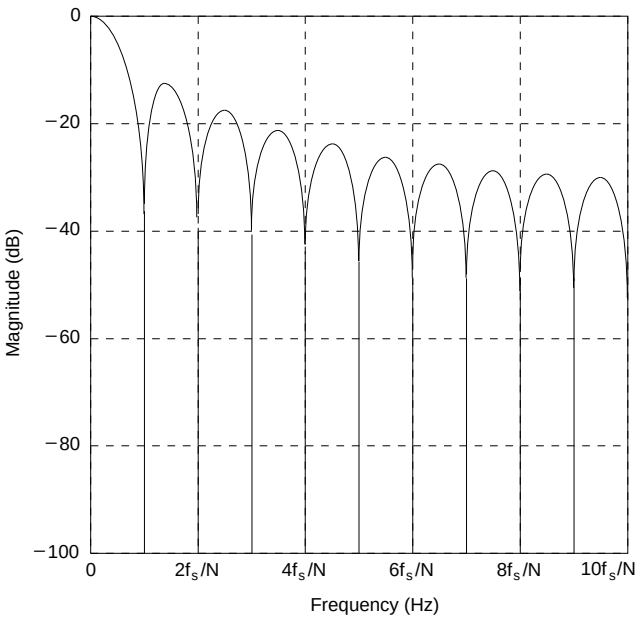


Figure 7. Averaging Filter Response

A digital filter's *impulse response* is what determines its filter function. It is basically a weighting function applied to the sequence of samples being considered. The averaging filter is an elementary example of an FIR filter because it uses equal weighting (weight = 1/N where N = # samples). More sophisticated impulse responses extract the information contained in the *relationship between samples*. Averaging filters ignore this information.

Figure 8 illustrates how an FIR filter actually implements the impulse response. The two basic operations are multiplication (indicated by ⊗) and addition - or accumulation - (indicated by Σ). Filter coefficients a_0 to a_3 represent the impulse response. The three unit delay elements insure

that each output is calculated using the current input sample and the three previous samples. The filter's input, x(n), and output, y(n), are digital words of any length. (For the CS5317, x(n) is 1-bit and y(n) is 16-bits). Each digital output requires one complete *convolution*. For the 4th-order filter shown in Figure 8, one convolution consists of four multiplications and the accumulation of the four products.

FIR filters are often described in terms of *taps*. This terminology hails back to analog transversal filters, which were basically analog implementations of the filter in Figure 8. The analog delay elements were termed taps. The number of taps indicated the filter's impulse duration. The longer the duration, the more powerful the filter.

Decimation

Digital filters often operate with input sampling rates well above the bandwidth of interest. This serves to minimize analog anti-alias filtering requirements. The filter's output rate, however, is generally dropped to a more manageable system sampling rate. Any reduction in sampling rate is termed *decimation*.

To illustrate the decimation process let's return to averaging. A filter which collects ten samples and then averages them to produce one output *decimates by ten*. That is, for an input rate of f_S, the output rate is $f_S/10$. Alternatively, one could use a "rolling average." For each input sample received, an output would be calculated using that sample and the nine previous samples. The sampling rate would therefore remain at f_S with no decimation.

The 4th-order FIR filter in Figure 9 exhibits the same filter response as that in Figure 8, but decimates by a factor of four. In this case, only one multiplication is performed per input cycle. Without any delay elements, the accumulator needs four input cycles to complete one convolution. Output samples are therefore produced at $f_S/4$. Decimation clearly relaxes computational complexity.

Decimation does not affect overall signal-to-noise or dynamic range. For this reason, one can decimate the CS5317's 20 kHz output (by selectively reading a fraction of the available samples) without affecting the converter's noise. However, a digital signal is normally not decimated if additional filtering is to be used to increase dynamic range (and resolution). All noise energy in a sampled signal lies between dc and one-half the sampling rate. Lower sampling rates therefore exhibit larger noise *densities* in the bandwidth of interest for a given amount of noise energy due to aliasing.

FIR Characteristics

The only source of inaccuracy in digital filters is rounding errors due to finite word lengths in the

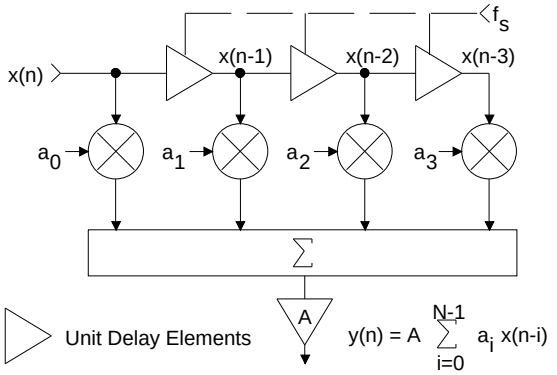


Figure 8. 4th-order FIR Filter

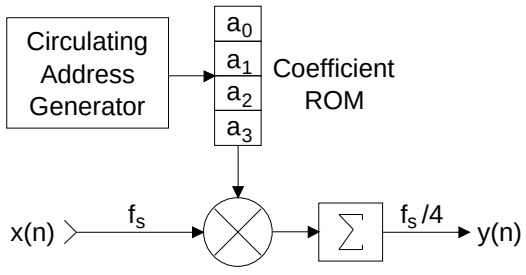


Figure 9. 4th-order FIR Filter with 4X Decimation

computations. If properly designed, a digital filter will not induce linearity, offset, or gain errors.

Aside from their simplicity, FIR filters' most popular characteristic is their ability to implement perfectly linear phase filters. The effect of every input sample on the output is always seen a *fixed* number of cycles later. This processing delay from input to output is termed the filter's *group delay*, and can be shown to equal one-half the impulse response duration.

Unfortunately, FIR filters can only implement zeroes, no poles. Roll-off is therefore limited. Of course, this limitation can be overcome by cascading FIR filters to produce an extraordinarily long impulse duration. (Fortunately stability is not an issue with FIR filters). The trade-off, though, is an extraordinarily long group delay.

IIR Filters

Infinite Impulse Response filters, on the other hand, can implement zeroes *and poles* to achieve high roll-off. Unlike FIR filters, which use previous inputs to calculate an output, IIR filters also utilize *historical output information* to calculate each new output. In this manner, IIR filters can implement mathematical filter equations with variables in the denominator (that is, poles).

The only drawback to IIR filters is their computational complexity. Since their computations use historical information on their past outputs, *each output must be calculated*. That is, unlike FIR filters an IIR filter cannot decimate to reduce computational complexity. Therefore, IIR filters generally operate with lower sampling rates.

The CS5317 Voice-band A/D Converter Implementation

The CS5317 uses oversampling, decimation, and FIR filtering to implement its digital filter. The CS5317 samples its analog input at 2.5 MHz (for a full-rated 5 MHz master clock). This high oversampling ratio of 500:1 (2.5 MHz sampling/5 kHz bandwidth) reduces external analog anti-alias requirements.

The FIR filter decimates the sampling rate from 2.5 MHz to 20 kHz to reduce computational complexity. The filter features an impulse response duration of 384 x 2.5 MHz and a decimation ratio of 128 (2.5 MHz:20 kHz). Since the filter does not decimate by 384 as shown in Figure 9, multiple convolutions must be in process concurrently. To achieve this, the CS5317 uses three accumulators working from a single 384-word coefficient memory. The three convolutions are spaced to begin and end 128 samples apart. Thus, a new 16-bit output sample becomes available every 128 input samples (for a decimation ratio of 128) whereas each 16-bit output is calculated using 384 input samples (for an impulse response duration of 384).

The CS5501 dc Measurement A/D Converter Implementation

The CS5501 uses oversampling, decimation, and both FIR and IIR filtering to implement its 6-pole Gaussian filter. The CS5501 samples its analog input at 16kHz (for a full-rated 4.096 MHz master clock). This high oversampling ratio of 1600:1 (16 kHz sampling/10 Hz bandwidth) reduces *and most often eliminates* external analog anti-alias requirements.

The FIR filter is used to decimate the sampling rate from 16 kHz to 4 kHz to reduce computational complexity in the subsequent IIR filter. The FIR filter response is not especially critical. Its only goal is to reject energy within ±10 Hz bands around integer multiples of 4 kHz, the IIR filter's sampling rate.

The IIR filter is needed to implement the poles in the 6^{th}-order Gaussian filter and achieve high roll-off of 120dB/decade. Its baseband filter characteristics are shown in Figure 10. Note that the

filter's entire frequency response can be scaled by adjusting the master clock. The converter's sampling rate simply scales accordingly. With its cut-off frequency set at 10 Hz (4.096 MHz master clock) for maximized settling, the CS5501 offers 55 dB rejection at 60Hz. With a 5 Hz cut-off, though, 60 Hz rejection increases to greater than 90 dB. Master clocks as low as 40.96 kHz are acceptable, yielding cut-off frequencies as low as 0.1 Hz.

The CS5335 Digital Audio A/D Converter Implementation

The CS5335 uses a three stage digital filter architecture. Each of the two modulators outputs a 6.144 MHz 1-bit stream into a comb filter stage. The comb filter is a fifth order Sinc function which decimates by 32. The output of the comb filter is then passed to two additional stages of filtering. The finite-impulse-response (FIR) stage which follows the comb filter has 20 taps and decimates by 2. This stage provides compensation for the gain error of the comb function. The final FIR stage has 127 taps and also decimates by 2. The entire filter achieves passband ripple of 0.002 dB from dc to 22 kHz, a transition band from 0.4535 Fs to 0.5465 Fs , and stopband attenuation of at least 85 dB. The filter provides antialiasing filtering at the word rate of 48 kHz, attenuating all analog frequencies from 26.2 kHz to 6.118 MHz.

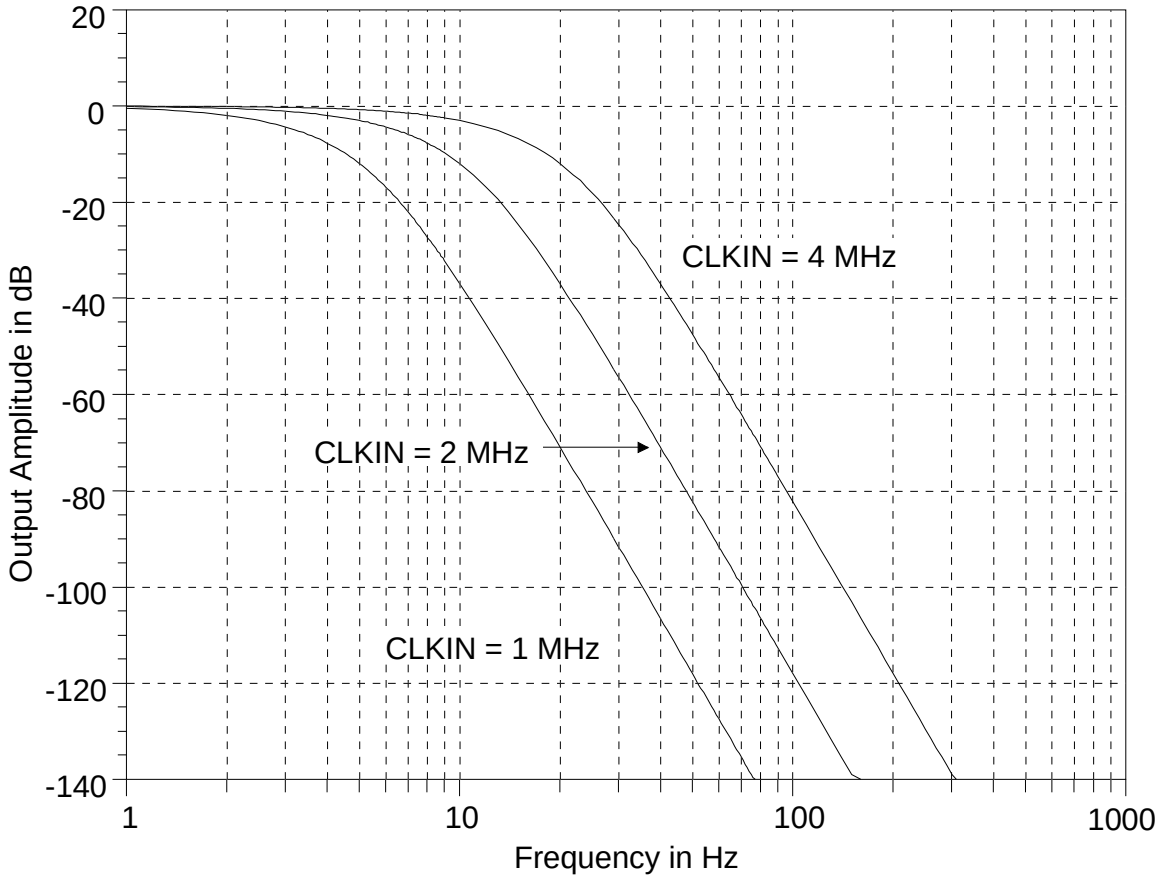


Figure 10. CS5501 Frequency Response