CS89712

High-Performance, Low-Power System-on-Chip with 10BASE-T Ethernet Controller

Marketing Brief

FEATURES

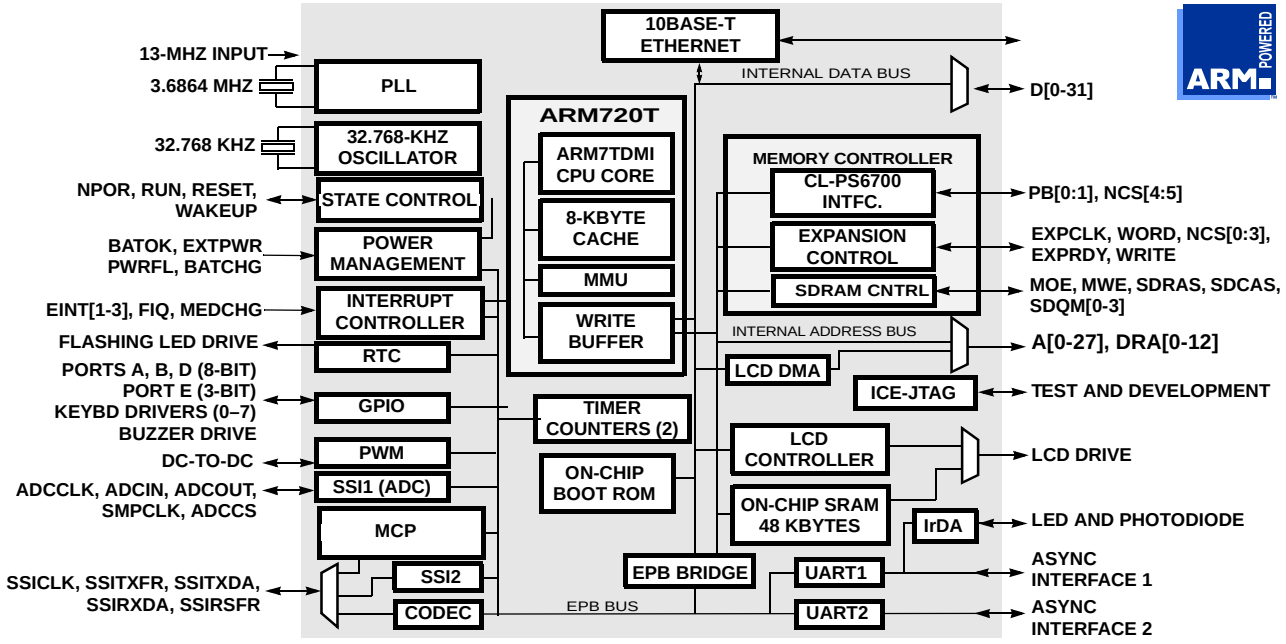
- **Massively integrated Network Enabled System-on-a-Chip**
- **High-Speed CPU and all major system peripherals**
- **Minimizes need for external components**
- **Maximizes design simplicity**
- **Ultra low power 66 DMIPS ARM720TDMI CPU with performance matching a 100-MHz Intel Pentium® based PC**
- **Dynamically programmable clock speeds of 18, 36, 49, and 74 MHz for power savings**
- **Ultra Low-Power 2.5 V implementation for power critical embedded designs**
- **Full featured 10BaseT controller**
- **6 external memory segments expansion**
- **Embedded 48KB data and program SRAM**
- **Programmable External Memory Controller Supports SDRAM, SRAM, ROM, and FLASH**
- **Comprehensive Suite of Software Drivers**
- **Linux and other OS support**

OVERVIEW

The CS89712 is designed for ultra-low-power communication applications such as: VoIP telephony, screen phones, Web appliances, email appliances, digital picture frames, and other network applications. With the added capabilities for expansion on the CS89712, router and bridges for home networking or wireless networking can be implemented.

The core-logic functionality of the device is built around an ARM720TDMI processor with 8 K-bytes of four-way set-associative unified cache and a write buffer. Incorporated into the ARM720TDMI is an enhanced memory management unit (MMU) which allows for support of sophisticated real time operating systems such as Vxworks or Linux.

In order to minimize external components, CS89712 incorporates all of the major system level peripherals including 10base-T Ethernet, Ethernet buffer memory, LCD controller, expansion memory controller, peripheral ports, internal zero wait state SRAM memory, and internal boot ROM. JTAG is also available on the CS89712 to speed up development with an in circuit emulator (ICE) and for use in production test.



ADDITIONAL FEATURES AND PERIPHERALS

- Sleep Modes
- LCD controller
- Interfaces directly to a single-scan panel monochrome LCD
- Panel width size is programmable from 32 to 1024 pixels in 16-pixel increments
- Video frame buffer size programmable up to 128 KB
- Bits per pixel of 1, 2, or 4 bits
- SDRAM controller
- Supports up to two banks of SDRAM
- Memory controller
- Decodes up to 5 separate memory segments of up to 256 MB each
- Each segment can be configured as 8, 16, or 32 bits wide and supports page-mode access
- Programmable access time for conventional ROM / SRAM / FLASH memory
- Supports Removable FLASH card interface
- Enables connection to removable FLASH card for addition of expansion FLASH memory modules
- 48 KB of on-chip SRAM for fast program execution and/or as a video frame buffer
- EEPROM Support for Jumperless Configuration of Ethernet port
- LED Drivers for Link Status and LAN Activity
- Synchronous serial interface
- ADC (SSI) Interface: Master mode only; SPI® and Microwire1®-compatible, ADI, and CODEC
- On-chip ROM; for manufacturing support
- 27-bits of general-purpose I/O
- Three 8-bit and one 3-bit GPIO port
- Supports scanning keyboard matrix
- Two UARTs (16550 type)
- Supports bit rates up to 115.2 kbps
- Contains two 16-byte FIFOs for TX and RX
- UART1 supports modem control signals
- SIR (up to 115.2 kbps) infrared encoder / decoder
- IrDA (Infrared Data Association) SIR protocol encoder / decoder
- DC-to-DC converter interface (PWM)
- Provides two 96-kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a DC to DC converter
- Two timer counters
- Support for up to two ultra-low-power CL-PS6700 PC Card controllers
- 32-bit Y2K-compliant real time clock and comparator
- Dedicated LED flasher pin from RTC
- 256-ball PBGA package
- Evaluation kit available with BOM, schematics, layout and sample code

DESCRIPTION

CPU Operation

- ARM720TDMI processor incorporates the following functional sub-blocks:
  - ARM7TDMI CPU core (which supports the logic for the Thumb instruction set, core debug, enhanced multiplier) running at a dynamically programmable clock speed of 18/36/49/74 MHz
  - Memory Management Unit (MMU) compatible with the ARM710 core (providing address translation and a 64-entry translation lookaside buffer)8 KB of unified instruction and data cache with a four-way set associative cache controller
  - Write buffer

Power Management

The CS89712 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5V-3.3 V. the device has three basic power states:

Idle — This state is the same as the Operating State, except the CPU clock is halted while waiting for an event such as a key press.

Snooze — This state is the same as the Standby state, except that the PLL, oscillator, and LCD display are enabled. The on-chip SRAM is used to store the video display data.

Standby — This state is equivalent to the computer being switched off (no display), and the main oscillator shut down. An event such as a key press can wake-up the processor.

Memory Interfaces

There are two main external memory interfaces.

The first one is the ROM / SRAM / FLASH-style interface that has programmable wait-state timings and includes burst-mode capability, with eight chip selects decoding six 256-MB sections of addressable space. For maximum flexibility, each bank can be specified to be 8, 16, or 32 bits wide. This allows the use of an 8-bit-wide boot ROM option to minimize overall system cost. The on-chip boot ROM can be used in product manufacturing to serially download system code into system FLASH memory. To further minimize system memory requirements and cost, the ARM Thumb® instruction set is supported, providing for the use of high-speed 32-bit operations in 16-bit op-codes and yielding industry-leading code density.

The second is the SDRAM interface that allows direct connection of two banks of SDRAM, for a total of 64 MB. The CS89712 supports self-refresh SDRAMs and SDRAM power down, assuring the lowest possible power consumption.

A DMA address generator is also provided that fetches video display data for the LCD controller from main SDRAM memory. The display frame buffer start address is programmable. In addition, the built-in LCD controller can utilize internal SRAM for memory, thus eliminating the need for SDRAMs.

Ethernet Port

The CS89712 Ethernet port incorporates all of the analog and digital circuitry needed for a complete Ethernet circuit. Major functional blocks include: an 802.3 MAC engine; 4 KB integrated buffer memory; a external serial EEPROM interface; and a complete analog front end for 10BASE-T. The 10BASE-T transceiver includes drivers, receivers, and analog filters, allowing direct connection to low-cost isolation transformers.

LCD Display Controllers

The LCD controller provides all the necessary control signals to interface to a directly to a single panel multiplexed LCD. The panel size is programmable and can be any width from 32 to 1024 pixels in 16 pixel increments. The maximum panel size is 1024x256 pixels in 4-bits-per-pixel. The frame buffer can be located in internal or external memory and a LCD DMA is provided to off load CPU bandwidth

Serial Interfaces

The CS89712 includes two 16550-type UARTs for RS-232 serial communications, both of which have two 16-byte FIFOs for receiving and transmitting data. The UARTs support bit rates up to 115.2 kbps. An IrDA SIR protocol encoder / decoder can be optionally switched into the RX / TX signals to / from one of the UARTs to enable these signals to drive an infrared communication interface directly.

In addition to the dual UARTs, four synchronous serial interfaces are provided as listed in Table 1.

Type	Comment	Max Transfer
SPI/Microwire 1	Master	128Kb/s
SPI/Microwire 2	Master/Slave	512Kb/s
DAI Interface	CD quality DACs and ADC	1.536Mb/s
CODEC Interface	Only use in PLL Clock mode	64Kb/s

Table 1. Serial Interface Options

SSI1 supports master mode only. The other three serial interfaces (SSI2, DIA, and CODEC) are multiplexed onto a single set of interface pins. SSI2 supports both master and slave mode. Both SSI1 and SSI2 support two industry-standard protocols (SPI and Microwire) for interfacing standard analog converters (e.g., CS552x or CS553x ADC), and for allowing peripheral expansion (e.g., a digitizer pen, additional networking peripherals such as Homeplug™ powerline networking controllers).

The full-duplex DAI interface allows direct connection to many low cost, low power, high quality audio converters. In particular, the DAI can directly interface with the Crystal® CS43L4x audio DAC and the CS53L3x ADC, allowing storage and playback of high quality sound.

The CODEC interface allows direct connection of a telephony type CODEC to the CS89712 for VoIP applications.

Expansion Bus

Six separate linear memory or expansion segments are decoded by the CS89712, two of which can be reserved for two PC Card controllers, each interfacing to separate single CL-PS6700 devices. This provides capabilities to add off the shelf PC Cards such as memory, HomeRF, 802.11, and HPNA cards. The flexibility of the expansion bus also provides glueless connection to industry standard networking controller adapters components such as the CS8900A Ehternet, HPNA, and 802.11 wireless LAN controllers.

Packaging

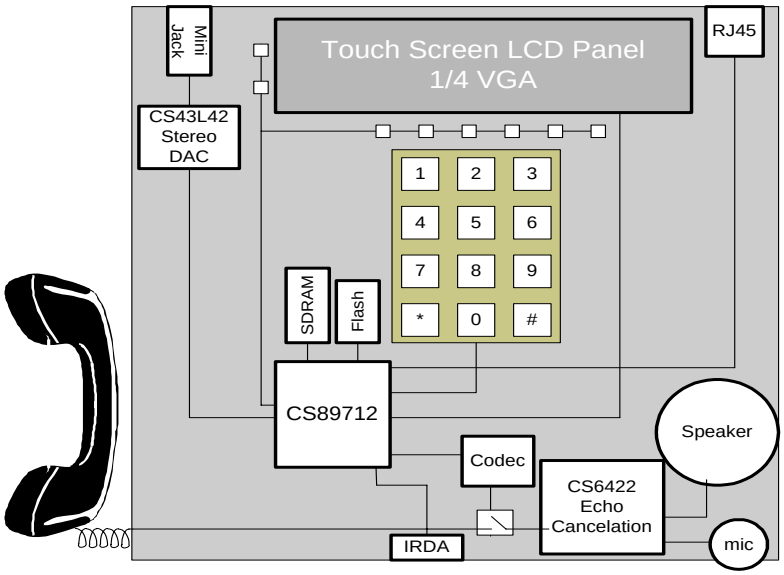
The CS89712 is available in a 256-ball PBGA package.

System Design

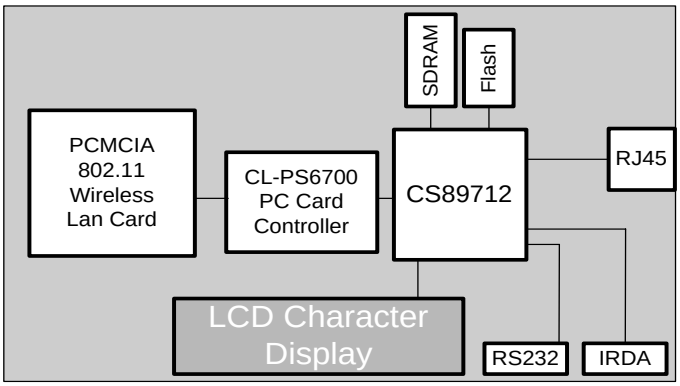
As shown in application examples, simply adding desired memory and peripherals to the highly integrated CS89712 completes a low-power network system solution. All necessary interface logic is integrated on-chip

Example Application

VoIP Internet Appliance
ViOP Telepone Speaker Phone
Streaming Audio
Web Brower



Wireless LAN Brigde/Router



Contacting Cirrus Logic Support

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