06/05/00

CS5460 Rev. C Errata

(Reference CS5460 Data Sheet revision DS279PP5 dated JAN '00)

Note: This product is classified at Quality Level "QPL IV"

1. Voltage Channel Noise (Referred to Input)

Specified 250 µV Maximum

Rev. C 350 µV Maximum

Comments The CS5460 will meet the data sheet specification in future revisions. The Current Channel has over 90% of the noise budget for the low-rate measurements and, therefore, the impact of the Voltage Channel noise will be virtually unnoticed in Energy and V_{RMS} measurements.

2. V_{RMS} and I_{RMS} Calculations overflow

Specified Internal Registers in the Power Calculation Engine should have enough range with maximum inputs and cycle count, N = 4000.

Rev. C V_{RMS} and I_{RMS} Internal Registers overflow when inputs exceed 50% of full-scale and N = 4000.

Comments The CS5460 will meet the data sheet specification in future revisions. When setting N = 4000, the gain calibration registers can be set to 0.5 to prevent overflow. RMS values of 0.5 will represent a full-scale input. This has minimal impact on accuracy or dynamic range.

3. External Clock with VA = ±2.5V; VD+ = +3V; DGND = 0V

Specified Internal or external clock will work for all power supply configurations.

Rev. C External clock does not work for VA = ±2.5V; VD+ = +3V; DGND = 0V.

Comments The CS5460 will meet the data sheet specification in future revisions. Note: External clock *can* be used with VA+ = +3V; VA- = –2V; VD+ = +3V; DGND = 0V.

4. Power Consumption in Sleep Mode

Specified 10 µW Typical

Rev. C 15 µW Typical and 50 µW Maximum

Comments The CS5460 will meet the data sheet specification in future revisions.

5. VREFOUT Load Regulation

Specified 6 mV Typical and 10 mV Maximum

Rev. C 8 mV Typical and 15 mV Maximum

Comments The CS5460 will meet the data sheet specification in future revisions.

6. Erroneous /EDIR Pulses

Specified /EDIR pin and /EOUT pin will both issue one pulse if the negative energy threshold has been reached in the pulse-output energy accumulation register.

Rev. C /EDIR pulses detected on /EDIR may be false/invalid if the Pulse-Rate Register is set to a value less than 4679 Hz. The /EDIR functionality should not be used if desired Pulse-Rate Register setting is less than 4679 Hz.

Note: Pulse-rates less than 4679 can be achieved by *gain-scaling*:

1. Determine the pulse-rate desired by the user. Call this 'DR'. (Example: 50Hz)
2. Set the Pulse-Rate Register to a value greater than 4679. Call this 'PR'. (Example: 4700Hz)
3. Define x = DR / PR. Scale the *product* of voltage and current gain register settings by a factor of x.

This technique still allows for sub-hertz full-scale pulse rates with over 3 orders of magnitude of power dynamic range. To maximize dynamic range, use Pulse Rate Register settings close to (but not below) 4700 Hz. The CS5460 will meet the data sheet specification in future revisions.

If there are any questions concerning this information, please contact the Crystal Power Measurement team. For questions contact any of the team members or send email to powermeter@crystal.cirrus.com. Visit our web site http://www.cirrus.com or call our literature department at +1 (800) 888-5016 ext. 3594 or +1 (512) 912-3594 for data sheets and application notes.

For application support, schematic and layout review call 512-912-3652