Introduction

The CL8000 product family is designed for socket compatibility with Altera's FLEX 8000 product family. In order to achieve this socket compatibility, the CL8000 uses or emulates the operating modes and configuration schemes of the FLEX 8000. This document describes how the CL8000 achieves FLEX 8000 compatibility during configuration loading.

Background

FLEX 8000 Operating Modes

The FLEX 8000 series of devices is configured based on data stored in static RAM cells. This information must be initialized each time the device is powered up. The FLEX 800 has three modes of operation to accommodate this configuration requirement:

Configuration Mode: During configuration mode the configuration data is loaded into the FLEX 8000 device from an external memory component.

Initialization Mode: Initialization begins once configuration is completed. During initialization, registers are reset, I/O pins are enabled, and the device commences operation in the system as a logic component.

User Mode: While in User Mode the FLEX 8000 device operates in the circuit performing the logic function for which it was designed.

FLEX 8000 Configuration Schemes

The FLEX 8000 can employ one of six configuration schemes. These schemes can be either *active*, where the FLEX 8000 controls the configuration procedure, or *passive*, where the FLEX 8000 configuration is controlled by an external device. The six configuration schemes are summarized below:

Active Serial: Active Serial configuration uses an external serial EPROM device for data storage. The FLEX 8000 controls the configuration process.

Active Parallel Up: In Active Parallel Up configuration, the FLEX 8000 generates ascending sequential addresses which are used to access data in an external PROM.

Active Parallel Down: In Active Parallel Down configuration, the FLEX 8000 generates descending sequential addresses which are used to access data in an external PROM.

Passive Serial: In this configuration scheme, the FLEX 8000 is configured using a serial bitstream from an external controller. In this scheme, the FLEX 8000 acts as a slave device.

Passive Parallel Synchronous: Passive Parallel Synchronous configuration uses an external host to configure the FLEX 8000 device using an 8-bit wide data path. Configuration data is latched and serialized synchronously with the DCLK signal.

Passive Parallel Asynchronous: This configuration mode uses an external host to configure the FLEX 8000 device through an 8-bit wide data path. Configuration data is latched using handshaking signals, and is serialized using the internal oscillator of the FLEX 8000.

Configuration Pin Functions

The configuration scheme for a FLEX 8000 device is determined by the value of the nSP, MSEL0, and MSEL1 pins. A truth table for configuration scheme selection is shown in Table 1. Configuration selection for the CL8000 is described in a later section of this application note.

nSP	MSEL1	MSEL0	Configuration Scheme
0	0	0	Active Serial (AS)
0	0	1	Reserved
0	1	0	Passive Serial (PS)
0	1	1	Reserved
1	0	0	Active Parallel Up (APU)
1	0	1	Passive Parallel Synchronous (PPS)
1	1	0	Active Parallel Down (APD)
1	1	1	Passive Parallel Asynchronous (PPA)

Table 1. Configuration Scheme Truth Table

The CL8000 either uses or emulates the Altera-defined function of the FLEX 8000 configuration pins. These pins, as well as their function and usage, are defined in Table 2. Again, the CL8000 will completely emulate the functionality of the FLEX 8000 in this area.

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nSP MSEL1 MSEL0	NA	All	Input	The combination of these three inputs is used to determine the configuration scheme, as shown in Table 1.
nSTATUS	NA	All	Bidirectional Open Drain	The CL8000 will drive this signal low at the start of the configuration cycle and release it after 4 DCLCK pulses. If an external source drives nSTATUS low after the Cl8000 has released it, the configuration process will be aborted.
nCONFIG	NA	All	Input	When this signal is driven LOW the CL8000 will be reset. A LOW to HIGH transition initiates the configuration process.
CONF_DONE	NA	All	Bidirectional Open Drain	This signal is held LOW by the CL8000 during the configuration process. A HIGH input causes the device to execute the initialization process and enter user mode.
DCLK	DCLK	AS PPS, PS	Output Input	Clock source for external PROM devices. Clock input from external host.
nWS	I/O	PPA	Input	Write strobe input. Does not impact CL8000 function.
nRS	I/O	PPA	Input	Read strobe input. A low input causes the CL8000 to place the RDYnBUSY signal on the DATA7 pin.
RDCLK	I/O	APU, APD	Output	Divide by 8 of DCLK.
nCS CS	I/O	PPA	Input	Chip select input. Does not impact CL8000 function.
RDYnBUSY	I/O	PPA	Output	Ready output.On the CL8000, this signal emulates the handshaking required for PPA configuration.
CLKUSR	I/O	All	Input	Optional user-supplied clock input for initialization.
ADD17 to ADD0	I/O	APD, APU	Output	Address outputs. These signals emulate the FLEX 8000 addressing for APU and APD configuration.
DATA7 to DATA0		APD, APU, PPA, PPS	Input	Does not impact CL8000 function in these configuration schemes
DATA0	I/O	AS, PS	Input	In AS/PS schemes the CL8000 will monitor this pin for the 64h preamble
DATA7		PPA	Output	In the PPA configuration scheme this pin can be used to present the RDYnBUSY signal.
SDOUT	I/O	All	Output	Driven HIGH during configuration.

Table 2. Configuration Pin Functions.

CL8000 Configuration Emulation

Since the CL8000 is not a programmable device, it does not need to be loaded with configuration data. However, to maintain compatibility with existing Altera-based designs, the CL8000 will operate as if it were being loaded with data during all configuration operations. Thus, timing and value of the various control signals will be identical to the FLEX 8000.

In all configuration modes, the CL8000 is forced into a reset state when nCONFIG is low. The actual configuration process starts when the nCONFIG pin goes from low to high. This could be at initial power up or at any time later. When nCONFIG is pulled low nSTATUS will be driven low within one to two DCLK cycles. Once the nCONFIG pin is driven high nSTATUS will be held low for four or five DCLK cycles and then released.

During the configuration process the CL8000 will hold CONF_DONE low. At the completion of configuration the CL8000 will release CONF_DONE. The CL8000 device will then monitor CONF_DONE and start the initialization phase when CONF_DONE is high.

The six Altera-compatible configuration schemes follow:

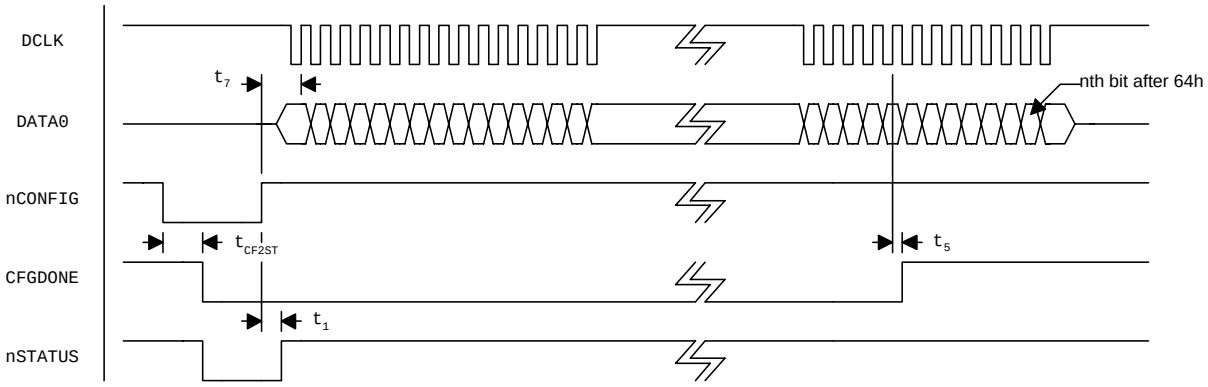

Figure 1. Active Serial Configuration

Active Serial

In this configuration scheme the CL8000 will emulate configuration, toggling the DCLK signal at a frequency of 4MHz ±1MHz, and a nominal 50% duty cycle. The CL8000 will count the correct number of memory cycles as described below. Active Serial configuration waveforms are shown in Figure 1.

The CL8000 will monitor the incoming data on DATA0. This data will start out as all F_H. When the CL8000 first sees the program length preamble it will start counting DCLK cycles. After the appropriate number of cycles (based on device size) CONFIG_DONE will be released.

Active Parallel Up

In this configuration scheme the CL8000 will count up through the valid addressing sequence while toggling RDCLK, starting at 00000_H and finishing at the appropriate value for the given CL8000 device. The CL8000 will output this count on the ADD[17..0] pins. Any data on the DATA[7..0] pins will be ignored.

The RDCLK output is generated by dividing DCLK by eight. The rising and falling edges of RDCLK will occur within 20ns. of the rising edge of DCLK, and the frequency will be 500 kHz ±125 kHz with a nominal duty cycle of 12.5%.

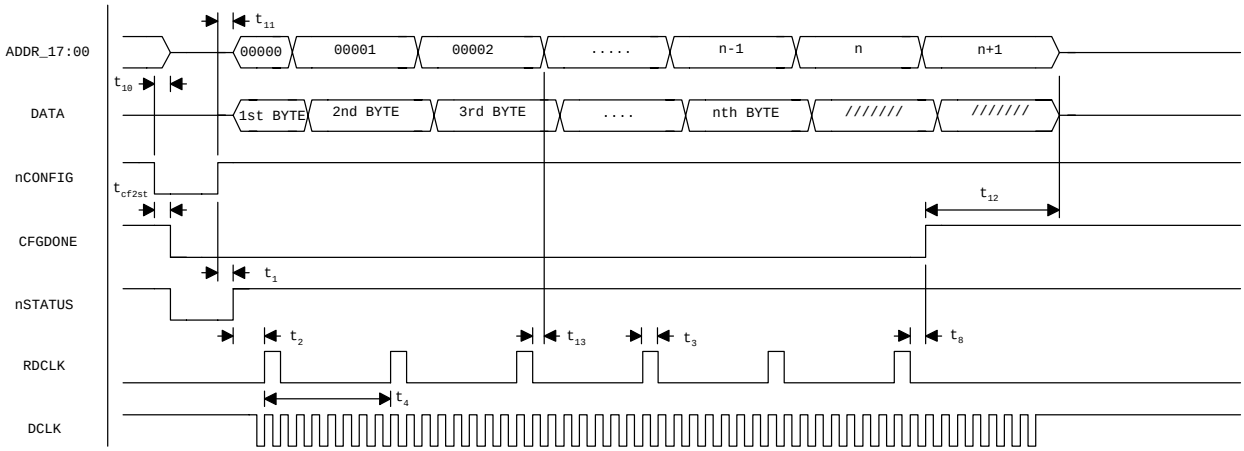

Figure 2. Active Parallel Up Configuration

The signal waveforms for Active Parallel Up configuration are shown in Figure 2.

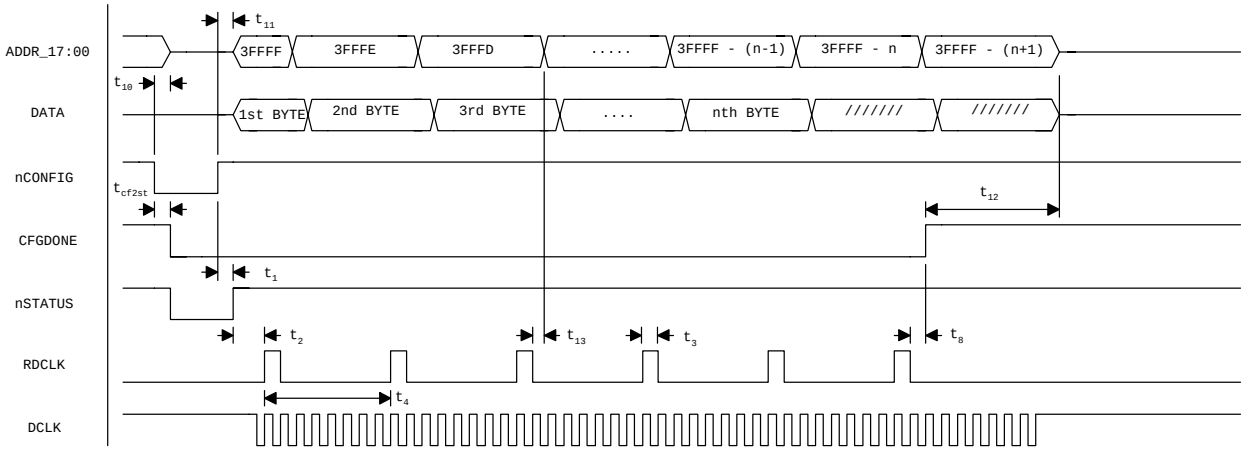

Figure 3. Active Parallel Down Configuration

Active Parallel Down

In this configuration scheme the CL8000 will count down through the valid addressing sequence while toggling RDCLK, starting at $3FFFF_H$ and finishing at the appropriate value for the given CL8000 device. The CL8000 will output this count on the ADD[17..0] pins. Any data on the DATA[7..0] pins will be ignored.

The RDCLK output is generated by dividing DCLK by eight. The rising and falling edges of RDCLK will occur within 20ns. of the rising edge of DCLK, and the frequency will be 500 kHz ±125 kHz with a nominal duty cycle of 12.5%.

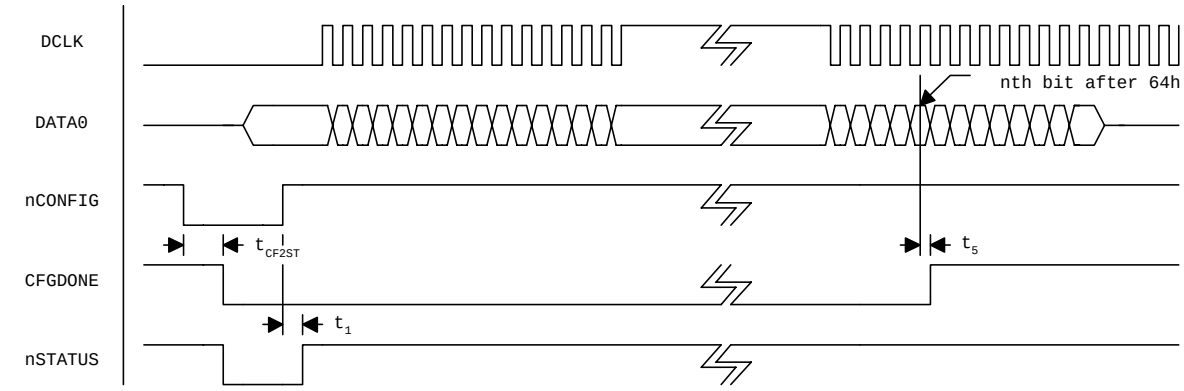

Figure 4. Passive Serial Configuration

Passive Serial

In this configuration scheme the CL8000 will monitor the incoming data on DATA0. This data will start out as all F_H, when the CL8000 device first sees the Program length preamble (64_H bit pattern) it will start counting DCLK cycles. After the appropriate number of clock cycles (based on the CL8000 device type) CONF_DONE will be released.

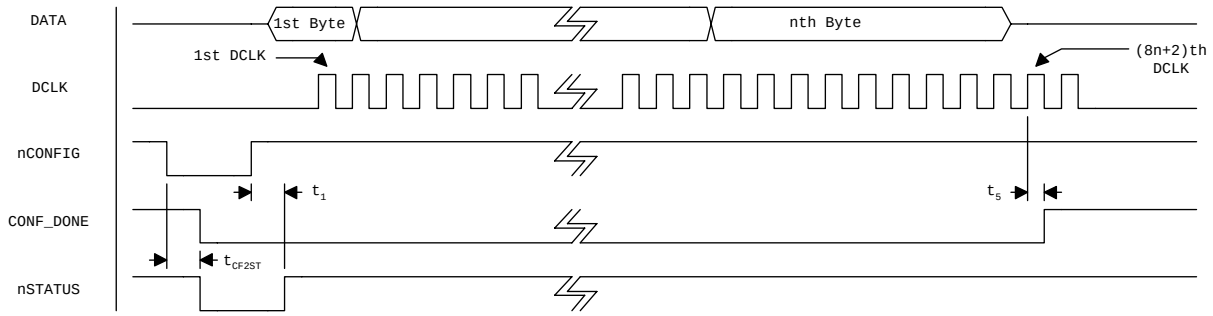

Figure 5. Passive Parallel Synchronous Configuration

Passive Parallel Synchronous

In this configuration scheme the CL8000 will emulate configuration by counting the appropriate number of clock cycles (based on the CL8000 device type) of the externally driven DCLK. The DATA[7..0] pins will be ignored. After the appropriate number of clock cycles CONF_DONE will be released.

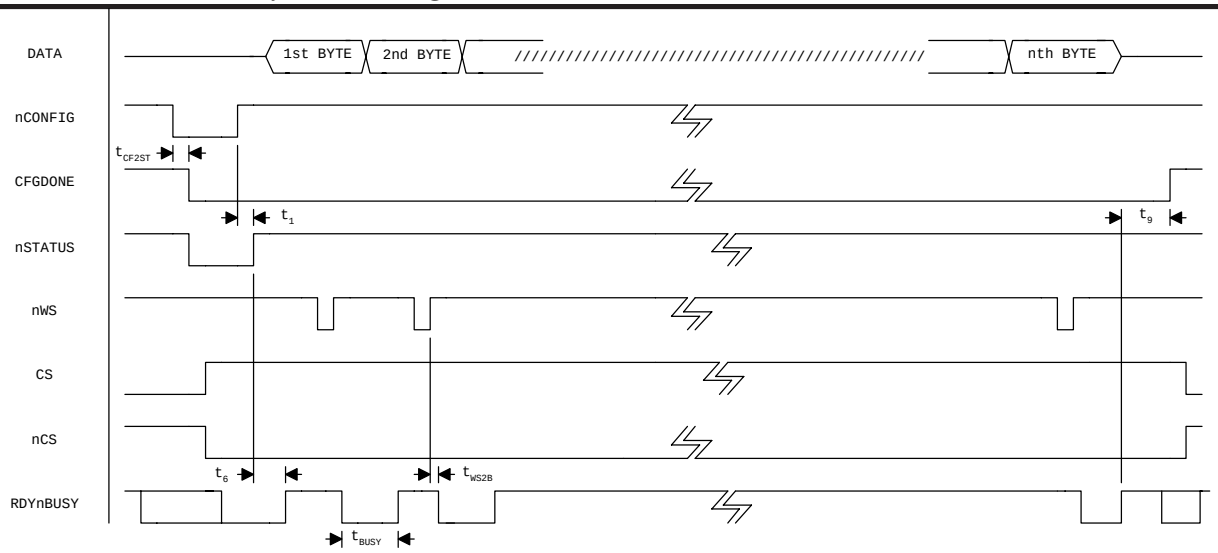

Figure 6. Passive Parallel Asynchronous Configuration

Passive Parallel Asynchronous

In this configuration scheme the CL8000 will emulate configuration by performing the appropriate number of handshake cycles, based on the CL8000 device type. There are two possible variations of the handshake.

1) If nRS is held high, the handshake cycle will start when nWS goes low while CS is high and nCS is low. The CL8000 device will then drive RDYnBSY low within 40nS for eight DCLK cycles. The DATA[7..0] pins will be ignored.

2) If nRS is pulsed low after nWS goes high, the handshake cycle will start when nWS goes low while CS is high and nCS is low. The CL8000 device will then drive the DATA7 pin low within 40nS for eight DCLK cycles. In this case DATA7 will be bidirectional. The DATA[6..0] pins will be ignored.

Configuration Option Bits

The FLEX 8000 product family has configuration options which are set during the design phase using the Max+Plus II development software. These options are controlled by the Device Configuration Option Bits. These bits are supported by the CL8000 family as follows:

User-Supplied Start-Up Clock

If this option is selected the CL8000 will utilize the user-supplied clock on the CLKUSR pin for its ten cycle initialization. If the option is not selected the ten cycle initialization will be clocked either by the CL8000 internal oscillator or by DCLK, as appropriate for the given configuration scheme.

Auto Restart on Frame Error

The value of this configuration bit does not affect CL8000 operation.

Release Clears before Tri-States

The function of this pin is identical to FLEX 8000 operation. If this option is selected then the CL8000 will release the Clear signal on all logic element and peripheral registers before releasing the Output Enable override on all tri-state buffers during initialization. Otherwise, the CL8000 will release the Output Enable signal on all logic element and peripheral registers before releasing the Clear override on all tri-state buffers during initialization.

Enable DCLK output in User Mode

Function of this pin is identical to FLEX 8000 operation. If this option is selected, the DCLK pin will be enabled when the device is operating in user mode. If this option is not selected, the DCLK pin will be disabled in User Mode.

Disable Start-Up Time-out

Function of this pin is identical to FLEX 8000 operation. If the option is disabled, the CL8000 will drive nSTATUS LOW if CONF_DONE does not go HIGH within ten clock cycles of being released by the device. Otherwise, the CL8000 will wait indefinitely for CONF_DONE to go HIGH before proceeding with initialization.

Enable JTAG Support

Function of this pin is identical to FLEX 8000 operation. When this option is set, JTAG testing is available on the four JTAG pins after configuration is completed. Otherwise, JTAG testing is not enabled.

Instant-On Configuration

The CL8000 is a hard-wired ASIC, rather than a programmable device. Therefore, configuration is required only for FLEX 8000 compatibility, not for correct operation. In order to take advantage of this characteristic, the CL8000 has an Instant-On configuration scheme which is not supported by the FLEX 8000 family.

When Instant-On has been specified, the CL8000 will enter User Mode ten DCLK cycles following the release of nCONFIG. Timing diagrams for Instant-On configuration are shown in Figure 7.

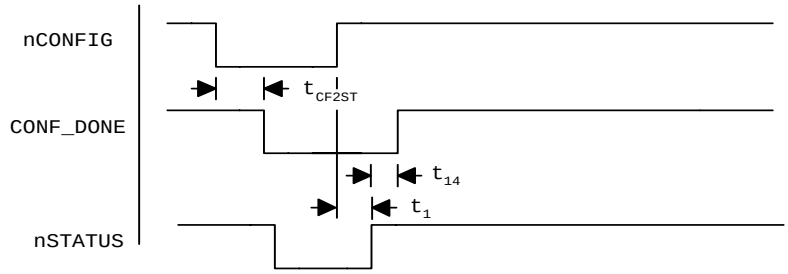

Figure 7. Instant-On Configuration

Instant-On configuration allows the elimination of external memory devices used to store FLEX 8000 configuration information. It may also dramatically reduce the time required to configure the system.

Selecting CL8000 Configuration

Within the CL8000 family there are two ways configuration is determined. For the CL8452A and the CL81188A, the configuration mode must be specified on the first article request form.

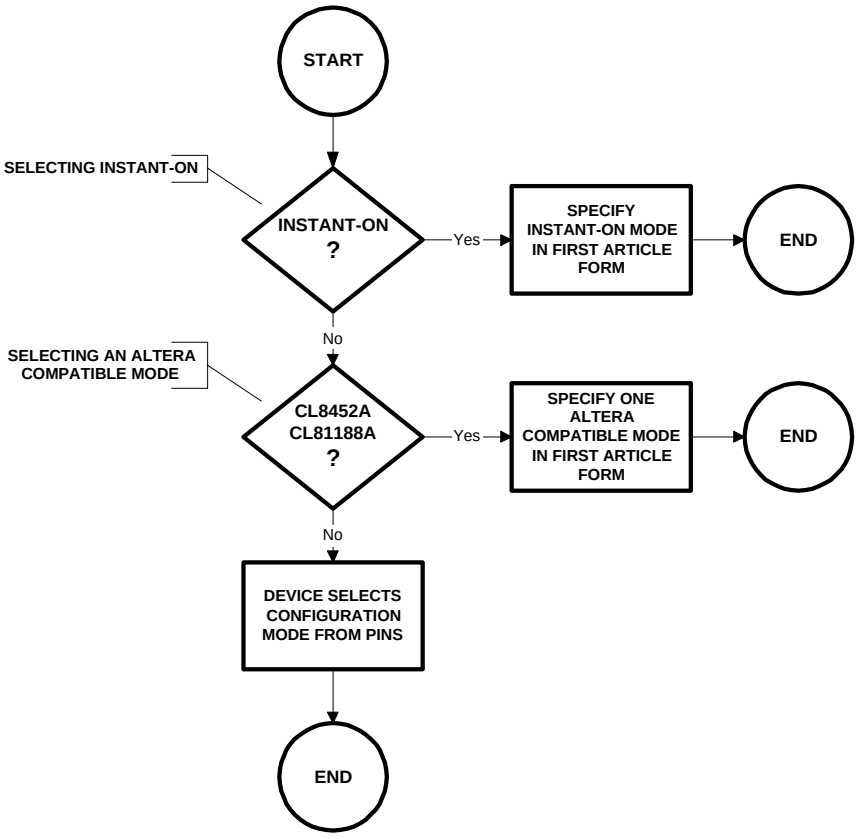

Figure 8. Customer Selection of CL8000 Family Configuration Mode

For other CL8000 family products, customers only specify Instant-On mode using the first article form. If Instant-On mode is not specified, the CL8282A, CL8636A, CL8820A, and the CL81500A select an Altera compatible mode based upon the state of the configuration mode pins nS/P, MSEL0, and MSEL1. The mode selection table is identical to that of Altera. See Table 1 in this application note. Specifying Instant-On mode overrides any other configuration mode selection.

Configuration Timing Values

Timing diagrams for the various configuration schemes are shown in Figures 1 through 7. The values of the timing parameters depicted in these diagrams are shown in Table 3.

Symbol	Parameter	Min	Max	Unit
tCF2ST	nCONFIG LOW to nSTATUS LOW	150	1000	ns
tWS2B	nWS rising edge to RDYnBUSY LOW		40	ns
tBUSY	RDYnBUSY LOW pulse width	1.3	4	µs
tCF2WS	nCONFIG HIGH to first nWS rising edge	5		µs
tDSU	Data set up time to nWS rising edge	50		ns
tDH	Data hold time from nWS rising edge	0		ns
tCSSU	Chip select delay before nWS rising edge	50		ns
tWSP	nWS LOW pulde width	500		ns
tRDY2WS	RDYnBUSY rising edge to nWS falling edge	50		ns
tWS2RS	nWS rising edge to nRS falling edge	500		ns
tRS2WS	nRS rising edge to nWS falling edge	500		ns
tRSD7	nRS falling edge to DATA7 valis with RDYnBUSY signal		50	ns
t1	nCONFIG HIGH to nSTATUS release	650	2500	ns
t2	nSTATUS release to first RDCLK rising edge		7.5	µs
t3	RDCLK HIGH pulse width	150	500	ns
t4	RDCLK period	1.3	4.0	µs
t5	DCLK rising edge to CFGDONE release		40	ns
t6	nSTATUS release to first RDYnBUSY	300	1000	ns
t7	nCONFIG HIGH to first DCLK rising edge	3.1	10.0	µs
t8	RDCLK falling edge to CONF_DONE		40	ns
t9	Last RDYnBUSY rising edge to CONF_DONE		1.5	µs
t10	nCONFIG LOW to ADDR high impedence	150	1000	ns
t11	nCONFIG HIGH to ADDR valid	1.1	4.0	µs
t12	CONF_DONE release to ADDR high impedence	650	2500	ns
t13	ADDR hold time from RDCLK falling edge	0		ns
t14	nSTATUS release to CONF_DONE release	0	2.5	µs

Table 3. Configuration Timing Parameters