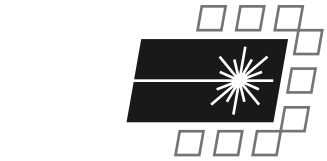


CL8000 TECHNOLOGY WHITE PAPER

Key Features

- Fast Cycle Times: Development and Production
- Easy Development with Altera FLEX 8000
- No Minimums
- No NRE
- Low power
- No Test Vector Development
- No Circuit Board Changes Required
- Mix and Match With FLEX 8000
- Non-Volatile Operation: No Configuration EPROM

Overview

The Clear Logic CL8000 Laser-Configured ASIC (LASIC™) family offers the ultimate combination of performance, flexibility, and cost. This family is an exact system level second source to Altera FLEX® 8000™ products.

Clear Logic simplifies the ASIC conversion problem by mapping only one FPGA product into one Clear Logic design. For example Altera's EPF8452A maps into the CL8452A. Each Clear Logic product is designed to support conversion of one FPGA product, the "source" FPGA.

If your system doesn't require in-system reprogrammability, you can literally design with Altera's software tools, launch pre-production with Altera devices, and then plug in the Clear Logic CL8000 equivalent. You need no circuit board changes and no tweaking or tuning.

Clear Logic laser-configured products give you the benefits of having an alternative source to field programmable products. They also allow you to reduce power consumption and system cost. Yet, you avoid ASIC conversion issues, porting to new tools, and conversion costs with our "no hassle" device. Clear Logic's innovative laser ASIC technology eliminates NRE costs, test vector development, ordering minimums and long lead times.

Key Elements of CL8000 Family Architecture

Recognizing the advantages and industry acceptance of the Altera FLEX families, Clear Logic has designed the CL8000 family to be an exact replacement in customer systems that do not require in-system reprogrammability.

You can prototype with FLEX 8000 programmable devices and then seamlessly transfer your working designs to the CL8000 family for volume production.

The Clear Logic CL8000 Laser-Configured ASIC family is based upon a large array of logic elements. Each logic element contains a configurable look up table for combinatorial functions and a register for sequential operations. A group of eight logic elements forms a block. Laser-configured metal fuses implement logical functions and control signal routing. Clear Logic offers you very short product delivery lead times because we implement your unique customer code as one of the final chip processing steps.

Laser configuration using fuses also provides a cost benefit. Laser fused configuration elements require much less die area than field programmable configuration registers. The resulting small die size leads to lower manufacturing costs.

Testing conventional ASIC circuits has always been a headache. Test vector generation impacts both development cost and time to market. Clear Logic takes care of the testing problem by putting it where it belongs: with us, not you. Our testable design and automatic test generation capability eliminate the test development problem when you use the CL8000 family. In addition, our TestCell™ technology, described later, ensures complete test coverage.

FLEX 8000 Compatibility

Bit Pattern Level Compatibility

Porting your Altera-based design to new tools to develop an ASIC certainly increases your development time. It may also introduce incompatibilities and errors. That's why we designed the CL8000 family to be fully compatible with the output file of the Altera MAX+PLUS® II software tool. All we need to convert your FLEX 8000 design is your bit stream.

Clear Logic extracts complete routing and placement information from the bit pattern that configures the field programmable product in your design. We use that information to configure laser fuses in the CL8000 family product. Our technique preserves routing and placement information so that the CL8000 maintains the internal timing relationships of the FLEX 8000 implementation.

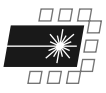
As a customer, you use Altera's MAX+PLUS II to generate the same target code both for the FLEX 8000 device and for the Clear Logic equivalent. This way you don't need to worry about introducing errors or changes to your design caused by porting it to a different tool platform.

Functional Patterns

Clear Logic's CL8000 design implementation maps the Altera FLEX architecture into a functionally equivalent device, even though laser configuration is very different from field programming. The CL8000 family contains more internal resources than the FLEX 8000 family. Designs that fit into FLEX 8000 devices will also fit into our products.

Timing Parameters

Metal routing lines that are laser configured by cutting metal fuses have less RC loading than field programmable products. Routing lines in field programmable products usually connect to the capacitive loading of several transistors. Because loading is less than or equivalent to the field programmable device, internal signals propagate as quickly in our laser-configured product. Performance of our CL8000 family product will meet or exceed that of Altera's field programmable counterpart. Since we match our routing and placement to your field programmable design, functional operation and relative timing performance will not change.



Configuration Loading

During the configuration loading process, the CL8000 is fully compatible with any of the six Altera FLEX 8000 configuration loading schemes. The CL8000 can reside in any position in the configuration chain during a multi-chip loading sequence. You may mix any combination of Altera FLEX and Clear Logic products in your system without disturbing the configuration loading of the Altera devices. You can also remove the configuration EPROM that stores the bit stream for the FLEX 8000 device that was replaced by the CL8000, if it is not required for other purposes in the system.

I/O Tuning

We have carefully matched the slew rates and drive capability of our I/O port design to the FLEX family. Analog issues like system noise and ground bounce have been the downfall of many "pin compatible" high speed digital integrated circuit substitutions. Our tuned I/O designs helps assure proper operation in your system.

Unique Benefits with Clear Logic

Power Consumption

Laser cut fuses do not add any significant capacitance to the signal lines to which they connect. Configuration transistors always increase the total line capacitance, even if they are in the "off" state. A typical field programmable device may have twenty or more transistors connected to a routing channel.

With much less capacitive loading in the chip, the CL8000 family has a much lower active power consumption specification than the Altera FLEX family.

Instant On Option

The Instant On option allows your system to begin operation immediately upon power-up. You can select this option when you submit your design files for prototypes. Remove your configuration storage device and substitute Clear Logic Instant On versions for all of the FLEX 8000 devices in your system. You'll have no more turn-on delays or configuration hassles!

Vcc Upset Tolerance

Non-volatile fuse elements control the configuration in Clear

Logic products. Power supply noise and fluctuations cannot disturb the configuration. You can even eliminate system supervisory chips and inadvertent "system reboots" related to losing configuration in field programmable products.

Cost Benefits

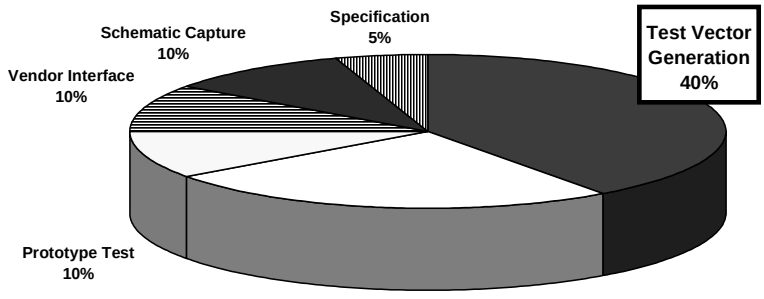
Laser-fused configuration elements occupy much less silicon area than the corresponding transistor storage elements and transistor routing switches needed in field programmable products. A single laser fuse is a combined switch and configuration memory. Laser configuration elements have as much as a five to one advantage over reprogrammable configuration elements. Smaller silicon die size reduces product cost.

In many systems, you will be able to eliminate a configuration storage device, such as a serial EPROM. Our product is preconfigured and non-volatile, unlike a field programmable product

Clear Logic TestCell™ Technology

Until now, ASIC solutions have required large investments of engineering effort and project development funds to develop test programs. Integrated Circuit Engineering Corporation (ICE) cites industry sources who, for typical ASICs, attribute 40% of engineering design time and 31% of project development cost to test. Customers needing a very high percentage of fault coverage may need to invest even more for test development.

The CL8000 contains unique design features that solve the testing problems associated with ASIC solutions. In addition to



Design Time by Task

Source: ASIC Technology News (via ICE, Inc.)

the register required for operation of each logic element, we add three test registers that can be scanned through the chip I/O pins. Only special test modes activate the test registers. They are not active during normal system operation.

Clear Logic uses the scan registers to segment your large, complex, customer-specific logic implementation on the chip into small TestCells. Then, based upon your customer-specific bit stream, Clear Logic automatically generates a series of test patterns for each TestCell. In this manner, we segment complex, difficult to test logic implementations, such as long chains of counters, into simple, easily tested blocks.

With testability built-in to Clear Logic products, you get 100% fault coverage. In addition, we test to your unique logic implementation. Field programmable device manufacturers must use generic patterns that do not test the operation of your specific design. Leave the testing to Clear Logic!

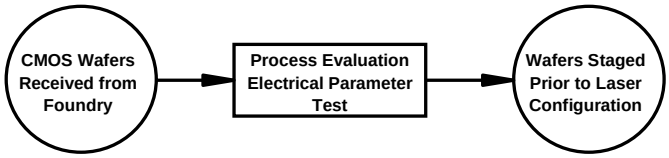
Customer Code Acceptance

Once you have designed your system and proven its operation using field programmable products, we encourage you to submit your design to Clear Logic for prototyping. Clear Logic verifies the validity of the checksum, assigns a unique Program-Specific Device Number (PDN), and adds the electronic file to our database. Within one week, we convert your FPGA design to LASIC and ship the prototype units to you for evaluation and qualification. Your design can be converted and in production in less than one month!

Key Manufacturing Process Steps

Wafer Fab Process and Incoming Inspection

Clear Logic manufactures the CL8000 family on six inch diameter, standard CMOS wafers. One layer of polysilicon and three



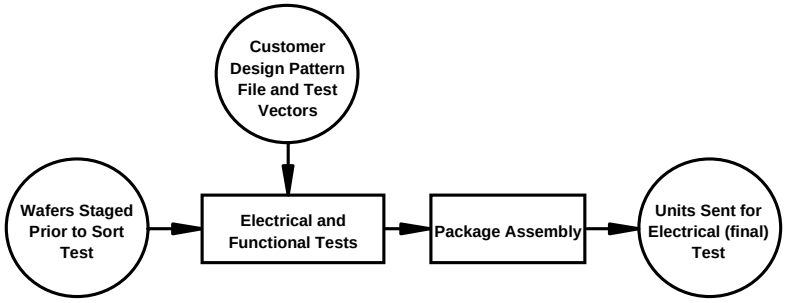
layers of metal provide the internal interconnections. The process lithography produces 0.5µm feature sizes.

Integrated Device Technology, Inc. (IDT) is our manufacturing foundry partner. IDT is a proven technology leader, producing high performance CMOS products in high volumes for its own customers.

When Clear Logic receives wafers from the foundry, we perform an incoming inspection and an electrical test to verify that the wafers have received proper processing.

Laser Configuration and Wafer Passivation

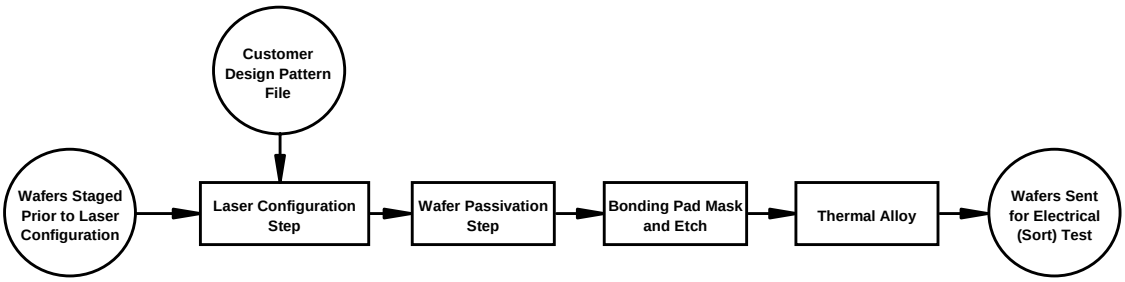
Clear Logic's unique customer benefits are possible because we use our proprietary Laser-Configured ASIC (LASIC) technology. Because laser configuration is one of the last wafer processing steps, you get the benefit of short lead times. You can place orders without a minimum quantity limit because we can configure any number of dice on the wafer to a customer design. We don't make any custom masks, so you don't pay any NRE.



Only Clear Logic has developed state of the art ClearFire™ laser technology that produces customer configured ASIC devices in high volume and on-time. Using proprietary techniques we configure tens of thousands of fuses at very high rates.

Wafer Level (Sort) Test and Assembly

After the final wafer manufacturing steps, we electrically test (wafer sort) the wafers. We test the wafers to assure correct electrical parameters and to verify the laser configuration results. The test system verifies that the correct customers' designs that we expect from laser configuration are actually on the wafer. In addition, we check the part with test vectors automatically generated from the bitstream to insure functionality of each specific customer design.

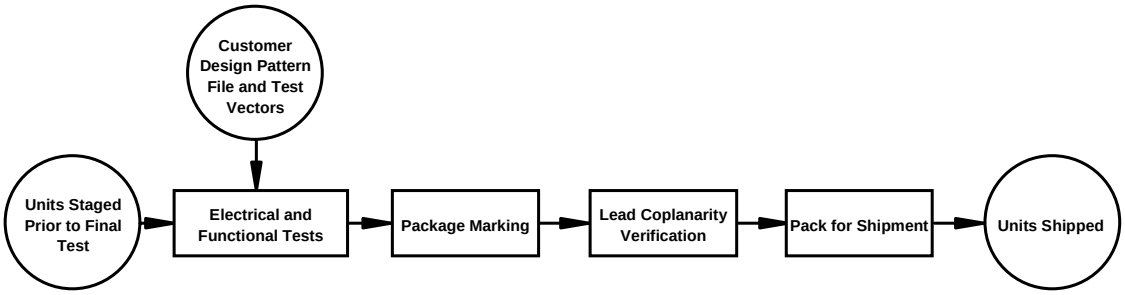


Then we ship the wafers to the assembly plant. There, they are sawed into dice, and packaged as units.

Final Test, Mark, and Ship

At final test we check the units for speed in addition to electrical and functional compliance. The testing occurs at elevated temperature, the worst case environment for speed. Again, similar to wafer sort testing, we check the units to the automatically generated test vectors. These vectors re-verify correct operation of your unique design.

Units that pass final test move to a laser marking machine to receive their part numbers and date codes. Next, we process the units next through a high speed automatic lead inspection



system. This machine guarantees optimum lead forming just prior to packing for shipment.

Our final step, of course, is to pack your units in appropriate protective materials and ship them to you!

Clear Logic Benefit Summary

- Fast Cycle Times: Development and Production
- Easy Design and Development with Altera FLEX 8000
- No Minimums
- No NRE
- Low power
- No Test Vector Development
- No Circuit Board Changes Required
- Mix and Match With FLEX 8000
- Non-Volatile Operation: No Configuration EPROM
- No Risk; Your Board Is Always Compatible With The FLEX 8000.