CL8000 Test Methodology

Introduction

Clear Logic's CL8000 family of Laser-Configured ASICs (LASICs) provide a turnkey ASIC conversion of Altera's FLEX 8000 family of Field Programmable Gate Arrays (FPGAs). Clear Logic's NoFault™ test method provides 100% stuck-at fault coverage on all conversions, while requiring no stimulus vectors from the customer. This document will outline how this fault coverage is achieved.

Background

Until now, ASIC solutions have required large investments of engineering effort and project development funds to develop test programs. Integrated Circuit Engineering Corporation (ICE) cites industry sources who, for typical ASICs, attribute 40% of engineering design time and 31% of project development cost to test. Customers needing a very high percentage of fault coverage may need to invest even more into test development.

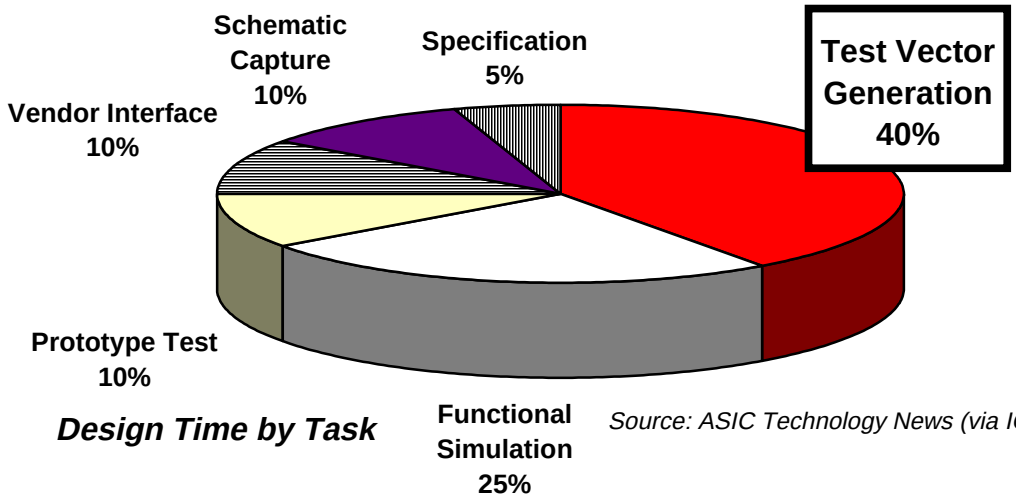


Figure 1. Test Vector Generation Represents 40% of Design Activity

Scan Chain Testing

As digital circuits have become increasingly complex, most electronics manufacturers have encountered the problems associated with testing. For integrated circuit manufacturers the problem has been that direct force and measure techniques using the device pins are not adequate for testing complex logic devices. An example is a long, complex counter. Counters implemented without testability features can require millions of cycles just to initialize the circuit to a known state. Then actually exercising the counter to verify operation in all possible states can require millions of additional test cycles. Adding internal feedback loops to already complex logic implementations can make testing from external pin connections practically impossible.

Scan testing was developed by IBM and other companies as a practical solution to the testing problem. A well known implementation is boundary scan testing of printed circuit boards as described in IEEE standard 1149.1. By placing a known value on an output pin of one device and observing the input pin of a connected device, the printed circuit board wiring can be tested for broken connections, shorts, and other circuit defects. The term "boundary scan" is used because scan registers control the I/O pins are at the boundary between the integrated circuits and the printed circuit board.

Key Elements of Internal Scan Testing

1. Break complex circuits into small testable pieces
2. Test each piece individually
3. Test the interconnects between the pieces
4. If each piece is correct and the interconnects are correct, the entire circuit will be correct

While boundary scan is most often used to verify the interconnections between ICs on a board, it can also be used to functionally test the ICs themselves. In fact, if the integrated circuits are simple enough, it is possible to use the boundary scan chain to implement a complete functional test of the printed circuit board and the ICs.

This is the approach taken by Clear Logic's NoFault test methodology, except boundary scan is replaced with internal scan, and the printed circuit board traces are replaced with the

internal routing resources of the LASIC. The integrated circuit blocks of board level testing are replaced with individual Logic Elements, IO Elements, and so forth, which are simple enough to be 100% tested using a formal mathematical model of all possible configurations of each circuit element.

LASIC Architecture Simplifies Testing

Each member of the CL8000 family is designed to receive converted designs from one member of the Altera® FLEX® 8000 product family. Each product in the family, for example the CL8452A, always contains the same architecture regardless of the customer's custom design. The customer's bitstream information is only mapped into the device, it does not modify the chip architecture. Because the chip architecture never changes for a given product, Clear Logic is able to invest the engineering effort to develop the proprietary NoFault test technology. With traditional ASIC devices the chip architecture changes with each customer implementation, making it impractical to cost effectively implement a true 100% fault coverage test solution like NoFault.

In addition to the look up table and register required for operation of each logic element (LE), Clear Logic adds three test registers that can be serially scanned through the chip I/O pins. Only special test modes activate the test registers. They are not active during normal system operation.

LASIC Scan Architecture

To guarantee 100 percent fault coverage, Clear Logic uses isolated scan design methodology. Isolated scan design means the scan registers are not part of the functional circuitry itself. The architecture of the scan design is shown in Figure 2.

NoFault test technology uses the scan registers to segment a large, complex, customer-specific logic implementation on the chip into small testable blocks. Feedback loops and connections among logic elements are disconnected while each logic element is tested. All nodes can be controlled and observed either directly or indirectly through the scan registers. This

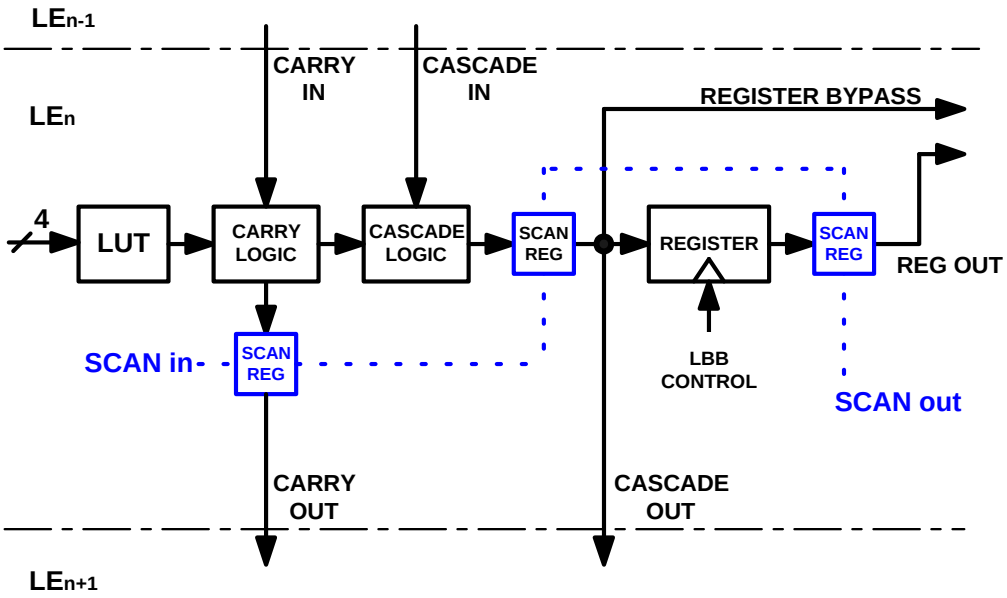


Figure 2. CL8000 Internal Scan Architecture

physically allows the detection of 100% of all stuck-at faults. In addition, the scan chain is used to test functional operation of all logic in each logic element. For example, the carry logic output in an LE can be measured directly by a scan register. The internal nodes of the four input Look Up Table (LUT) can be measured indirectly by exercising the 16 possible input combinations.

The scan registers are also used to verify connection and detect shorts in interconnects. The NoFault scan architecture has these design features that enable interconnect testing.

1. Each row interconnect line, column interconnect line, and Logic Building Block (LBB) Local Feedback line is directly controllable by a single scan register (either an LE output drive, IOE output drive, or Dedicated Input drive), because every possible drive source has a scan register and because two drive sources sre not allowed to control the same line.

2. Each Peripheral Bus Signal and LBB Control Signal is controlled by a single Row Fast Track line or Column Fast Track line (either directly or after a simple inversion). Based upon the previous design feature 1, each such signal is thus also controllable by a single scan register.

3. Scan registers are inserted in the Carry Out and Cascade Out paths between adjacent Logic Elements, giving direct control of these signals.

Taken together, these properties assure direct control of every interconnect resource in the CL8000 architecture, much as boundary scan can directly control every trace on a printed circuit board.

Automatic Test Vector Generation

The proprietary ClearShot™ bitstream extraction tool automatically decodes the customer specific bitstream in order to create the manufacturing data. Based upon the same customer-specific bitstream, Clear Logic's NoFault test generation tool automatically generates a series of scan test patterns for production testing.

Key Elements of NoFault Test Vector Generation

1. NoFault analyzes bitstream to develop an exhaustive stimulus set
2. NoFault EDA tool generates the expected response for all internal circuit nodes

NoFault automatic test generation controls the connecting and disconnecting of circuits at scan register insertion points to break the complex circuitry of the chip into blocks. In this manner, it segments complex, difficult to test logic implementations, such as long chains of counters, into simple, easily tested blocks. An example of a small testable block would be one stage of a large counter, which could be implemented in a single logic element.

Clear Logic's proprietary NoFault EDA tool identifies all of the input signals that contribute to the state of each circuit node and generates an exhaustive stimulus truth table of all possible input combinations. This is done for each node, until test vectors have been generated for all scan registers on the chip.

The first task of the automatic test generator becomes the testing of internal circuitry within each small logic block (for instance, a given Logic Element or IO Element). Figure 3 shows

a typical case. Scan Registers "A" though "N" represent scan registers somewhere on the chip which are controlling Row Interconnect lines or Column Interconnect lines. The "Logic Function" represents the logic block to be tested - perhaps a Logic Element with a Look Up Table configured to implement a given Boolean expression. The output of the Logic Element is observable at scan register "Y".

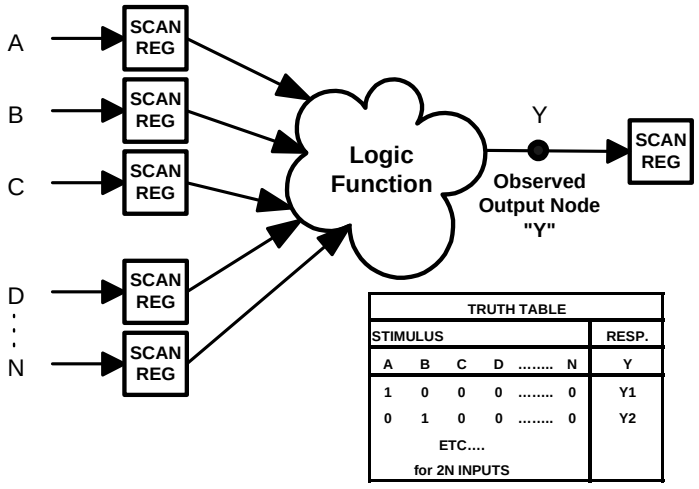


Figure 3. Testing Logic Elements

Methodology

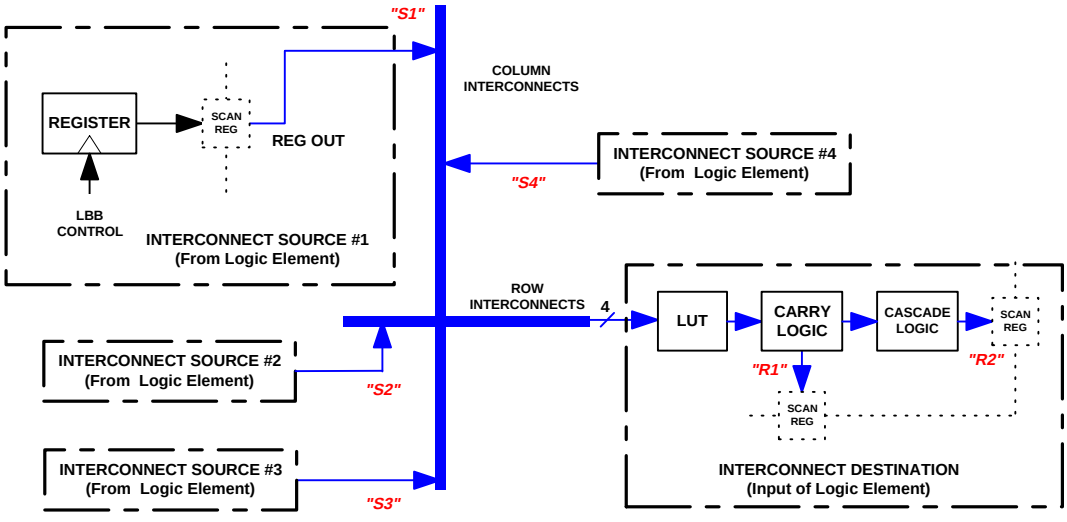
How does the NoFault process insure 100% fault coverage testing of a combinatorial circuit such as this? There are a number of complicated ways to do it, but the actual approach is attractively simple. If a combinatorial circuit has N inputs, its truth table has 2^N rows. The NoFault solution is to test all 2^N cases and not worry about finding the fewest vectors needed to catch the entire possible fault set. The NoFault automatic test pattern generator models the logic function to calculate a scan test expected response for each of the 2^N truth table input stimulus possibilities. If the functional behavior of a circuit is described by a truth table of 2^N rows, and the test confirms the proper behavior of every case in the table, then the circuit is 100% checked against stuck-at faults.

Testing all possible combinations may seem unrealistic, but it is not. Scan registers are always two or less gates apart in the chip logic. This keeps the number of inputs "N" that can influence any node to be a relatively small number.

This describes the approach as it applies to combinatorial circuits. The sequential case (circuits embedding internal feedback) is slightly more complicated, but NoFault testing takes the same approach of creating an exhaustive set of test vectors.

The engineering work of optimizing the design for test has been done by Clear Logic, instead of the customer, yielding short test times, minimum scan register area, and 100% fault coverage. This is the designed-in strength of the CL8000 family scan architecture.

Finally the NoFault scan test vectors exercise row and column interconnects to verify that intended connections exist and the interconnects are not stuck. Scan registers at the source and at the destination of each row and column interconnect allow this testing. Each source connection is forced and the destination is observed for proper function. Also, each interconnect is exercised to verify that it does not have a stuck-at fault.



"S1, S2, S3, S4" Are Stimuli From Scan Register Outputs For Interconnect Testing

"R1, R2" Are Scan Register Input Points Where Response Is Observed

Figure 4. Interconnect Testing

Testing to 100% fault coverage is complete when the logic associated with all scan register output nodes has been tested, and all interconnects have been verified.

Circuits that are on the chip but not associated with customer logic implementation are tested by other means. For example, the circuitry that emulates Altera configuration modes and JTAG boundary scan chains are tested using conventional LSI testing techniques.

Summary

Clear Logic's NoFault testing technology guarantees 100% stuck-at fault coverage. NoFault technology is an integrated scan-based approach that solves the fault coverage problem through an innovative combination of chip design for testability and automatic test vector generation. This capability allows Clear Logic to test product without requiring the customer to supply any test vectors or design support of any kind.