CL8000 LASIC Timing and Function Compatibility

Introduction

Clear Logic's CL8000 family of Laser-Configured ASIC (LASIC™) devices are fully socket-compatible with the Altera® FLEX®8000 family of Field Programmable Gate Arrays (FPGAs). Clear Logic uses an automated conversion process to produce ASIC devices that replace Altera FLEX 8000 products without any modification to the customer's design or printed circuit board. This conversion process insures that Clear Logic LASIC devices duplicate the logic function and the relative timing of the original Altera FPGA design.

Traditional ASIC vendors convert FPGA designs by migrating them to a general purpose "sea of gates" device. Because the fine-grained architecture of the ASIC is very different than the coarse-grained architecture of the FPGA, conversion is complex and painfully difficult. Clear Logic's conversion process, on the other hand, provides a "high fidelity" or exact reproduction of the FPGA design.

If the Altera device is properly designed into a system, **the corresponding Clear Logic device is guaranteed to operate correctly in the system, and the Clear Logic design will actually be more robust.**

Background

ASIC customers have been very much involved in the design and verification processes of IC development. Because ASIC manufacturers have required large NRE (nonrecurring engineering charges) and minimum purchase quantities, the cost of design mistakes has been very high, in both real money and time to market. Because of the risk, customers extensively analyze software models and timing simulations before committing to produce a silicon prototype.

Until now, FPGA to ASIC conversions have also been done this way. Since the ASIC design has traditionally been implemented in a very different chip architecture than the FPGA, the "conversion" has been actually a second, and different, design.

Customers have done logic synthesis, placement, routing and test vector development for their ASIC conversions without being able to use the constraints developed for the original FPGA designs. The financial and schedule risks associated with these conversions has been the same as any other ASIC development. So customers have taken the same precautions that they use when developing an ASIC.

The Clear Logic FPGA to LASIC conversion process is radically different. The customer first successfully implements the design in an FPGA. Then the design is moved directly to a matching LASIC device. Silicon prototypes of LASIC products are available within two weeks. Since the LASIC uses the completed FPGA design as the basis of conversion, the probability of a successful prototype is very high. With Clear Logic the prototype chip is inexpensive and can be used to qualify the LASIC. This saves a lot of engineering time that would be normally be spent evaluating simulations. In addition, system level evaluation using actual silicon allows a more accurate validation than software simulation.

GENERAL COMPATIBILITY TO ALTERA
◆ Identical Packaging, Pin Functions, and Pin Locations
◆ All Altera Special Function Circuits Emulated
◆ Conversion Preserves Run Time Function and Timing

Table 1. General Altera Compatibility

Clear Logic insures a high fidelity conversion in three ways (see Table 1).

First, CL8000 packaging, pin functions and pin locations are identical to the FLEX 8000 family. Secondly, Clear Logic exactly duplicates the behavior of special function circuitry including configuration loading, JTAG, and power-on reset. Third, the CL8000 FPGA-to-ASIC conversion process produces LASICs that preserve the logic function and relative timing that is implemented in the FPGA design.

Of the three areas of concern, timing performance has been the biggest problem for customers. Most customers with ASIC experience have been burned more frequently by timing issues than any other problem. This application note reviews the ways that Clear Logic insures timing compatibility with Altera FPGA designs. In addition, there are some suggestions for methods that may be used to qualify Clear Logic products in a system.

Because Clear Logic produces prototypes quickly and does not require NRE payments, system designers can quickly and inexpensively verify functional and timing compatibility of the LASIC device. Actual silicon is the best vehicle for comprehensive system validation. Software HDL modeling cannot simulate all real world conditions. *Just order a Clear Logic prototype and try it in the system!*

Timing Compatibility

Clear Logic has developed a new laser configured cell array chip architecture that insures the highest level of compatibility when converting an FPGA to an ASIC. Clear Logic simplifies the ASIC conversion problem by mapping each FPGA product into a Clear Logic chip that has been specifically designed to receive the conversion. For example, designs for Altera's EPF81188A map into the CL81188A.

Clear Logic's conversion technology is based on the following:

FUNCTION AND TIMING COMPATIBILITY

1. Architecture electrically and physically matches the Altera source FPGA

- **a. I/Os are matched to Altera for timing and voltage/current drive**
- **b. Internal transistors and loading are tuned for FPGA compatibility**
- **c. Critical timing parameters are better than source FPGA parameters**

2. Logic is mapped into structures that match the source FPGA design

3. Placement and routing relationships are preserved

Table 2. Insuring Function and Timing Compatibiity

First, the structure of each Clear Logic product is similar to the architecture of the corresponding Altera FLEX 8000 device. The basic element of the CL8000 family is a logic element consisting of a four input lookup table, a register, and control signals. Clear Logic constructs these elements to be exactly compatible with the FPGA. They are not synthesized from a sea of gates.

The Clear Logic CL8000 architecture is designed to insure that any routing connection available in the source FPGA can be duplicated in the laser configured architecture. The connection paths are physically similar and maintain the relative timing relationships of signals in the original FPGA design.

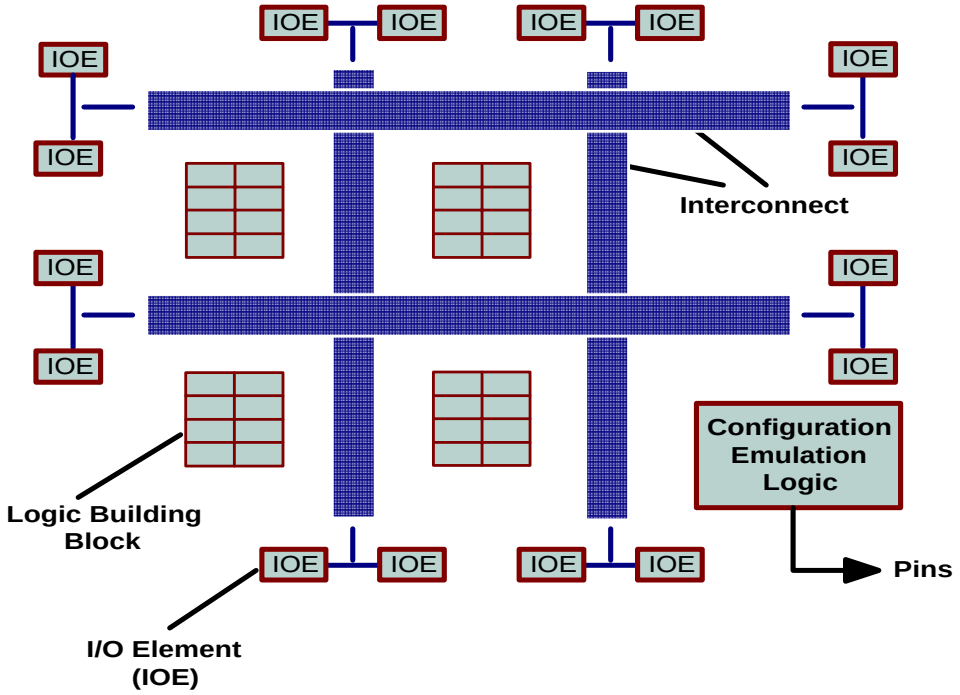

Figure 1. Clear Logic Architecture Similar to Altera FLEX

I/O elements are designed to match the timing and I-V drive characteristics of the source FPGA. Propagation delays, setup time, and hold time are better than the Altera device.

Second, the logic implementation is synthesized into structures that match the source FPGA design. For example, if an FPGA function is synthesized using five specific logic elements, it will be mapped into five logic elements, each in a physically similar location, in the Clear Logic device. Nothing is constructed from a sea of gates.

Third, Clear Logic extracts complete routing and placement information from the bitstream pattern that configures the field programmable product in the design. The ClearShot™ proprietary automated EDA tool converts the bitstream information to an electronic file used to configure the laser fuses in the CL8000 family product. The conversion technique preserves routing and placement information so that the CL8000 maintains the internal timing relationships of the FLEX 8000 implementation.

Proving Timing Compatibility

Timing compatibility is proved by determining the critical timing parameters in the FPGA. Then, testing verifies that, in the Clear Logic product, those parameters are better than in the FPGA. To insure functional operation, the timing parameters that must be compatible with the Altera device are propagation delay, setup time, and hold time.

Because exceeding specifications and actual performance for these three parameters are critical to compatibility, Clear Logic circuit designers insured that there is substantial performance margin for each parameter. Clear Logic products have more performance margin at voltage and temperature extremes. Designs implemented in Clear Logic will actually be more robust than those implemented in the source FPGA.

Propagation Delay Time:

Propagation delay time (t_{PD}) specifies the speed at which a signal travels through the device. If a signal does not propagate quickly enough through a device, it will not be available at subsequent internal logic stages when it is required.

The Clear Logic chip has approximately the same floor plan and signal routing as its Altera counterpart. However, the Clear Logic fuse structure and interconnects replace transistor switch points in the FPGA with metal to metal connections. Therefore, the Clear Logic product will have faster row and column interconnect delays (see Figure 2), resulting in better (smaller) t_{PD} specifications.

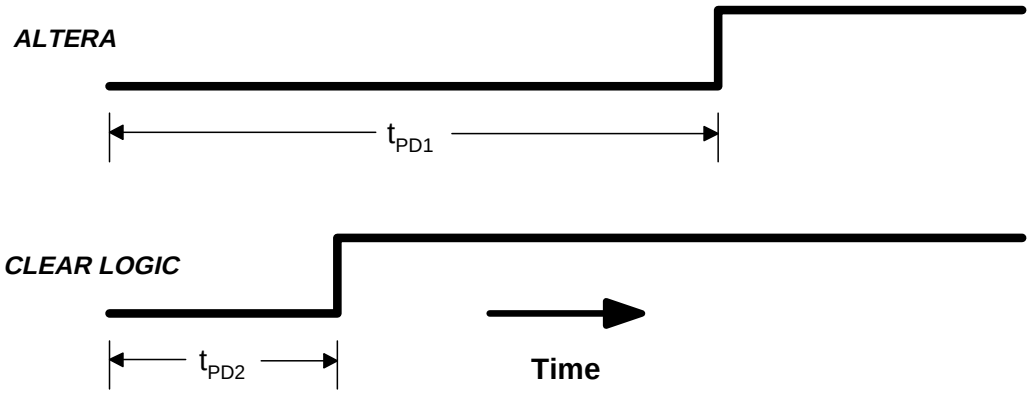

Figure 2. Clear Logic Interconnect Delay Faster Than Altera

Propagation delays are specified by Altera as maximum values with no minimum specification. The Max+Plus II software also models t_{PD} parameters as maximums with minimums that are effectively zero. Assuming that the designer has properly modeled the FPGA implementation and has not built a circuit that is somehow dependent upon minimum t_{PD}, the Clear Logic device will be proved compatible if propagation delay is measured to be less (better) than Altera.

Test Method For Propagation Delay Time:

Clear Logic measured relative propagation delay by implementing several test circuits, including a t_{DDR} test circuit (Figure 3) as described by Altera in Application Note AN76, v2, Figure 1. The t_{DDR} test circuit allows measurement of the delay caused by three logic elements in series.

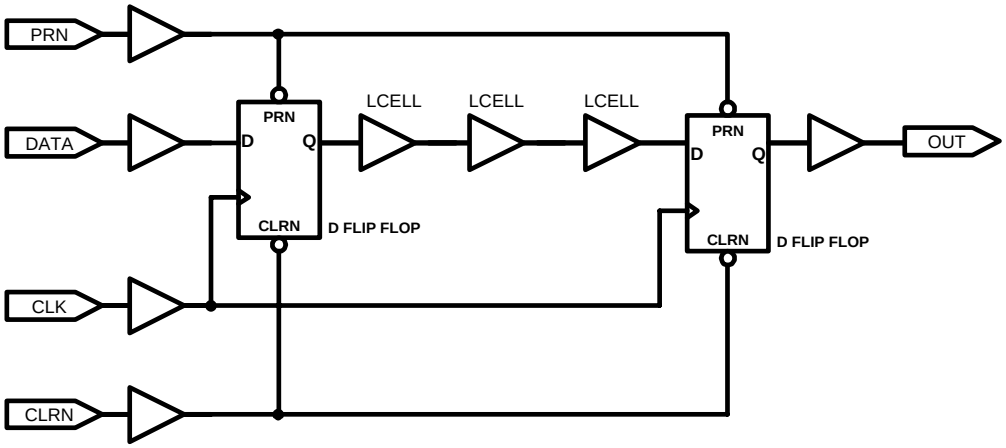

Figure 3. Propagation Delay t_{DDR} Test Circuit

	Clear Logic CL8452A-2		Altera EPF8452A-2	
Vcc volts	t_{DDR} measured nsec		t_{DDR} measured nsec	t_{DDR} specification nsec
4.50	11.0		13.7	NA
4.75	10.6		13.2	16.0
5.00	10.2		12.7	16.0
5.25	9.9		12.3	16.0
5.50	8.9		12.0	NA

T_A = 25° C

Table 3. t_{DDR} Measurement Data

The measurements in Table 3 show that Clear Logic t_{DDR} is always better than Altera t_{DDR}, both for actual performance and data sheet specifications.

Ring Oscillator Demonstrates Clear Logic Speed

As another way to check propagation delay, Clear Logic constructed a nine stage ring oscillator using logic cells. The maximum free running oscillation rate shows that Clear Logic overall propagation delay through multiple logic cells is approximately 20% faster than Altera. Both Clear Logic and Altera silicon operate much faster than the 4.25 nsec worst case delay per stage simulated using MAX+PLUS II.

	Clear Logic CL8452A-2		Altera EPF8452A-2	
Vcc volts	Delay per Stage nsec (measured)		Delay per Stage nsec (measured)	Delay per Stage nsec (MAX+PLUS II)
4.50	2.27		3.09	NA
4.75	2.20		2.93	4.25
5.00	2.14		2.82	4.25
5.25	2.06		2.76	4.25
5.50	1.99		2.68	NA

Oscillator Operating at F_{MAX} T_A = 25° C

Table 4. Nine Stage Ring Oscillator At Maximum Frequency

Setup Time:

For data to successfully propagate through the device, it must arrive in proper relationship to the pulses used to clock the data through various elements of the circuit. This is called setup time (t_{SU}).

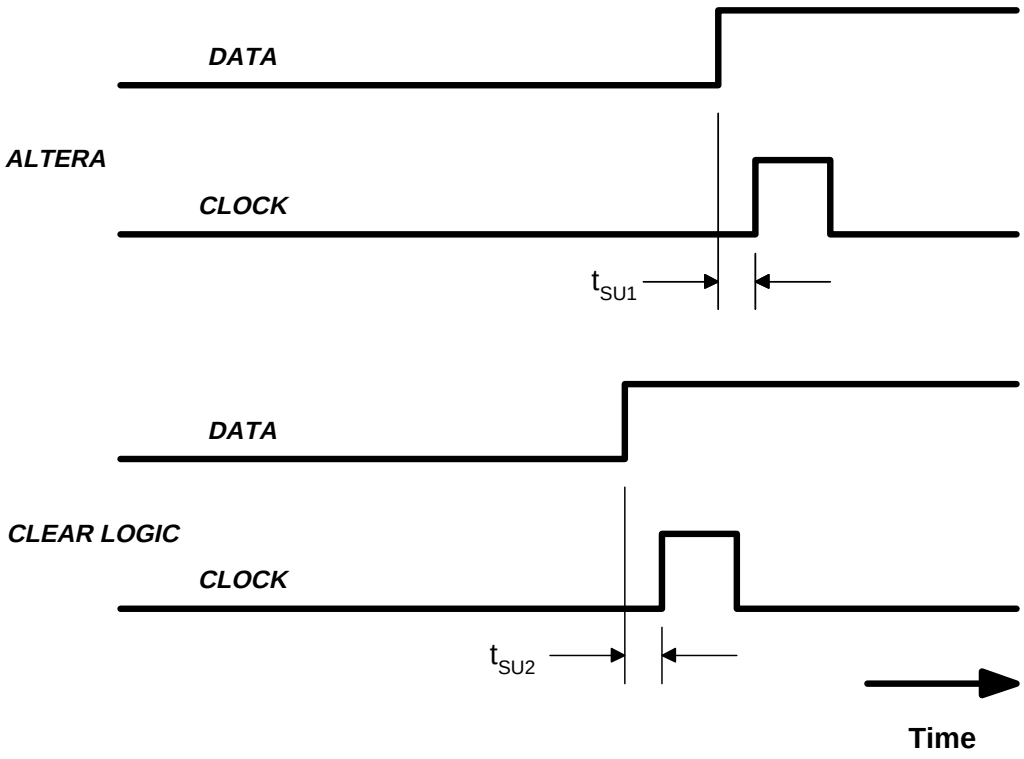

Figure 4. Set Up Time Similar For Both Clear Logic and Altera

Since the propagation delay of the clock I/O pin to a register's clock input and the delay from an input pad to a register's data input are both faster than Altera, the relative difference is little changed in the Clear Logic device. It is this relative time difference that is critical to maintaining compatibility. The actual magnitude of the delay from the pad to the internal register is not critical.

Signals that originate internally instead of from I/O pins must also satisfy setup requirements.

Description of Setup Test Methods :

In order to generate a Clear Logic test device with a configuration that can truly compare setup time to Altera products, the bitstream used to configure the test device must provide for worst case measurements.

The key goal of the testing was to develop clock and data paths that give worst case measurements. If the worst case measurements are better than Altera, Clear Logic devices will be functionally compatible.

Factors Affecting Delay From Pads To Registers

1. Dedicated inputs are routed by a large driver to every logic building block. To minimize signal propagation delay, route signals from a dedicated input pad instead of I/O pads to an internal register.

2. Physically placing and routing the clock and input pad to opposite corners of the chip achieves longer relative delay effects.

3. Load signals from input pads by connecting additional fan-ins. Make connections to multiple circuits, increasing loading effects for worst case measurement.

Maximum Setup Time Test Pattern

A register with a very short clock path and a very long data path allows a maximum setup time measurement. Using Max+Plus II, Clear Logic generated valid worst possible case designs for the Altera device. These designs are worst case for both Altera and Clear Logic because of architectural similarity.

Clear Logic placed the register and the clock at one corner of the chip. The data input is placed at the farthest corner from the clock. To minimize the clock delay, Clear Logic chose a dedicated input as the clock pin. For maximum data delay, Clear Logic chose an I/O pin and tested four loading cases. The different cases used total load fan-in of 1, 8, 15 or 22 loads.

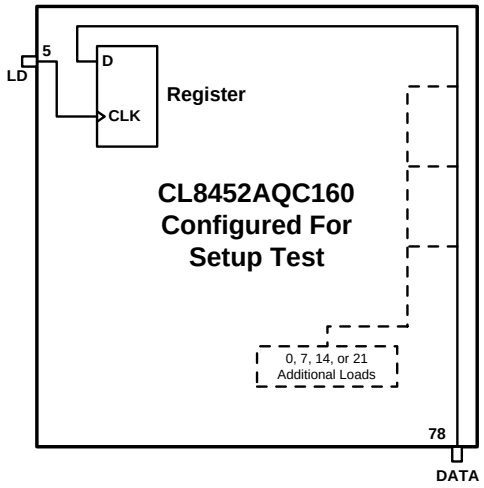

Figure 5. Configuration Used For Setup Test

Results of this test are in Table 5. They show that in all cases the setup performance of the Clear Logic devices exceeds that of Altera.

	Case A 1 load	Case B 8 loads	Case C 15 loads	Case D 22 loads
	t_{SU} nsec	t_{SU} nsec	t_{SU} nsec	t_{SU} nsec
Clear Logic CL8452AQC160-2	0.75	0.95	1.10	1.30
Altera EPF8452AQC160-2	2.30	2.50	2.55	2.75
MAX+Plus II Simulation	2.70	3.70	4.10	4.50

Vcc = 5.0V; T_A = 25° C

Table 5. Setup Time Measurement Results

Hold Time

The same discussion of relative performance that applied to setup time also applies to hold time. System functionality and timing are preserved by the Clear Logic device as long as hold time is less than the equivalent hold time parameters of Altera.

Maximum Hold Time Test Pattern

Worst case hold time occurs when the clock path is very long and the data path is very short. For this test the register and the data pin are at one corner of the chip with the clock pin placed at the farthest corner away. Using a dedicated input minimizes the data delay. To insure maximum clock delay, Clear Logic chose an I/O pin and loaded it with a total fan-in of 1, 8, 15, or 22 loads (Cases A to D).

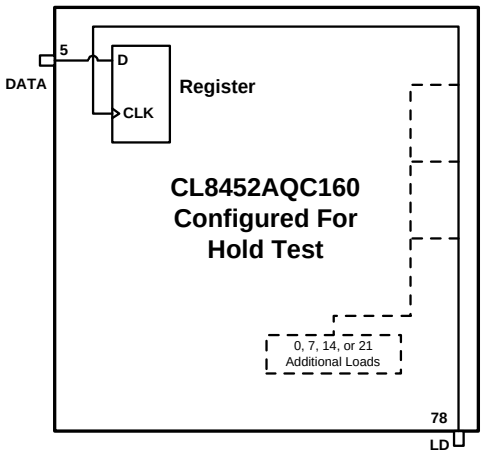

Figure 6. Configuration Used For Hold Time Test

The test data in Table 6 shows that the Clear Logic devices always have a better hold time than Altera.

	Case A 1 load	Case B 8 loads	Case C 15 loads	Case D 22 loads
	t_H nsec	t_H nsec	t_H nsec	t_H nsec
Clear Logic CL8452AQC160-2	-2.05	-1.90	-1.65	-1.40
Altera EPF8452AQC160-2	0.55	0.90	0.95	1.30
MAX+Plus II Simulation	1.50	2.80	3.20	3.50

Vcc = 5.0V; T_A = 25° C

Table 6. Hold Time Measurement Results

Results

All Clear Logic products are designed for complete Altera compatibility as previously explained in Table 1 and Table 2.

Clear Logic CL8452A critical timing parameters for propagation delay, setup time, and hold time were measured. All critical parameters are better than both the measured and specified parameters of the corresponding Altera device. In a similar manner Clear Logic verifies compatibility of all of its products.

Therefore, designs properly implemented in Altera products will also function correctly when implemented with Clear Logic.

Validation

Customers sometimes ask for recommendations for validating operation of a Clear Logic product in systems that were initially designed using Altera.

Generally, the best techniques are those used to qualify operation of standard semiconductor devices that have been designed for alternate sourcing. This is because Clear Logic products have been specifically designed to match architecture and exceed critical timing parameters of Altera, like any second source device.

Use a “four corners” test of Vcc voltage versus operating temperature to check system level functioning. See Figure 7. Checking operation slightly outside of the specified operating range adds a margin of safety to the system validation testing.

Testing actual silicon from Clear Logic is a much more accurate validation technique than the HDL modeling usually used to validate ASICs. Using a real system and real Clear Logic silicon, second order effects like system noise and ground bounce reflect the true nature of system operation.

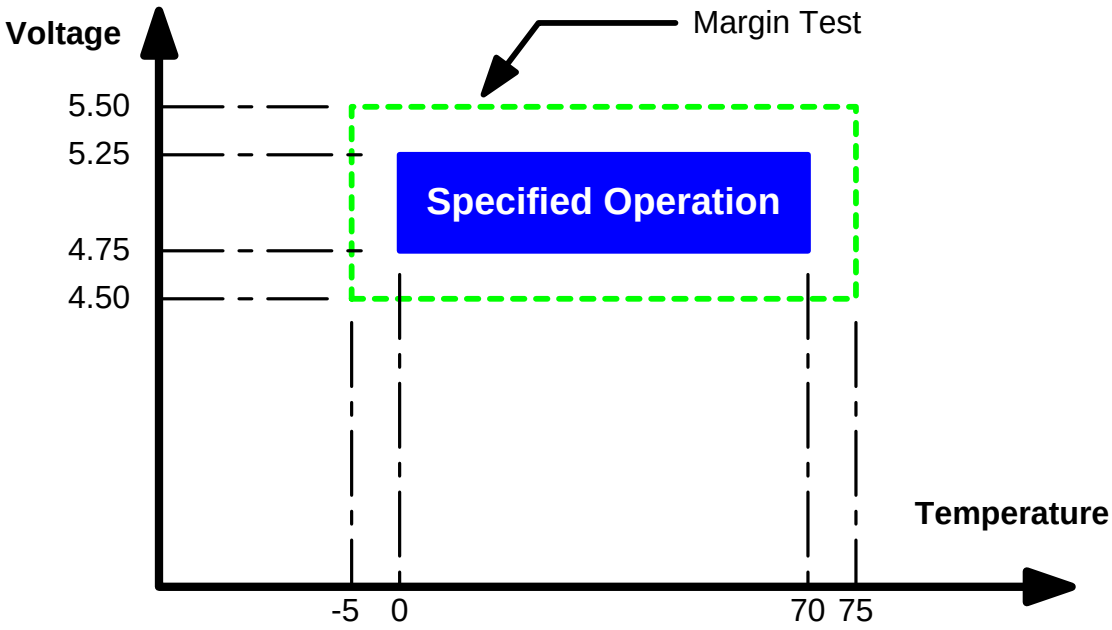

Figure 7. Four Corner System Validation Testing

Asynchronous Designs

Use synchronous techniques where possible to achieve the most robust designs. Because all propagation delays, setup times and hold times exceed Altera specifications, Clear Logic conversions are essentially guaranteed by design to work in synchronous systems. An excellent tool for finding unintended asynchronous conditions in your design is the Altera "Design Doctor."

If you cannot eliminate asynchronous situations, then be sure to allow ample timing margin where potential race conditions could occur. Remember, Altera does not guarantee minimum propagation delay. Even though a marginally designed asynchronous system may operate today with Altera products, Altera may migrate products to new technologies causing system failure.

Summary

Clear Logic products are ideal lower cost production alternatives for FPGAs in most applications. Designs that have been implemented using Altera devices transfer quickly and easily to Clear Logic. Because Clear Logic products have similar architecture to Altera, but offer better timing performance, designs will actually be more robust after the conversion.

Clear Logic charges no NRE and delivers first article prototypes in two weeks. This means that validating system operation with actual silicon can be less expensive and quicker than with HDL software simulation. In addition, silicon evaluation tests all of the real system operating parameters, not just those that can be modeled in software.

Just send us a bitstream, and we ship your prototypes in two weeks!

Notices