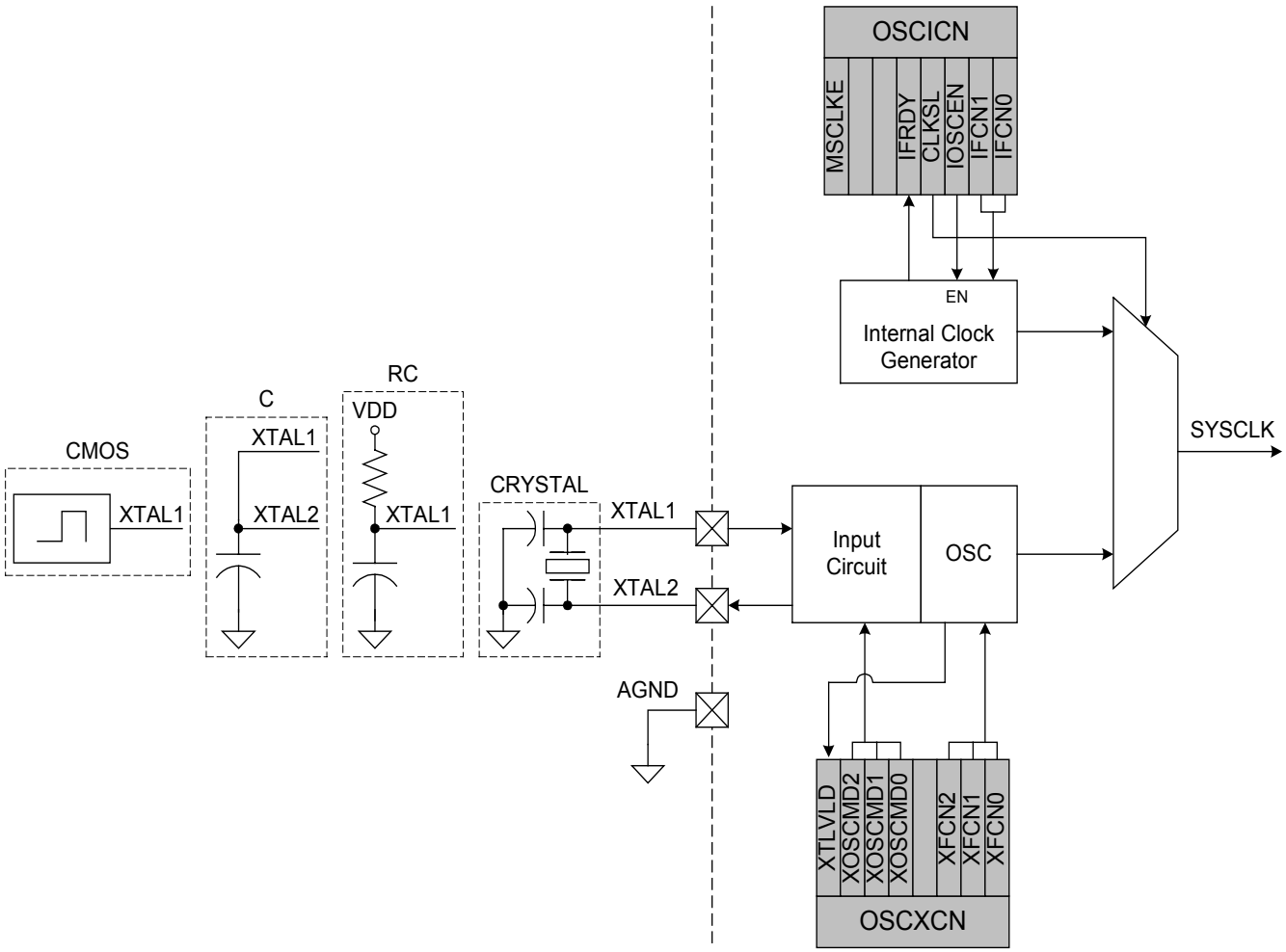

Introduction

The purpose of this application note is to describe how to configure and use the internal and external oscillators. Configuration descriptions, setup examples, and sample code are provided.

Key Points

- The internal oscillator operating at 1.9 MHz is enabled and selected automatically when the device is reset.
- The system clock can be easily switched between the internal and external oscillators.
- It is legal to select the External Oscillator as the System Clock and disable the Internal Oscillator in the same write. If running off the external oscillator, it is legal to enable the internal oscillator and select the internal oscillator as the system clock in the same write.
- It is legal to change the frequency of the internal oscillator while using the internal oscillator as the system clock.
- In all oscillator modes, /SYSCLK, a buffered version of the system clock, can be output on a port pin by enabling it in the Crossbar.
- If the Missing Clock Detector is enabled, a RESET will occur if the system clock drops below about 10 kHz.
- The Crystal Oscillator Valid flag can be used to generate an interrupt when the crystal oscillator stabilizes, allowing the interrupt handler to switch to the external oscillator.

Configuration Descriptions

In addition to being highly configurable, the oscillator is both flexible and easy to use.

The system clock can be freely switched between the internal and external oscillators. Furthermore, you can leave the external oscillator enabled while the internal oscillator is selected to avoid startup delays when the system clock is switched back to the external oscillator.

The external oscillator is highly configurable, offering many choices to the system designer. The time base can be derived from an external CMOS-level clock source, an attached crystal or ceramic resonator, an attached RC combination, or an external capacitor.

The operation of the internal and external oscillators is governed by two SFR registers, OSCICN (Internal Oscillator Control Register) and OSCXCN (External Oscillator Control Register). The descriptions for these registers are given in Figures 7 and 8 respectively.

Internal Oscillator

At reset, the internal oscillator operating at 1.9 MHz is selected as the system clock. The internal oscillator is programmable to one of four frequencies as shown in Table 1. The frequency of the internal oscillator can be changed on the fly. The frequency change takes just a few clock cycles. If the operating frequency is important to the instructions immediately following the oscillator change, IFRDY (Internal Oscillator Frequency Ready flag, OSCICN.4) can be polled.

The power consumption of the internal oscillator itself is independent of the selected frequency; however, the power consumption of the entire device is frequency dependent.

The accuracy of the internal oscillator is ± 20 % across process, power supply, and temperature variations.

External CMOS Clock

The system clock can be supplied from an external CMOS-level clock source tied to the XTAL1 pin, such as a crystal oscillator module or the clock signal from another microcontroller.

External Crystal

In general, a crystal is called for when an accurate time base is needed, for example when the absolute sampling rate of the ADC is critical or a standard UART baud rate must be generated. Alternately, a low-frequency tuning-fork crystal, e.g. a 32.768 kHz watch crystal, can be used to operate the device in a low-power mode, then control can be switched to the high-frequency internal oscillator as required by the system.

The accuracy and stability of the crystal oscillator is governed almost exclusively by the attached crystal or ceramic resonator, provided that the loading capacitance parameters and oscillator drive level are set appropriately.

External RC

Alternately, the time base can be derived from an external series RC combination. In this configuration, the capacitor is charged through the supplied resistor until the voltage at XTAL1 reaches (⅓)*AV+, at which time XTAL1 is driven to ground, discharging the cap. This operation produces a saw-tooth type waveform at XTAL1 whose period is dominated by the rise time of the voltage across the cap; the discharge time is less than 10 ns for a 100 pF capacitor. This signal is buffered and fed to a divide-by-two stage, the output of which becomes the system clock.

The accuracy of the time base in external RC mode is dominated by the tolerances of the R and C components.

External C

This mode is similar in operation to the external RC mode above, except that in this mode the charging current for the capacitor is supplied by an internal programmable current source at XTAL2. This is the least accurate time base mode; it is also the most flexible in that a single component value provides up to eight different operating frequencies, the highest frequency being almost a factor of 3000 greater than

Table 1. Internal Oscillator Frequency Select

IFCN[1:0]	Nominal Frequency
00	1.9 MHz
01	3.8 MHz
10	7.5 MHz
11	15 MHz

the lowest frequency.

The accuracy of the time base in external C mode is dominated by the tolerance on the capacitor and the accuracy of the internal current source at XTAL2. The accuracy of the internal current source is on the order of ± 30 % across process, power supply, and temperature variations.

Configuration Examples

Below are some example oscillator configurations.

Internal Oscillator

At reset, the internal oscillator operating at 1.9 MHz is selected as the system clock.

If the system design uses the internal oscillator exclusively and does not use the external oscillator, the XTAL1 pin should be grounded externally as shown in Figure 1, or grounded internally by setting the XOSCMD bits (OSCXCN.6-4) to '000'. If the system calls for having the /RST line of the part held low for long periods of time, then grounding XTAL1 externally is recommended.

The IFCN bits (OSCICN.1-0) program the internal oscillator frequency. Four frequencies are selectable as shown in Table 1.

After the oscillator frequency has been changed, the IFRDY (Internal Oscillator Frequency Ready, OSCICN.4) flag will go low to indicate that the frequency of the oscillator has not yet reached its programmed value. Once the oscillator stabilizes at its newly programmed frequency, IFRDY will go high.

The startup time for the internal oscillator is nearly instantaneous.

The frequency of the internal oscillator can be changed arbitrarily at will. Furthermore, the internal oscillator stabilizes at its newly programmed frequency in a couple of clock cycles. Therefore, IFRDY polling is not required unless the absolute frequency is important to the application.

External Oscillator

The device supports four different external oscillator configurations: external CMOS driver, external crystal or ceramic resonator, external RC network, and external capacitor. To enable the external oscillator, first configure OSCXCN, the External Oscillator Configuration register to the appropriate value, then set CLKSL to '1' (OSCICN.3) to select the external oscillator as the system clock.

In crystal-based designs, because the start-up time of the crystal oscillator can take milliseconds, it is necessary to wait for XTLVLD (Crystal Oscillator Valid flag, OSCXCN.7) to go high, indicating the external oscillator has stabilized, before setting CLKSL to '1'.

In external RC and external C modes, the startup time of the external oscillator is instantaneous.

External CMOS Driver

The master clock can be supplied from an external CMOS-level source tied to the XTAL1 input. In this configuration, XTAL2 should be left floating, as shown in Figure 2. Additionally, the XOSCMD bits should be set to '010' to use the incoming frequency as-is, or '011' to enable the divide-by-two stage.

Note: unlike the Port I/O pins, the XTAL1 and XTAL2 pins are NOT 5-V tolerant. The voltage at XTAL1

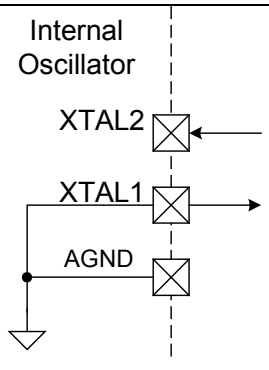

Figure 1. Internal Oscillator Connection

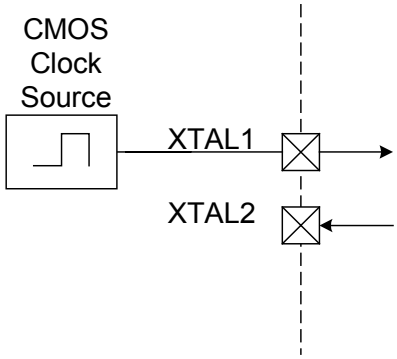

Figure 2. External CMOS Clock Connection

should be kept between AV+ and AGND.

Note: the XTLVLD flag can be used to detect an external CMOS oscillator if XOSCMD is set to '1xx'.

External Crystal

The master clock can be derived from a crystal or ceramic resonator connected across the XTAL1 and XTAL2 pins. Configuration requires setting XOSCMD to '110' to use the crystal frequency as-is, or '111' to enable the divide-by-two stage, and setting XFCN based on the crystal frequency, effective loading capacitance, and crystal Effective Series Resistance (ESR), as described below. Figure 3 shows the system configuration for an external crystal.

Note that the loading capacitors should be tied to the analog ground plane. Also note that the feedback resistor for the crystal oscillator inverter is supplied on-chip, making an external resistor unnecessary.

The XTLVLD (Crystal Oscillator Valid) bit in OSCXCN should be polled (or used to generate an interrupt) when the crystal oscillator frequency has stabilized. Once XTLVLD has gone high, CLKSL (OSCICN.3) can be set to '1' to use the external oscillator as the system clock.

Determining XFCN

XFCN controls the drive level of the crystal oscillator driver. In essence, the drive level should be strong enough to excite the crystal to oscillation, but not so strong as to stress the crystal to cause it to degrade prematurely.

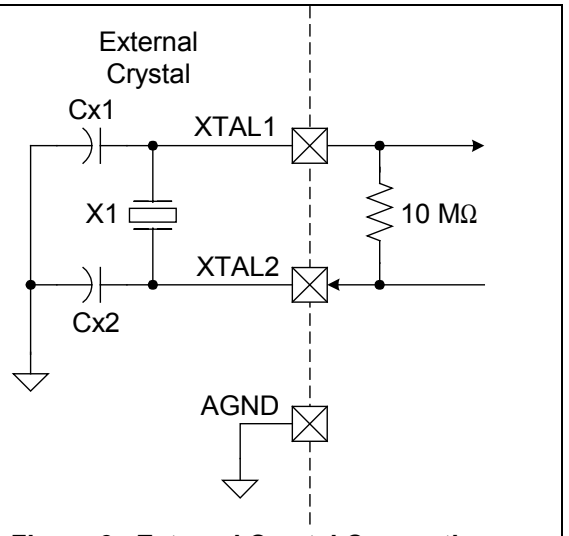

Figure 3. External Crystal Connection

For 3 MHz crystals and above, degradation based on an XFCN setting that is too high is typically not an issue, and the maximum XFCN value can be used, though this will result in a higher operating current for the oscillator. For low-frequency tuning-fork crystals, 32.768 kHz and 100 kHz for example, overdriving the crystal does present a reliability concern. Additionally, if the drive level is too high, the tuning-fork crystals may not oscillate at all.

If the design uses a normal quartz crystal with a specified loading capacitance near 20 pF, Table 2's "Approx Freq" column can be used to quickly determine XFCN. This column also applies to low-frequency tuning-fork crystals and most ceramic resonators. Alternately, the Power Factor can be calculated explicitly as demonstrated in the examples below.

Equation 1 gives the Power Factor (PF) required to excite the crystal to oscillation.

Equation 1. Power Factor

$$PF = 5 * ESR * f^2 * C_L^2,$$

Where:
PF = Power Factor,
ESR = Effective Series Resistance of crystal (or ceramic resonator) **in Ohms**,
f = crystal frequency **in MHz**
C_L = effective loading capacitance **in pF**.

The ESR can be found from the data sheet for the crystal. The frequency is a known based on the crystal selected. The effective loading capacitance must be calculated, as shown in Equation 2 below.

Table 2. Power Factor vs. XFCN (Crystal mode)

XFCN	Power Factor	Approx Freq (*)
000	90 (10^3)	15 kHz – 400 kHz
001	280 (10^3)	400 kHz – 1 MHz
010	810 (10^3)	1 MHz – 2 MHz
011	2.30 (10^6)	2 MHz – 4 MHz
100	6.30 (10^6)	4 MHz – 6 MHz
101	20.4 (10^6)	6 MHz – 12 MHz
110	36.6 (10^6)	12 MHz – 20 MHz
111	110 (10^6)	20 MHz – 30 MHz

* For a crystal specified with 20 pF load capacitance

The effective loading capacitance is a measure of the total capacitance seen between the XTAL1 and XTAL2 pins. The primary contributors to this capacitance are the crystal's shunt capacitance (called 'Co' in most crystal data sheets), the external added load capacitors (Cx1 and Cx2), and the parasitic capacitance of the circuit board traces and device pins (Cp1 and Cp2). See Figure 4.

Looking from the perspective of the XTAL1 and XTAL2 pins, Co is in parallel with the series combination of Cx1 and Cx2 and also in parallel with the series combination of Cp1 and Cp2. Assuming that Cx1=Cx2 (which is usually the case in crystal designs) and Cp1 = Cp2 (which is the case if the PCB traces are of similar length and shape), we have:

Equation 2. Loading Capacitance

$$C_L = ½ * (Cx1 + Cp1) + Co$$

Where:
CL = the total loading capacitance in pF,
Cx1 = the value of one of the external added capacitors in pF,
Cp1 = the value of one of the parasitic capacitors in pF, and
Co = the value of the shunt capacitance of the crystal in pF.

For short traces, Cp is typically 2 to 5 pF.

We illustrate calculating PF with a few examples:

Crystal Example: 11.0592 MHz

We start with an 11.0592 MHz crystal from ECS (ECS p/n: ECS-110.5-20-1, http://www.ecsxtal.com). The data sheet for this device specifies that the maximum ESR is 30 Ω, and the shunt capacitance is 7.0 pF.

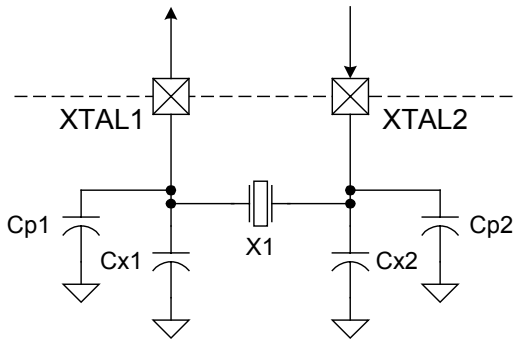

Figure 4. Load Capacitance Diagram

This crystal is specified to operate with a load capacitance of 20 pF. This "load capacitance" is defined as the total capacitance seen across the crystal's terminals, and does not include the crystal's shunt capacitance. Assuming that the total stray capacitance across the crystal terminals is 3 pF (Cp1 and Cp2 are 6 pF each), then Cx1 and Cx2 need to be (20 – 3) * 2 ~ 33 pF each.

To obtain C_L for the Power Factor equation, we add in the crystal's shunt capacitance:

$$C_L = ½ * (6 + 33) + 7 ~ 27 \text{ pF}$$

The equation for the power factor becomes:

$$PF = 5 * 30\ \Omega * (11.0592)^2 * (27)^2 = 13 * 10^6$$

The goal is to set XFCN to the smallest power factor that is at least as big as the equation above dictates. Of the two closest values we find in Table 2, 6.30E+6 and 20.4E+6, we choose 20.4E+6, resulting in an XFCN value of '101'.

Crystal Example: 32.768 kHz

The crystal oscillator driver is capable of driving low-frequency tuning-fork crystals for low-power applications. In this example, we use a 32.768 kHz watch crystal from ECS (ECS p/n: ECS-.327-12.5-8). The data sheet specifies that the ESR is 35 kΩ, the rated load capacitance is 12.5 pF, and the shunt capacitance is 1.6 pF. We again assume 3 pF of stray loading capacitance.

$$C_L = ½ * (6 + 18) + 1.6 ~ 14 \text{ pF}$$

The equation for the power factor becomes:

$$PF = 5 * 35000\ \Omega * (0.032768)^2 * (14)^2 ~ 36.8 * 10^3$$

From Table 2, we find that a power factor of $90 * 10^3$ is sufficient, resulting in an XFCN value of '000'.

Crystal Example: 20.00 MHz

Using a 20 MHz crystal with an ESR of 30 Ω, specified loading capacitance of 20 pF, and shunt capacitance of 5.0 pF, we have:

$$C_L = ½ * (6 + 33) + 5 ~ 25 \text{ pF}$$

$$PF = 5 * 30\ \Omega * (20)^2 * (25)^2 = 37.5 * 10^6$$

From Table 2, XFCN for this power factor is '111'.

External RC Network

Figure 5 shows the connection diagram for external RC mode. Note that the series RC connection is made between the analog power supply and the analog ground.

Equation 3 gives the frequency of oscillation in RC mode.

Equation 3. Oscillation Frequency in RC Mode

$$Fosc = (1.23 * 10^3) / (R * C)$$

Where:
Fosc = the frequency of oscillation **in MHz**,
R = the value of the charging resistor **in kΩ**, and
C = the value of the capacitor including stray capacitance **in pF**.

To configure the device for RC mode, XOSCMD must be set to '100' or '101'. An internal divide-by-two stage is always enabled. This divide-by-two stage is accounted for in Equation 3. Furthermore, XFCN must be set to a value high enough to support the selected frequency. Table 3 lists XFCN values vs. required frequency.

XFCN can always be set to a number higher than indicated in Table 3, but will result in a higher operating current for the oscillator. If XFCN is set too low, the oscillator frequency will be lower than predicted by the above equation, and spurious clock pulses may result.

Note: the startup time for the external oscillator in RC mode is nearly instantaneous. The XTLVLD flag is undefined in this mode.

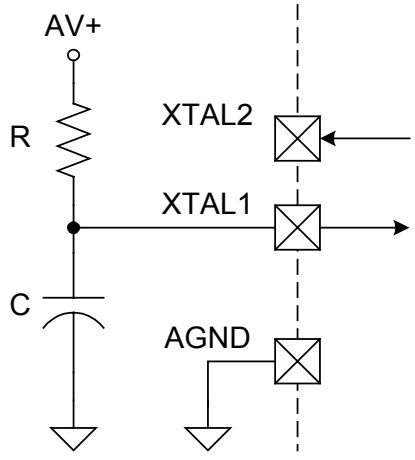

Figure 5. External RC Connection

The supplied capacitor should be between 10 pF and 100 pF, keeping in mind that at lower capacitance values the parasitic capacitance will have a greater impact on the final frequency. We illustrate with a few examples:

RC Example: 100 kHz

We start with C = 33 pF. The total capacitance including stray capacitance is 33 + 6, or 39 pF.

Assuming we want a frequency of oscillation of 100 kHz, we solve Equation 3 to find R:

$$FOSC = (1.23 * 10^3) / (R * C)$$

$$R = (1.23 * 10^3) / (FOSC * C)$$

$$R = (1.23 * 10^3) / (0.1 * 39)$$

$$R = 315\ k\Omega$$

From Table 3, we also need to set XFCN to at least '010'.

RC Example: 3.2 MHz

It is possible to operate the external oscillator in RC mode at frequencies greater than 3.2 MHz, but this practice is not recommended. There will be a significant deviation of the oscillation frequency from the equation-predicted value as the frequency increases. Specifically, the actual frequency of oscillation will tend to be lower than the predicted value due to fixed internal delays, which become appreciable as the oscillation period decreases.

Using a 33 pF capacitor which results in a total capacitance of 39 pF, we solve Equation 3 to find R:

$$FOSC = (1.23 * 10^3) / (R * C)$$

Table 3. Frequency vs. XFCN (RC mode)

XFCN	Frequency
000	Fosc < 25 kHz
001	25 kHz < Fosc < 50 kHz
010	50 kHz < Fosc < 100 kHz
011	100 kHz < Fosc < 200 kHz
100	200 kHz < Fosc < 400 kHz
101	400 kHz < Fosc < 800 kHz
110	800 kHz < Fosc < 1.6 MHz
111	1.6 MHz < Fosc < 3.2 MHz

$$R = (1.23 * 10^3) / (FOSC * C)$$

$$R = (1.23 * 10^3) / (\mathbf{3.2} * 39)$$

$$R = 9.86\ k\Omega$$

From Table 3, we set XFCN to a value of '111'.

RC Example: 1 kHz

If A/D converter performance is not critical, the system clock frequency can be made arbitrarily slow, provided that the missing clock detector is disabled (MSCLKE = '0', OSCICN.7, which is its reset state). If the missing clock detector is enabled, it will generate a system RESET if the system clock falls below about 10 kHz.

In this example, we use a C value of 100 pF, resulting in a total capacitance of 106 pF. Solving Equation 3 for R:

$$FOSC = (1.23 * 10^3) / (R * C)$$
$$R = (1.23 * 10^3) / (FOSC * C)$$
$$R = (1.23 * 10^3) / (\mathbf{0.001} * \mathbf{106})$$

$$R = 11.6\ M\Omega$$

From Table 3, XFCN can be set to '000'.

External Capacitor

Figure 6 shows the connections for external C mode. Note that the XTAL1 and XTAL2 pins are tied together, and that the supplied capacitor is tied between the XTAL pins and the analog ground plane.

Equation 4 gives the frequency of oscillation in external C mode.

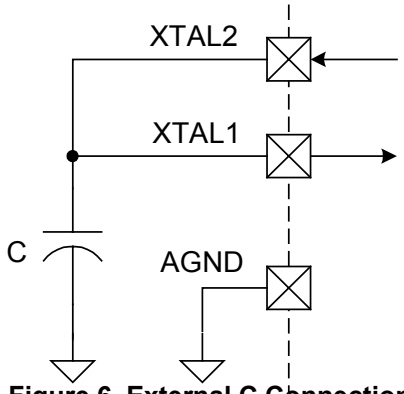

Figure 6. External C Connection

Equation 4. Oscillation Frequency in C Mode

$$Fosc = KF / (C * AV+)$$

Where:
Fosc = the oscillation frequency **in MHz**,
KF = the 'K Factor', a unit-less quantity derived from Table 4,
C = the capacitance value including parasitic capacitance **in pF**, and
AV+ = the analog power supply voltage at the AV+ pins in Volts.

Table 4 lists K Factor vs. XFCN setting.

External C mode is similar in operation to external RC mode, except that the charging current for the capacitor is supplied by a programmable current source at XTAL2. The supplied capacitor should be between 10 pF and 100 pF, keeping in mind that at lower capacitance values the parasitic capacitance will have a greater impact on the final frequency.

The actual frequency of oscillation is difficult to predict due to capacitor tolerance, parasitic capacitance, and the variance of the internal current source, which is about ± 30 %.

Note: the startup time for the external oscillator in C mode is nearly instantaneous. The XTLVLD flag is undefined in this mode.

We illustrate external C mode with some examples:

C Example: 100 kHz

Assuming a 3.0V analog power supply and a 33 pF external cap which results in a total capacitance of 39 pF adding parasitic capacitance, we solve Equation 4 for KF:

$$KF = Fosc * (C * AV+)$$
$$KF = 0.1 * (39 * 3)$$

Table 4. KF vs. XFCN (C mode)

XFCN	KF (K Factor)
000	0.74
001	2.4
010	7.1
011	21
100	61
101	230
110	770
111	2100

KF = 11.7

Referencing Table 4, the closest KF value is 7.1, which would result in an oscillation frequency of about 60 kHz. We can decrease our capacitance by a factor of 1.65 to 18 pF (24 pF total) to achieve 99 kHz. We set XFCN to '010' to select a KF value of 7.1.

Adjacent XFCN values result in K Factors which are about a factor of three apart. For example, increasing XFCN to '011' in the above example would result in an increase in the oscillation frequency from 100 kHz to about 300 kHz.

Setting XFCN to its highest value '111', results in a KF of 2100. Using this setting with the above capacitance results in a frequency of oscillation of about 30 MHz as predicted by Equation 4. As in the external RC mode, the equations are accurate for frequencies that are 3 MHz and below, and become less accurate as the frequency increases.

C Example: 3 MHz

Using the above external capacitor of 18 pF (24 pF total) and 3.0 V AV+, we solve Equation 4 for KF:

KF = Fosc * (C * AV+)
KF = 3 * (24 * 3)
KF = 216

The closest KF in Table 4 is 230, with XFCN = '101'. This results in a frequency of oscillation of about 3.2 MHz.

Oscillator Register Definitions

Figure 7. OSCICN: Internal Oscillator Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
MSCLKE	-	-	IFRDY	CLKSL	IOSCEN	IFCN1	IFCN0	00000100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB2

Bit7: MSCLKE: Missing Clock Enable Bit
0: Missing Clock Detector Disabled
1: Missing Clock Detector Enabled; triggers a reset if a missing clock is detected
Bits6-5: UNUSED. Read = 00b, Write = don't care
Bit4: IFRDY: Internal Oscillator Frequency Ready Flag
0: Internal Oscillator Frequency not running at speed specified by the IFCN bits.
1: Internal Oscillator Frequency running at speed specified by the IFCN bits.
Bit3: CLKSL: System Clock Source Select Bit
0: Uses Internal Oscillator as System Clock.
1: Uses External Oscillator as System Clock.
Bit2: IOSCEN: Internal Oscillator Enable Bit
0: Internal Oscillator Disabled
1: Internal Oscillator Enabled
Bits1-0: IFCN1-0: Internal Oscillator Frequency Control Bits
00: Internal Oscillator typical frequency is 1.9MHz.
01: Internal Oscillator typical frequency is 3.8MHz.
10: Internal Oscillator typical frequency is 7.5MHz.
11: Internal Oscillator typical frequency is 15MHz.

Figure 8. OSCXCN: External Oscillator Control Register

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
XTLVLD	XOSCMD2	XOSCMD1	XOSCMD0	-	XFCN2	XFCN1	XFCN0	00110000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB1

Bit7: XTLVLD: Crystal Oscillator Valid Flag
(Valid only when XOSCMD = 11x.)
0: Crystal Oscillator is unused or not yet stable
1: Crystal Oscillator is running and stable

Bits6-4: XOSCMD2-0: External Oscillator Mode Bits
00x: Off. XTAL1 pin is grounded internally.
010: System Clock from External CMOS Clock on XTAL1 pin.
011: System Clock from External CMOS Clock on XTAL1 pin divided by 2.
10x: RC/C Oscillator Mode with divide by 2 stage.
110: Crystal Oscillator Mode
111: Crystal Oscillator Mode with divide by 2 stage.

Bit3: RESERVED. Read = undefined, Write = don't care

Bits2-0: XFCN2-0: External Oscillator Frequency Control Bits
000-111: see table below

XFCN	Crystal (XOSCMD = 11x)	RC (XOSCMD = 10x)	C (XOSCMD = 10x)
000	Power Factor = 90 (10^3)	$f \leq 25kHz$	K Factor = 0.741
001	Power Factor = 280 (10^3)	$25kHz < f \leq 50kHz$	K Factor = 2.36
010	Power Factor = 810 (10^3)	$50kHz < f \leq 100kHz$	K Factor = 7.10
011	Power Factor = 2.30 (10^6)	$100kHz < f \leq 200kHz$	K Factor = 21.0
100	Power Factor = 6.30 (10^6)	$200kHz < f \leq 400kHz$	K Factor = 60.8
101	Power Factor = 20.4 (10^6)	$400kHz < f \leq 800kHz$	K Factor = 225
110	Power Factor = 36.6 (10^6)	$800kHz < f \leq 1.6MHz$	K Factor = 773
111	Power Factor = 110 (10^6)	$1.6MHz < f \leq 3.2MHz$	K Factor = 2141

CRYSTAL MODE (XOSCMD = 11x)
Choose smallest Power Factor (PF) such that:
$PF > 5 * ESR * f^2 * C_L^2$, where
ESR = crystal equivalent series resistance in ohms
f = crystal frequency in MHz
C_L = load capacitance in pF (crystal capacitance, parasitic, compensation network)

RC MODE (XOSCMD = 10x)
Choose oscillation frequency range where:
$f = 1.23(10^3) / (R * C)$, where
f = frequency of oscillation in MHz
C = capacitor value in pF
R = Pull-up resistor value in kΩ

C MODE (XOSCMD = 10x)
Choose K Factor (KF) for the oscillation frequency desired:
f = KF / (C * AV+), where
f = frequency of oscillation in MHz
C = capacitor value on XTAL1, XTAL2 pins in pF
AV+ = Analog Power Supply on MCU in volts

Software Example

```
;-------------------------------------------------------------------------
;     CYGNAL INTEGRATED PRODUCTS, INC.
;
;
;     FILE NAME   : cryosc.ASM
;     TARGET MCU  : C8051F000
;     DESCRIPTION : Example source code for configuring the external oscillator
;                   to use an external 11.0592MHz crystal, using XTLVLD interrupt
;                   to change from internal osc to external osc.  Also shows how
;                   to change internal osc frequency to 15MHz from the default of
;                   1.9MHz and to poll IFRDY (Internal Oscillator Frequency Ready,
;                   OSCICN.4) to wait until the internal osc. has stabilized at
;                   its programmed value.
;
; IMPLEMENTATION NOTES:
;
;
;-------------------------------------------------------------------------

;-------------------------------------------------------------------------
; EQUATES
;-------------------------------------------------------------------------

$MOD8F000

;-------------------------------------------------------------------------
; VARIABLES
;-------------------------------------------------------------------------

DSEG

;--------------------
; STACK

            org   0e8h  ; temporary forced STACK location (rev A,B errata)

STACK_TOP:  DS    1     ; placeholder in symbol table for beginning
                        ;  of hardware stack

;-------------------------------------------------------------------------
; MACRO DEFINITIONS
;-------------------------------------------------------------------------

;-------------------------------------------------------------------------
; RESET AND INTERRUPT VECTOR TABLE
;-------------------------------------------------------------------------

CSEG
            org   00h
            ljmp  Reset

            org   0abh
            ljmp  XTLVLD_ISR        ; Crystal OSC Valid interrupt
```

```
;-------------------------------------------------------------------------------
; INTERRUPT VECTORS
;-------------------------------------------------------------------------------
; Reset Vector

            org   0b3h

Reset:
            mov   WDTCN, #0deh            ; disable watchdog timer
            mov   WDTCN, #0adh
            mov   OSCXCN, #01100101b      ; Enable Crystal osc., divide by 1 mode
                                          ;  XFCN = '101' for 11.0592 MHz crystal
                                          ;  External oscillator will be selected
                                          ;  via the XTLVLD interrupt handler
                                          ;  once the crystal osc. has started
                                          ;  and settled (several hundred
                                          ;  microseconds from now).

            orl   OSCICN, #00000011b      ; enable internal osc at 15MHz
osc_wait:
            mov   a, OSCICN               ; wait for new freq to be valid
            jnb   acc.4, osc_wait         ;  Note: polling is only necessary if the
                                          ;  absolute frequency is important to the
                                          ;  following instructions. It isn't in
                                          ;  this case; we show it as an example
                                          ;  only. The frequency change will take
                                          ;  place in just a few clock cycles.

            orl   EIE2, #10000000b        ; set EXVLD (XTLVLD interrupt enable)
            anl   EIP2, #NOT(10000000b)   ; XTLVLD is a LOW priority interrupt

            mov   SP, #STACK_TOP          ; init stack pointer to end of allocated
                                          ;  RAM

            setb  EA                      ; enable GLOBAL interrupts

            ljmp  Main

;-------------------------------------------------------------------------------
; XTLVLD Interrupt Vector
;
; LOW priority interrupt
;
; This ISR is called when the external crystal oscillator valid flag has been set.
;  It switches osc. control to the external oscillator then explicitly disables
;  the XTLVLD interrupt (because there is no interrupt flag and the XTLVLD bit
;  is not writable).  It also enables the missing clock detector, which will
;  issue a RESET if the oscillator stops for any reason.
;
XTLVLD_ISR:
            orl   OSCICN, #00001000b      ; Select external osc. as
                                          ;  system clock source
            anl   OSCICN, #NOT(00000100b) ; Disable internal oscillator
            orl   OSCICN, #10000000b      ; Enable missing clock detector
                                          ;  this must be done AFTER
                                          ;  selecting ext osc as system
                                          ;  clock source if the crystal
```

```
                                        ;  is less than 70 kHz.

            anl   EIE2, #NOT(10000000b)   ; Disable XTLVLD interrupts

            reti

;-------------------------------------------------------------------------------
; MAIN PROGRAM CODE
;-------------------------------------------------------------------------------

Main:
            jmp   $                       ; Do nothing forever…

;-------------------------------------------------------------------------------
; END
;-------------------------------------------------------------------------------

END
```