MILITARY iFX8160
FLEXlogic FPGA WITH SRAM OPTION

- High Performance FPGA (Field Programmable Gate Array)
  - — Deterministic 12 ns Pin-to-Pin Propagation Delays
  - — 66 MHz System Clock Frequency
- 160 Complex Macrocells (7,000 Maximum Logic Gates) or up to 20,480 Bits of SRAM
- 168 Inputs and I/Os
- Any Configurable Function Block (CFB) can be either 24V10 Logic or SRAM Block
  - — 128 x 10 SRAM Configuration
  - — CFB Selectable 3.3V or 5V Outputs
  - — Open-Drain Output Option
- Supports Group Reconfigurability and Reprogrammability
- JTAG 1149.1 Compatible Test Port
  - — Supports Boundary Scan and In-Circuit Reconfiguration and Re-Programming
- Supported by Industry Standard Design and Programming Tools
- Electrically Erasable 0.6μ ETOX™ IV CHMOS FLASH Technology
  - — Power Management Options Minimize Active Power Consumption (2.5 mA/MHz)
  - — 1 mA Standby
- High Drive I/O
  - — PCI Capable
  - — 24 mA Drive Capability
- 24V10 Macrocell Features
  - — Dual Feedback on All I/O Pins
  - — Allocation Supports up to 16 Product Terms per Macrocell with No Performance Penalty
  - — 12 Clocking Options
  - — Flexible Preset/Clear Options
  - — Selectable D/T Flip-Flops
  - — Fast 12-Bit Identity Compare Option
- Sixteen Configurable Function Blocks (CFBs) Linked by a 100% Connectable Matrix
  - — Improves Fitting of Complex Designs
- Available in 208-Pin Ceramic Pin Grid Array (PGA)
- Military Temperature Range: $-55°C$ to $+125°C$ (T_C)

Package Options

Contact the factory for package options and pinout.

*Other brands and names are the property of their respective owners.

July 1994 Order Number: 271311-001

INTRODUCTION

The Military iFX8160 is a member of the Intel FLEXlogic FPGA (Field Programmable Gate Array) family. The Military iFX8160 consists of sixteen configurable function blocks (CFBs) linked by a 100% connectable matrix. Each CFB can be defined either as a 24V10 logic block or as a block of 128-word x 10-bit SRAM. This will provide approximately 7,000 gates of logic in a PGA package.

FLEXIBLE PERFORMANCE

The Military iFX8160 uses Intel's 0.6μ ETOX FLASH technology to provide a 66 MHz external clock frequency with predictable 12 ns pin-to-pin delays and high drive capability. This advanced process technology combined with power management options enables very low active and standby power consumption.

FLEXIBLE FEATURES

The unique combination of features available in the Military iFX8160 make it ideal for a wide variety of applications. For example, the high performance and flexible clock options provided are designed to support functions such as bus control, custom cache and DRAM control for the current and next generation of Intel microprocessors. The very low power consumption and user selectable 5V/3.3V outputs allow the Military iFX8160 to be used in mixed voltage applications such as portable or embedded systems where CPUs operating at 3.3V still need to communicate to 5V peripherals. The combination of SRAM and logic in a single device becomes a big advantage when designing communication or bus interface controllers where memory is required for buffering data in addition to the logic for the controller design. High drive I/O buffers allow the Military iFX8160 to directly interface to a system bus like PCI without the need for external buffers.

FLEXIBLE TESTING AND PROGRAMMING

The Military iFX8160 provides dedicated JTAG 1149.1 compatible pins to support boundary scan and in-circuit reconfiguration/reprogramming. In-circuit reconfiguration/reprogramming not only allows the designer ultimate flexibility in prototyping new designs but also supports applications where the final configuration is not fixed. New configurations may be downloaded to the Military iFX8160 upon power-up to reflect changes in system organization or design requirements that cannot be determined at production time. For more information on in-circuit reconfiguration and reprogramming, refer to Application Note AP-394.

FLEXIBLE TOOLS SUPPORT

The FLEXlogic FPGA family is supported by industry standard design entry/programming environments including Intel's PLDshell Plus software. This software runs on Intel386™ or higher PC-compatible platforms, and is offered FREE of charge.

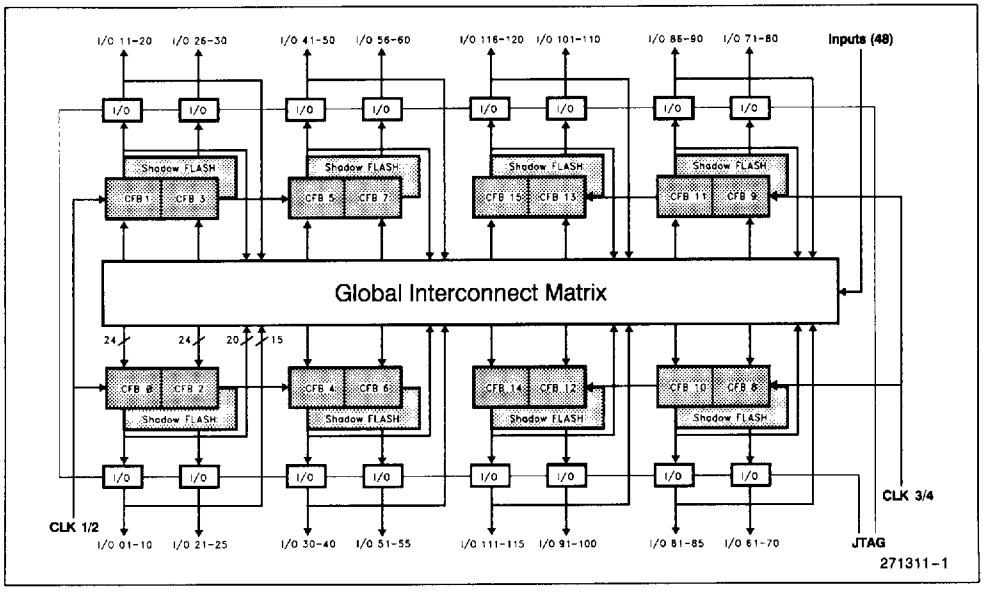


Figure 1. iFX8160 Architecture

INTERCONNECT

The Global Interconnect Matrix that connects each of the CFB blocks is 100% connectable. Any combination of signals in the matrix can be routed into any CFB block, up to the maximum fan-in of the block (24).

This high degree of connectivity between CFB blocks eliminates routing problems during rework of a complex design.

Configurable Function Blocks (CFB)

Each CFB can be defined either as a 24V10 logic block or as a block of 128-word x 10-bit SRAM.

24V10 Configuration

When a CFB is configured as 24V10 logic, each block contains a product term array, a P-Term Allocation circuit, 10 macrocells, clocks and I/O logic in the familiar architecture of a simple PLD.

The 24V10 CFB blocks have a generous fan-in to macrocell ratio (24:1). This improves the fitting capacity of the Military iFX8160 architecture by providing more available lines from the global interconnect matrix for each macrocell.

The 24V10 blocks also provide two asynchronous Clear/Preset control terms and two Output Enable control terms (with an inversion option for each). Within each 24V10 block an identity compare circuit is available that can perform a compare of up to 12 bits within the t_{PD} of the device.

MACROCELL CONFIGURATIONS

Each I/O of the device has dual (internal and pin) feedback paths (see Figure 2). This allows macrocells to be used for buried logic while the I/O pins are used as inputs. Macrocell outputs that are not brought outside the package may still be used to provide buried logic since internal feedback is available. The macrocells can be configured either as a fast combinatorial block, a D-register, or a T-register. J/K and S/R registers are available via software emulations.

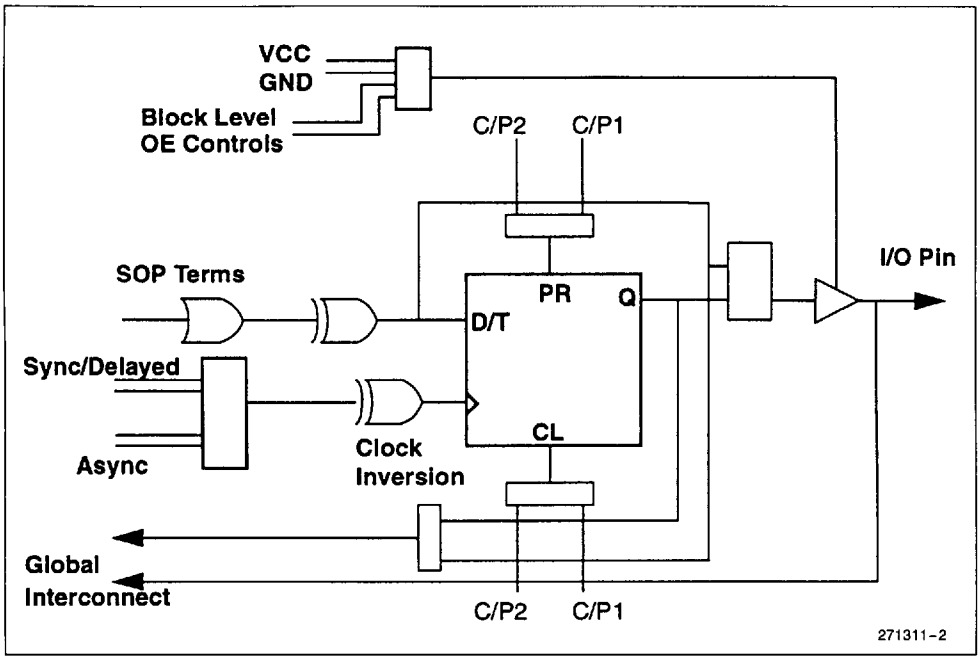


Figure 2. CFB as 24V10 Block

CLOCKING MODES

There are three clocking modes available for every macrocell (see Figure 3): *synchronous, delayed, asynchronous.* Table 1 shows the different timing options each clock mode offers.

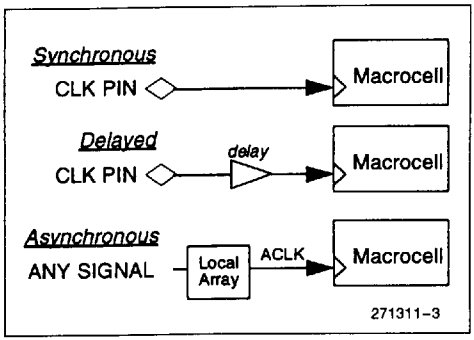


Figure 3. Clocking Modes

Synchronous is the standard clock mode where the register clock is driven directly from one of the four global clock pins.

Delayed clock is similar to *synchronous*, but there is a local delay added (within the CFB) to either of the two synchronous clock signals.

Asynchronous mode is where the register clock uses one of the two local CFB ACLK product terms.

Table 1. Clock Mode Timings

Mode	T_{SU}	T_{HOLD}	T_{CO}
Synchronous	7	0	8
Delayed	8	2	10
Asynchronous	2	5	14

In addition, each clocking mode may be inverted to allow the macrocell register to be clocked either on the rising or falling edge of the clock signal. This combination provides up to twelve different clock options for each macrocell.

CONTROL SIGNALS

There are 4 control signals in each CFB in addition to the clocks (see Figure 4). These include two Output Enable (OE) signals, and two asynchronous Clear/Preset signals. This provides a total of 32 clear/preset and 32 output enable signals within the Military iFX8160. Each control signal is generated by a single product term from the local 24V10 AND array with an inversion option. This allows multiple product term control equations to be implemented.

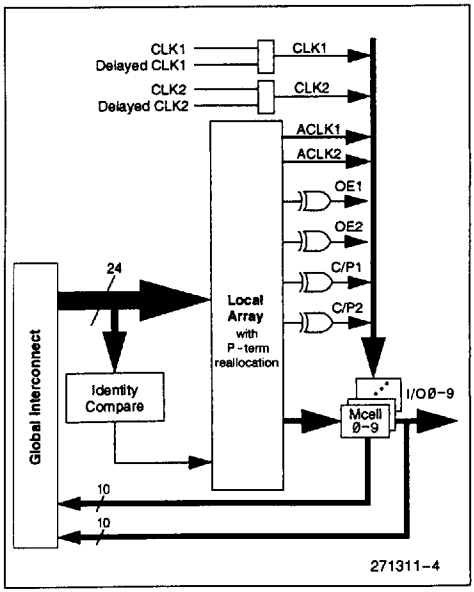


Figure 4. Control Signals

COMPARATOR LOGIC

Each 24V10 block provides a comparator circuit (see Figure 5). This circuit can do an identity compare of up to 12 signals, within the T_{PD} of the device.

The number of bits that can be compared is only limited by the fan-in of the CFB. Since the fan-in is 24 signals, a 12-bit comparator is the maximum implementation possible.

When less than 12 bits are being compared, the other signals available from the Interconnect Matrix can be used in equations. For instance, doing an 8-bit compare still leaves 8 other signals on the block fan-in (24 − 16 = 8). The bits being compared may also be used to implement SOP logic in parallel with the compare function.

The output of the comparator circuit may be used in place of any of the product term pairs in the product term allocation logic allowing the compare result to be used in any macrocell. However, only one of the ten macrocells in the CFB can use the comparator output.

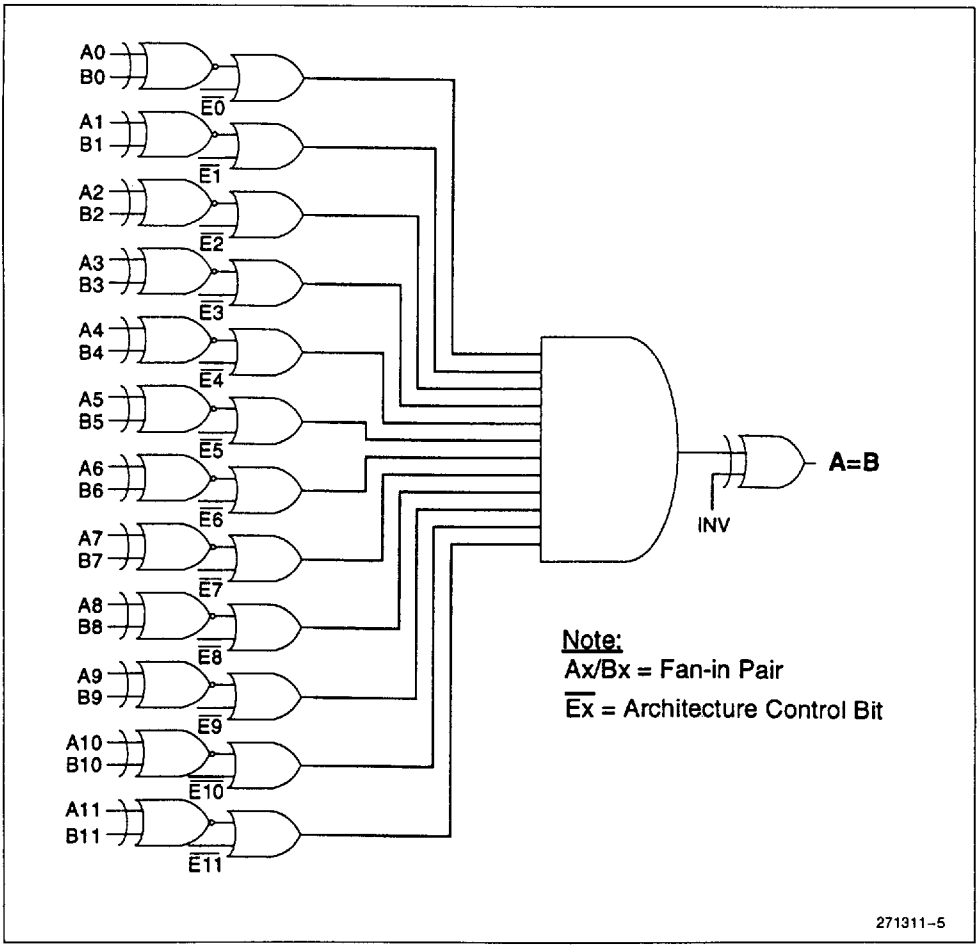


Figure 5. 12-Bit Identity Compare Logic

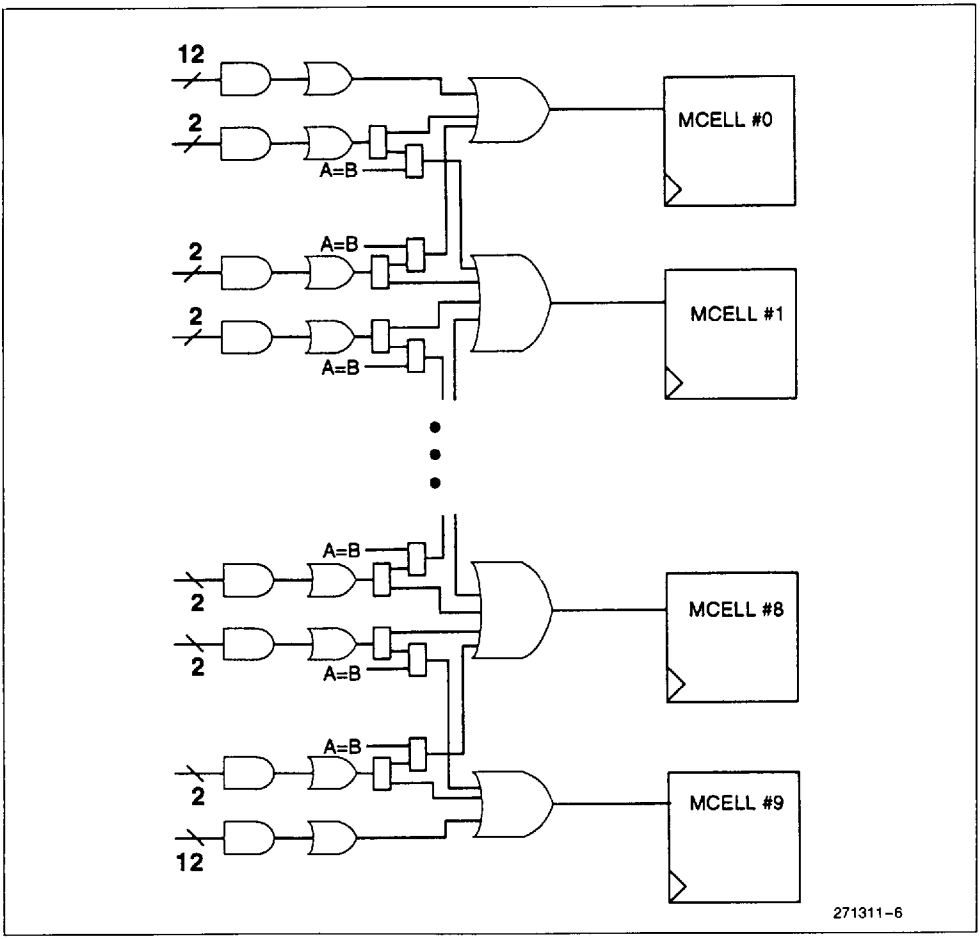


Figure 6. CFB Product Terms

PRODUCT TERM ALLOCATION

The Military iFX8160 uses the patented Intel product term allocation scheme, which gives better utilization of the P-term resources without the performance penalty of other approaches. The P-terms are typically grouped into sets of two product terms each, and there are two sets per macrocell.

Each macrocell may borrow from adjacent macrocells in order to increase the total number of P-terms to a maximum of 8. In addition, the macrocells located at the "ends" of each CFB have access to additional product terms and can support up to 16 P-term equations (see Figure 6). The performance of any macrocell is the same whether 2 P-terms or 16 P-terms are being used.

SRAM Configuration

Each Military iFX8160 CFB block can be configured as a 128 x 10 (128 words by 10 bits) SRAM block (see Figures 7 and 8). The SRAM is accessed in a conventional manner by using 7 bits of the 24 signal fan-in as address information and 10 bits as data-in. Three bits are used for BE (Block Enable), WE (Write Enable), and OE (Output Enable) controls (see Table 2). SRAM control signals on the Military iFX8160 may be active-high or active-low.

Table 2. SRAM Function Table

Inputs			Cycle	I/O Pins
$\overline{BE}$/BE	$\overline{WE}$/WE	$\overline{OE}$/OE		
1/0	X	X	None	Disabled
0/1	1/0	1/0	Read	Disabled
0/1	1/0	0/1	Read	Enabled
0/1	0/1	1/0	Write	Disabled
0/1	0/1	0/1	Write	Enabled

It is possible to define the SRAM memory either with a bidirectional I/O data bus or with a separate input data bus and output data bus.

The SRAM memory bits are initialized by the on-chip FLASH cells during power-up. Therefore, the data in the SRAM can be pre-configured at programming time. As long as no memory writes to this block are executed, the SRAM will contain a copy of the nonvolatile cells. In this way, the SRAM block can be used as read only memory (ROM).

When a CFB is configured as a SRAM, regular Sum-of-Product logic is unavailable in that block. All of the logic and p-terms have been converted to SRAM use. The macrocells, however, are available to latch the SRAM output. This allows the registered SRAM output to directly drive a subsystem like a D/A converter.

Different sized SRAM organizations are possible by cascading multiple CFBs to increase the width or depth of the memory.

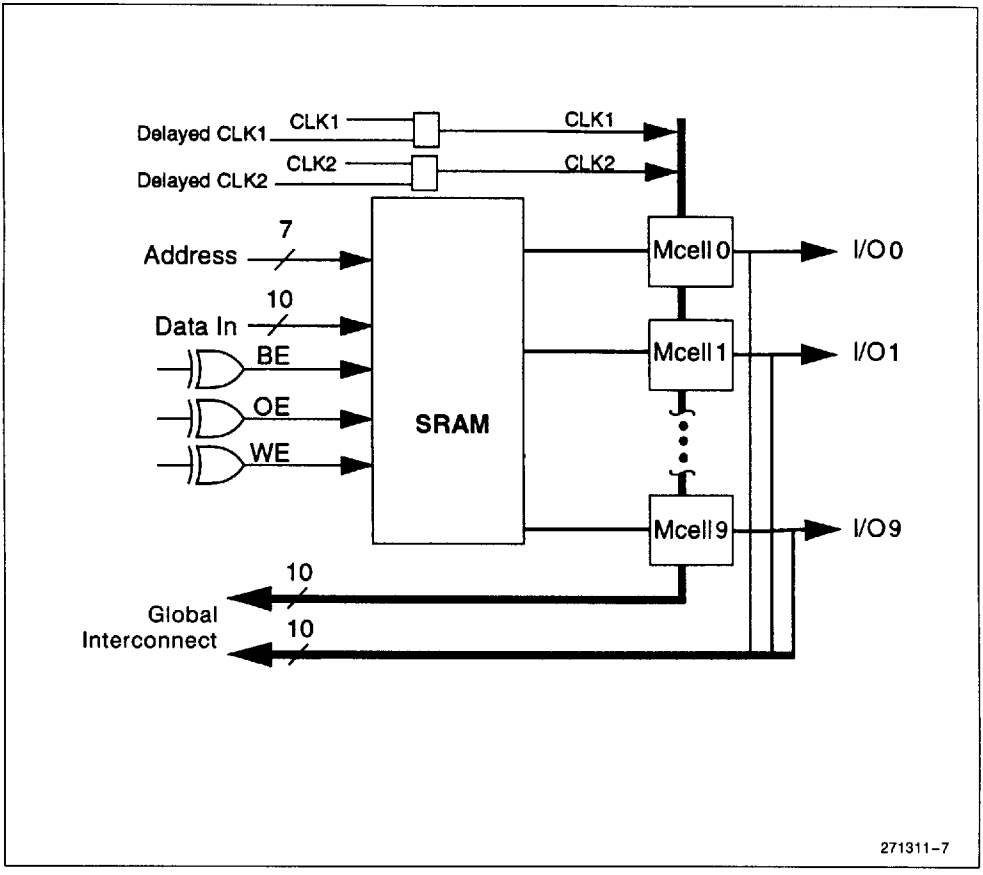


Figure 7. SRAM Overall Block Diagram

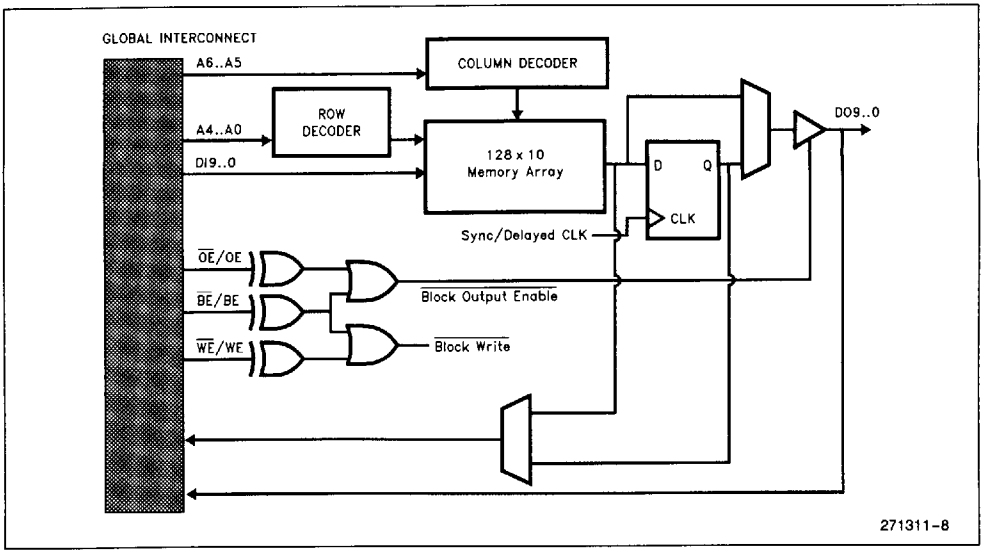


Figure 8. SRAM Functional Block Diagram

Input Configuration

Inputs, as well as I/O pins that are used as inputs, can be optimized for minimum standby current during either CMOS or TTL operation by using the "CMOS_LEVEL" and "TTL_LEVEL" keywords available in the PLDasm design language of PLDshell Plus. For 5V CMOS inputs, the "CMOS_LEVEL" keyword should be used. For TTL or 3.3V CMOS inputs, the "TTL_LEVEL" keyword (the default condition for PLDasm) should be used to minimize standby power consumption. Third party tools that support the FLEXlogic family provide input configuration in a method specific to each tool. For additional information refer to Application Brief AB-27.

Output Configuration

3.3V SELECTION

The pins in an I/O block can operate at 3.3V by tying the appropriate V_{CCO} pins to a 3.3V power supply. While the Military iFX8160 still requires 5V V_{CC} for normal operation, the V_{CCO} pin associated with each CFB block pair may be connected to either 5V or 3.3V to control the output voltages of the I/O pins in that block pair. This allows the Military iFX8160 to be used in mixed voltage systems. For example, the Military iFX8160 device may be used as an interface to bridge between a 3.3V CPU and 5V peripheral logic. In addition, all input pins are 5V safe so mixing 3.3V outputs and 5V inputs is supported.

OPEN DRAIN OUTPUT OPTION

The device can also be configured to an open drain output option for each I/O pin. If desired, more complex equations can be implemented by using multiple open drain outputs with an externally supplied pull-up resistor to emulate an additional OR plane.

TTL VERSUS CMOS OUTPUTS

There is a weak pullup provided for CMOS-compatible outputs. This pullup is always active in both 3.3V and 5V modes.

I/O PULL UP RESISTOR

There is an active weak pull-up resistor on the I/O pins which hold the I/O at a logic 1 level during power-up, reconfiguration and erase/program cycles. This resistor is disabled during normal device operation to reduce power consumption. Dedicated inputs do not have active pull-up resistors.

HIGH DRIVE I/O

The Military iFX8160 output buffers are designed specifically for applications requiring high drive current. These buffers allow the iFX8160 to drive a bus, like PCI, and at the same time provide 12 ns pin-to-pin performance. This eliminates the need for external buffers and their associated delays. This drive capability will also benefit designs on other standard buses.

PCI CAPABILITIES

The output buffers of the Military iFX8160 are designed to meet the PCI V/I curve specifications. As a result, the Military iFX8160 will achieve the acceptable drive voltages in typical PCI configurations.

The Military iFX8160-12 also offers a predictable, 12 ns pin-to-pin propagation delay, 8 ns clock-to-signal valid delay, and 7 ns synchronous setup time to meet the timing demands of PCI applications. To support bi-directional PCI signals, two output enable (OE) products terms are provided in each CFB for a total of 32 OE p-terms in the device.

When using the Military iFX8160 in PCI applications, the designer should ensure that the total input capacitance on a PCI signal line or clock line does not exceed 100 pF or 120 pF, respectively. The typical input capacitance of the Military iFX8160 has been characterized at 10 pF for a dedicated input, 12 pF for an I/O and 15 pF for the clock.

As a rule of thumb, a PCI system can have a load of up to 10, where peripherals on the system board count as one and PCI peripherals in slots as two. Typical PCI Local Bus implementations support up to three expansion cards. As a result, the small additional capacitance presented will not adversely affect the system performance.

For further information on the use of the Military iFX8160 in PCI applications, refer to Application Note AP-396, order number 292143.

JTAG/IEEE 1149.1 TESTABILITY

The JTAG/IEEE 1149.1 Standard Boundary Scan architecture is implemented in the Military iFX8160. This feature supports fault isolation testing of board designs at the component level and enhances production testing, field repair, and is ideal for Fault Tolerant applications.

The Military iFX8160 boundary scan support consists of an Instruction Register, a Data Register, scan cells, and associated logic which are accessed through the Test Access Port (TAP). The TAP interface consists of three inputs: Test Mode Select (TMS), Test Data In (TDI) and Test Clock (TCK), and one output: Test Data Out (TDO).

The Military iFX8160 contains two JTAG TAP controllers that support group (partial) reconfiguration, group reprogramming and boundary scan. Figure 13 shows the internal connection of the JTAG Tap controllers.

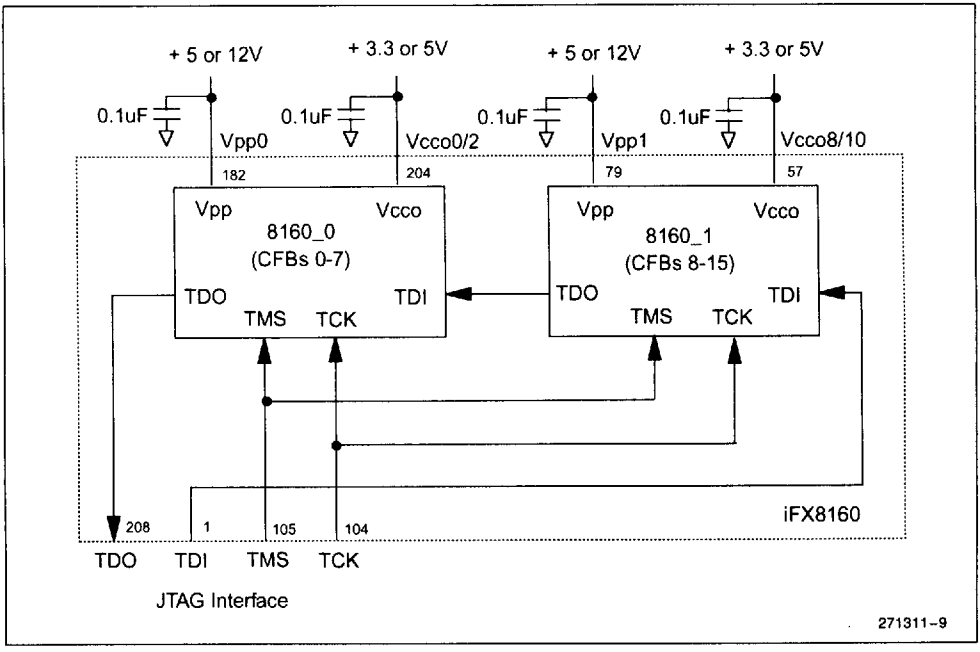


Figure 13. iFX8160 JTAG Connections of TAP Controllers

The boundary scan cells of the iFX8160 external signals are linked to form a shift register chain for all active pins. This chain provides a path which can be used to shift in test stimulus as well as shift out test response data for inspection.

For example, a continuity test may be performed between two JTAG devices on a circuit board by placing a known value on the output buffers of one device while observing the input buffers of the other device. This same technique may be used to perform simple in-circuit functional testing of the Military iFX8160 for prototyping new system designs.

The 4-pin JTAG test interface is also used for standard programming, in-circuit reconfiguration, and in-circuit reprogramming.

Boundary Scan Instructions

The Military iFX8160 boundary scan Instruction Register (IR) supports public instruction opcodes, extended instruction opcodes used for the Program/Verify modes, and additional Intel private instructions.

Public Instructions

EXTEST (IR OPCODE 00000 BINARY)

The EXTEST instruction drives the output pins to the values contained in the boundary scan cells which allows testing of circuitry external to the Military iFX8160 package, typically for printed circuit board interconnects.

BYPASS (IR OPCODE 11111 BINARY)

The BYPASS instruction selects the one bit ByPass Register, (BPR), to be connected to TDI and TDO.

SAMPLE/PRELOAD (IR OPCODE 00001 BINARY)

The SAMPLE/PRELOAD instruction is used for two functions. The SAMPLE/PRELOAD instruction 1) allows a snap-shot of the values of the pins of the Military iFX8160 in an unobtrusive manner and 2) preloads data to the Military iFX8160 pins to be driven to the system circuit board when executing the EXTEST instruction.

IDCODE (IR OPCODE 00010 BINARY)

The IDCODE instruction selects the ID code register to be connected to TDI and TDO allowing the ID-code to be serially shifted out of TDO.

UESCODE (IR OPCODE 10110 BINARY)

The UESCODE instruction selects the User Electronic Signature (UES) register to be connected to TDI and TDO allowing the UES code to be serially shifted out of TDO.

HIZ (IR OPCODE 01000 BINARY)

The HIZ instruction sets all I/Os to a high impedance state.

For additional information on JTAG instructions, refer to Application Note AP-395, order number 292142-001.

IN-CIRCUIT RECONFIGURATION AND REPROGRAMMING

The Military iFX8160 supports in-circuit reconfiguration through the use of the 4-pin JTAG test port. Downloading a new configuration can be accomplished by simply shifting the new data into the device. This may be done as many times as desired in a prototyping scenario.

Once the design is confirmed it may be programmed into the FLASH cells so that the configuration will not be lost even when the power is turned off. This is also done through the use of the JTAG test port plus the programming voltage pins (V_{PP}).

The Military iFX8160 FLASH cells are electrically erasable and may be reprogrammed.

Group reconfiguration and reprogrammability is supported in the Military iFX8160. New configurations may be downloaded to either half of the Military iFX8160 (see Figure 13) during operation to reflect changes in system design, while the other half continues to operate.

For more information on in-circuit reconfiguration/reprogramming and group reconfiguration, refer to Application Brief AP-394, order number 292145-001.

SECURITY

A programmable security bit controls access to the data programmed into the device. Once this security bit is set, the design cannot be read out of the nonvolatile cells or the SRAM. The state of the nonvolatile security bit at power-up determines access and cannot be changed by in-circuit reconfiguration.

SOFTWARE SUPPORT

PLDshell Plus

PLDshell Plus is a sophisticated development tool for Intel programmable logic and is all you need to begin designing with Intel FPGAs. With PLDshell Plus, you can develop, compile, and simulate efficient designs for Intel FPGAs and PLDs.

PLDshell Plus is FREE of charge and includes support for:

- Design Merge
- SRAM Configuration Support
- Compare Operation Support
- Simulation Support for Intel FPGAs
- Vector Notation
- Device Selector

DESIGN MERGE

PLDshell Plus can merge multiple PDS design files into any Intel PLD, including the Intel Military iFX8160. The Merge function makes it easy for designers to consolidate multiple PLDs into a single, high-performance FPGA or PLD.

FPGA ARCHITECTURAL FEATURE SUPPORT

PLDshell Plus supports all of the innovative architectural features of the Military iFX8160 through the implementation of new language syntax such as:

- SRAM configuration
- Compare operation
- Buried macrocells
- Clocking options
- 3.3V and 5V options

FUNCTIONAL SIMULATION

PLDshell Plus allows the designer to simulate the internal function of any Intel FPGA or PLD for rapid design verification.

PLDshell Plus provides the following simulation capabilities:

- Event-driven simulation of combinatorial, registered, and state machine designs
- Ability to set any input, preload any register, and compare any output against an expected value
- Ability to group signals together (form a vector) to simulate a bus
- Generation of test vectors from simulation results for inclusion in the JEDEC file

DEVICE SELECTOR

The designer can develop the logic design first, and then use the PLDshell Plus device selector to pick a list of appropriate devices. After a design is compiled or estimated through PLDshell Plus a report file is generated. Contained in the report file is a listing of suggested devices appropriate for the target design.

SYSTEM REQUIREMENTS

Listed below are the minimum requirements for a system in order to use PLDshell Plus:

- Intel 386 based PC compatible
- 3 MB available hard drive space (minimum)
- 4 MB extended memory (minimum)
- VGA monitor/adaptor
- DOS 3.1 (or later)

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})[1] ..... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})[1] ..... −2.0V to +12.6V

DC Input Voltage (V_I)[1, 2] .... −0.5V to V_{CC} + 0.5V

Storage Temperature (T_{stg}) ..... −65°C to +150°C

Ambient Temperature (T_{amb})[3] ... −10°C to +85°C

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

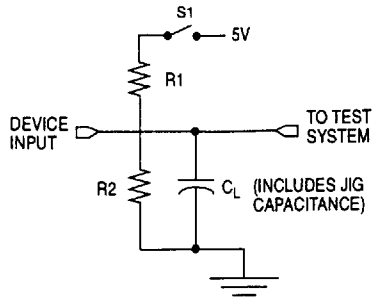
Symbol	Parameter	Min	Max	Units
V_{CC}/V_{CCO}	Supply Voltage—5.0V	4.75	5.25	V
V_{CCO}	Output Supply Voltage—3.3V	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CCO}	V
T_C	Operating Case Temperature	−55	+125	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

DC CHARACTERISTICS (Over Specified Operating Conditions)

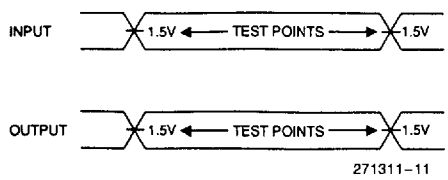
Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}(5)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(5)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}(7)	5V TTL High Level Output	2.4			V	I/O = −16.0 mA D.C., V_{CC} = Min.
	5V CMOS High Level Output	V_{CCO} − 0.2			V	I/O = −100 μA D.C., V_{CC} = Min.
	3V High Level Output Voltage	V_{CCO} − 0.2			V	I/O = −100 μA D.C., V_{CC} = Min.
V_{OL}(7)	5V Low Level Output Voltage			0.5	V	I/O = 24.0 mA D.C., V_{CC} = Min.
	3V Low Level Output Voltage			0.2	V	I/O = 12 mA D.C., V_{CC} = Min.
I_I(8)	Input Leakage Current			±10	μA	V_{CC} = Max., V_{IN} = GND or V_{CC}
I_{OZ}	Output Leakage Current			±50	μA	V_{OUT} = V_{CC} Max.
				±100		V_{OUT} = GND
I_{SC}(6)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max., V_{OUT} = 0.5V
I_{SB}	Standby Power Supply Current		1		mA	V_{IN} = V_{CC} or GND, Outputs Open
I_{CC} Active	Power Supply Current		2.5		mA per MHz	V_{IN} = V_{CC} or GND, Outputs Open, Device Programmed as Eight 20-Bit Counters
V_{PP}	Programming Voltage	11.4	12	12.6	V	
I_{PP1}(9)	V_{PP} Read Current, ID Current or Standby Current		90	200	μA	V_{PP} > V_{CC}
			15	40		V_{PP} ≤ V_{CC}
I_{PP2}(9)	V_{PP} Programming/ Program Verify Current		30	60	mA	V_{PP} = V_{PPH} Programming in Progress
I_{PP3}(9)	V_{PP} Erase/Erase Verify Current		30	60	mA	V_{PP} = V_{PPH}
E_{CNT}	Erase/Reprogram Count Limit			100		

NOTES:
4. Typical values are at T_A = 25°C, V_{CC} = 5V.
5. Absolute values with respect to device GND; all over and undershoots due to system and tester noise are included. Do not attempt to test these values without suitable equipment.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
7. When driving an I/O pin under JTAG boundary scan, I_{OH} = −4.0 mA and I_{OL} = 12 mA.
8. Input Leakage current on JTAG pins: ±20 μA
9. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C.

AC TESTING LOAD CIRCUIT



AC TESTING INPUT, OUTPUT WAVEFORM



NOTE:
Inputs are driven at 3.0V for a LOGIC "1" and 0V for a Logic "0". Timing measurements are made at 1.5V. Outputs are measured at 1.5V. Device input rise and fall times < 3 ns.

SWITCHING TEST CIRCUIT

Specification	S1	C_L	Commercial		Measured Output Value
			R1	R2	
t_{PD}	Closed	35 pF	165Ω	100Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

PIN CAPACITANCE(10)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz		10	12	pF
C_{IO}	I/O Capacitance	V_{OUT} = 2V, f = 1.0 MHz		12	15	pF
C_{CLK}	Clock Pin Capacitance	V_{OUT} = 2V, f = 1.0 MHz		15	18	pF
C_{VPP}	V_{PP} Pin Capacitance	f = 1.0 MHz		15	18	pF

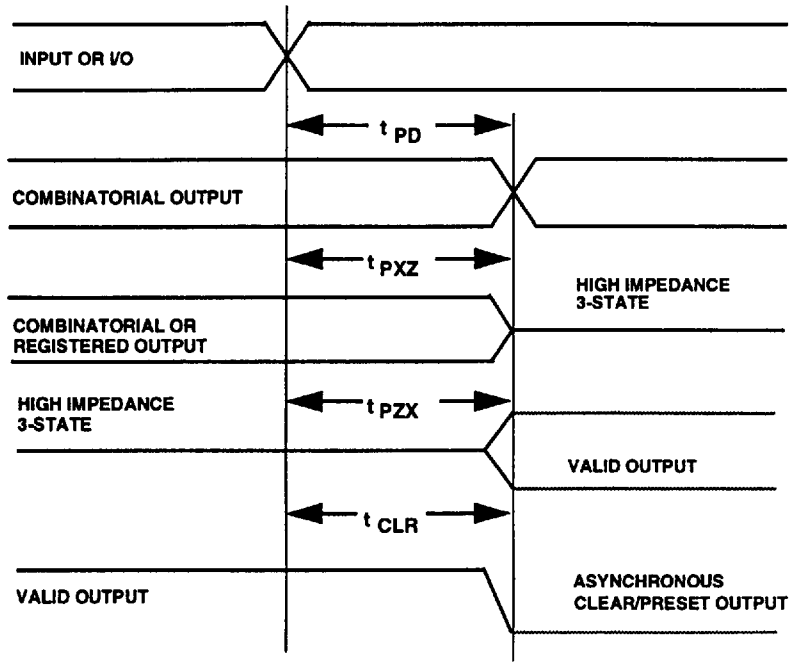
NOTE:
10. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.

COMBINATORIAL MODE AC CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	iFX8160-12			iFX8160-15			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or I/O to Output Valid			12			15	ns
t_{PZX}(11)	Input or I/O to Output Enable			14			17	ns
t_{PXZ}(11)	Input or I/O to Output Disable			14			17	ns
t_{CLR}	Input or I/O to Asynchronous Clear/Preset			17			21	ns
t_{COMP}	Comparator Input or I/O Feedback to Output Valid			12			15	ns

NOTE:
11. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by specified output load. t_{PXZ} is measure with C_L = 5 pF. Z → H and Z → L are measured at 1.5V on output.

COMBINATORIAL MODE WAVEFORMS



REGISTER MODE—MILITARY iFX8160-12 CLOCK AC CHARACTERISTICS

(Over Specified Operating Conditions)

Symbol	Parameter	Synchronous		Delayed Synchronous		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max. Counter Frequency $1/(t_{SU} + t_{CO1})$—External Feedback	66		62.5		58.8		MHz
f_{CNT2}	Max. Counter Frequency $1/(t_{CNT})$—Internal Feedback	66		62.5		58.8		MHz
f_{MAX}	Max. Frequency (Pipelined) $1/(t_{CP})$—No Feedback	83.3		83.3		76.9		MHz
t_{SU}	Input or I/O Setup Time to CLK	7		6		3		ns
t_H	Input or I/O Hold Time from CLK	0		2		5		ns
t_{CO1}	CLK to Output Valid		8		10		14	ns
t_{CO2}	CLK to Output Valid Fed through Combinatorial Macrocell		18		20		24	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		15		16		17	ns
t_{CL}	CLK Low Time	5.5		5.5		6		ns
t_{CH}	CLK High Time	5.5		5.5		6		ns
t_{CP}	CLK Period	12		12		13		ns

REGISTER SRAM READ—MILITARY iFX8160-12 AC CHARACTERISTICS

(Over Specified Operating Conditions)

Symbol	Parameter[12]	Synchronous		Delayed Synchronous		Units
		Min	Max	Min	Max	
t_{SU}	Input or I/O Setup Time to CLK	12		11		ns
t_H	Input or I/O Hold Time from CLK	0		2		ns
t_{CO1}	CLK to Output Valid		6		10	ns
t_{CL}	CLK Low Time	5.5		5.5		ns
t_{CH}	CLK High Time	5.5		5.5		ns
t_{CP}	CLK Period	15		15.5		ns

NOTE:
12. Device Characterization of Registered SRAM T_{SU}/T_{CO} has not been completed.

REGISTER MODE—MILITARY iFX8160-15 CLOCK AC CHARACTERISTICS

(Over Specified Operating Conditions)

Symbol	Parameter	Synchronous		Delayed Synchronous		Async		Units
		Min	Max	Min	Max	Min	Max	
f_{CNT1}	Max. Counter Frequency $1/(t_{SU} + t_{CO1})$—External Feedback	50		50		46.5		MHz
f_{CNT2}	Max. Counter Frequency $1/(t_{CNT})$—Internal Feedback	50		50		46.5		MHz
f_{MAX}	Max. Frequency (Pipelined) $1/(t_{CP})$—No Feedback	71.4		68.9		66.7		MHz
t_{SU}	Input or I/O Setup Time to CLK	10		8		4.5		ns
t_H	Input or I/O Hold Time from CLK	0		2		6		ns
t_{CO1}	CLK to Output Valid		10		12		17	ns
t_{CO2}	CLK to Output Valid Fed through Combinatorial Macrocell		24		24		26.5	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path		20		20		21.5	ns
t_{CL}	CLK Low Time	6.5		6.5		6.5		ns
t_{CH}	CLK High Time	6.5		6.5		6.5		ns
t_{CP}	CLK Period	14		14.5		15		ns

REGISTER SRAM READ—MILITARY iFX8160-15 AC CHARACTERISTICS

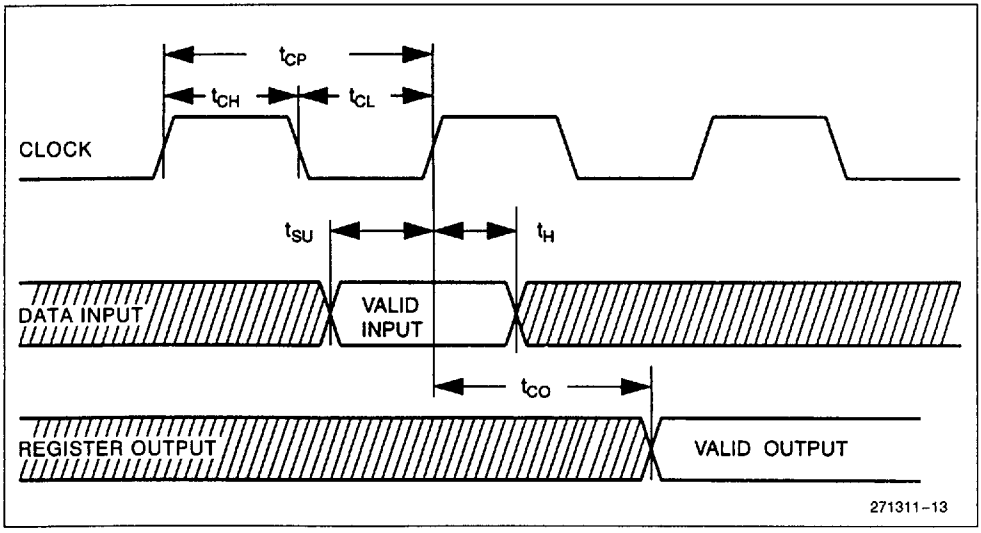
(Over Specified Operating Conditions)

Symbol	Parameter[12]	Synchronous		Delayed Synchronous		Units
		Min	Max	Min	Max	
t_{SU}	Input or I/O Setup Time to CLK	14		12		ns
t_H	Input or I/O Hold Time from CLK	0		2		ns
t_{CO1}	CLK to Output Valid		9.5		11.5	ns
t_{CL}	CLK Low Time	6.5		6.5		ns
t_{CH}	CLK High Time	6.5		6.5		ns
t_{CP}	CLK Period	17		17.5		ns

NOTE:

12. Device Characterization of Registered SRAM T_{SU}/T_{CO} has not been completed.

REGISTERED MODE WAVEFORMS

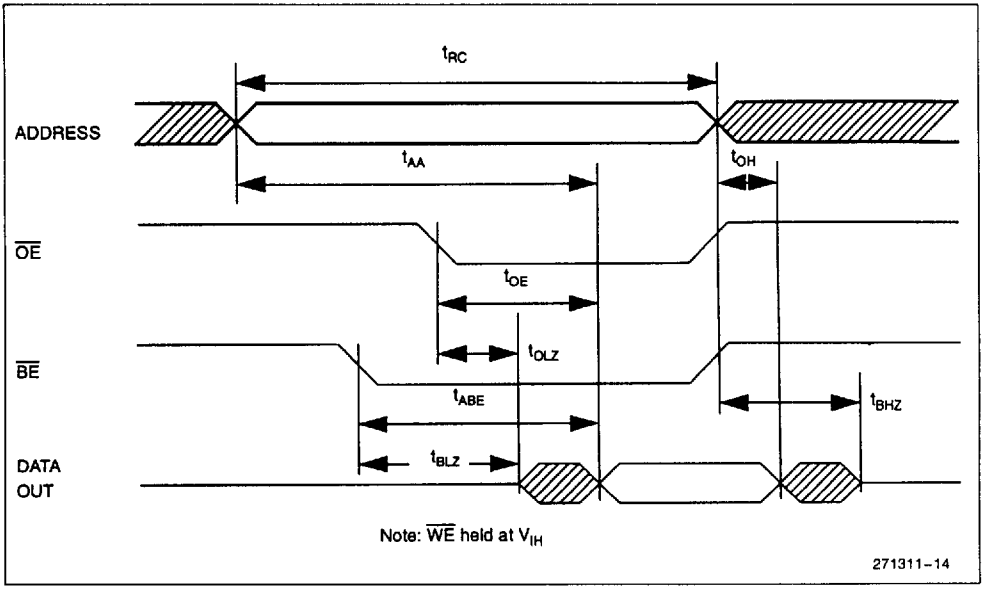


SRAM READ—AC CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	iFX8160-12		iFX8160-15		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		18		ns
t_{AA}	Address Access Time		15		18	ns
t_{ABE}	Block Enable Access Time		15		18	ns
t_{OE}(13)	Output Enable to Output Valid		12		15	ns
t_{OH}	Output Hold from Address Change	2		3		ns
t_{BLZ}(13)	Block Enable to Output in Low Z	3		4		ns
t_{BHZ}(13, 14)	Block Disable to Output in High Z		12		15	ns
t_{OLZ}(13)	Output Enable to Output in Low Z	3		4		ns

NOTES:
13. These signals are measured at ±0.5V from steady state voltage as driven by specified output load. Z ⟶ H and Z ⟶ L are measured at 1.5V on output.
14. These signals are measured with C_L = 5 pF.

TIMING WAVEFORM OF READ CYCLE

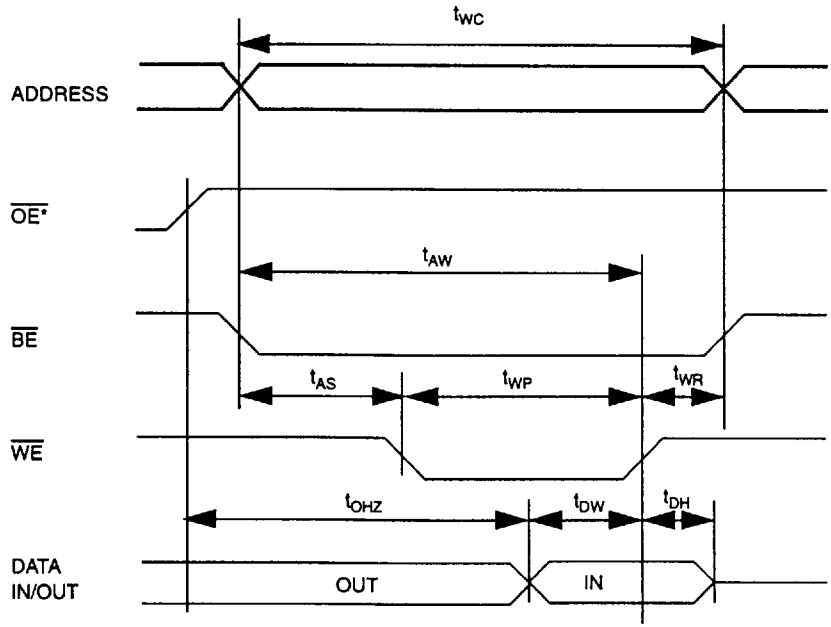


SRAM WRITE—AC CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	iFX8160-12		iFX8160-15		Units
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		18		ns
t_{BW}	Block Enable to End of Write	10		12		ns
t_{AW}	Address Valid to End of Write	13		15		ns
t_{AS}	Address Set-up Time	3		3		ns
t_{WP}	Write Pulse Width	10		12		ns
t_{WR}	Write Recovery Time	2		3		ns
t_{DW}	Data Valid to End of Write	10		12		ns
t_{DH}	Data Hold Time	2		3		ns
t_{OHZ}(13, 14, 15)	Output Disable to Valid Data In	12		15		ns

NOTES:
13. These signals are measured at ±0.5V from steady state voltage as driven by specified output load. Z ⟶ H and Z ⟶ L are measured at 1.5V on output.
14. These signals are measured with C_L = 5 pF.
15. Does not apply for separate data in and data out buses.

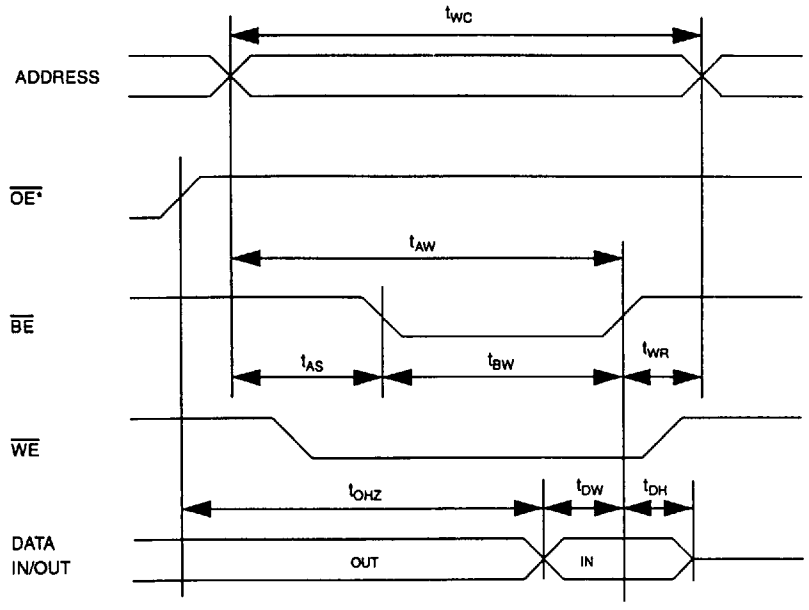
TIMING WAVEFORM OF WRITE CYCLE #1 ($\overline{WE}$ Controlled Timing)



*Note: Cycle shown is for common data in and data out bus.

271311-15

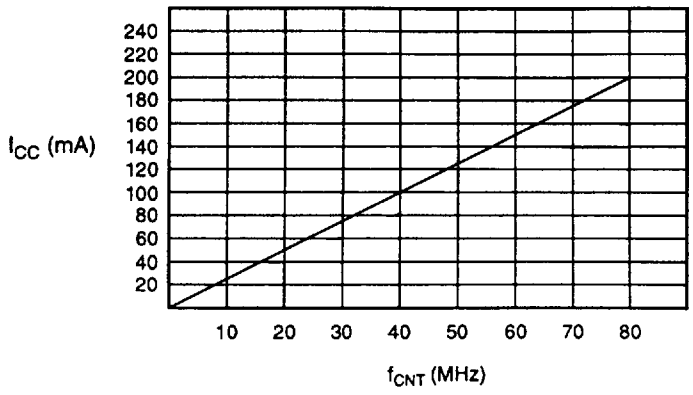
TIMING WAVEFORM OF WRITE CYCLE #2 ($\overline{BE}$ Controlled Timing)



*Note: Cycle shown is for common data in and data out bus.

271311-16

I_{CC} VERSUS FREQUENCY



Conditions: TA = +25°C, VCC = 5V

(Note: Eight 20-bit counters)

271311-17

POWER-UP CYCLE

Because V_{CC} rise can vary significantly from one application to another, the power-up cycle time varies. For a monotonic V_{CC} rise (1 ms/V min.), the power-up cycle is complete when V_{CC} reaches the V_{CC} min. value.

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered-up. Also, the JTAG TAP controller will be put into the *Test-Logic-Reset* state. During power-up I/Os are held high by an active weak pullup. The outputs on an unprogrammed device are placed in a high impedance state upon completion of power-up cycle.

POWER-ON RESET (PORST) FEATURE

The iFX8160 configuration may be reloaded from FLASH memory at any time by issuing a JTAG reset or by holding V_{PP} at a logic low level (0.8V max.) for a minimum of 300 ns. By holding V_{PP} low during power-up, the power-up cycle can be delayed. The power-up cycle is completed within a delay of t_{RESET} after V_{PP} reaches 2.0V. During normal operation, V_{PP} must be held at a logic high level (2.4V min.) or tied to the V_{PP} supply (12V).

During reconfiguration or reprogramming, the JTAG reset instruction is automatically issued by the PENGN or JED2JTAG software. It is not necessary to pull V_{PP} low after a reconfiguration or reprogram cycle.

For more information about the PORST feature, refer to Application Note AP-394, order number 292145.

RESET CHARACTERISTICS

Symbol	Parameter	Value	Condition
t_{RESET}	JTAG Reset Time	150 µs Max	Software Control
	$\overline{V_{PP}}$ Reset Time		$V_{PP} \geq 2.0V$

PIN DESCRIPTIONS

Table 4 lists the dedicated pin names and descriptions.

Table 4. Dedicated Pins

Pin Name	Description
V_{CC}(1)	Supply voltage for the Military iFX8160. All must be connected to 5V.
V_{SS}	Ground connections for the Military iFX8160. All must be connected to GND.
V_{PP}(1)	Programming voltage for the Military iFX8160. During programming, 12V must be supplied to this pin. When not in programming mode, this pin may be connected to V_{CC} or V_{PP}. To initiate a reset, hold V_{PP} low (0.8V max.) for a minimum of 300 ns.
INx	Input only pins. These pins may not be available on all packages. Unused inputs should be connected to V_{CC} or GND.
TDI	The Testability Data Input is the boundary scan serial data input to the Military iFX8160. JTAG instructions and data are shifted into the Military iFX8160 on the TDI input pin on the rising edge of TCK. TDI may be left floating if unused.
TDO	The Testability Data Output is the boundary scan serial data output from the Military iFX8160. JTAG instructions and data are shifted out of the Military iFX8160 on the TDO output on the falling edge of TCK.
TCK	The Testability Clock input provides the boundary scan clock for the Military iFX8160. TCK is used to clock state information and data into and out of the Military iFX8160 during boundary scan or programming modes. The maximum operating frequency of the boundary scan test clock is 8 MHz. TCK may be left floating if unused.
TMS	The Testability Control input is the boundary scan test mode select for the Military iFX8160. TMS may be left floating if unused.

Table 5 lists the user-defined pin names and descriptions.

Table 5. User-Defined Pins

Pin Name	Description
V_{CC0x}(1)	Supply voltage for the outputs of the CFBs. Connecting these pins to +5V causes the CFB to output 5V signals. Connecting these pins to +3.3V causes the CFB to output 3.3V signals. These pins must always be connected to the desired output drive voltage.
CLKx	Global clocks.
I/Oxx	Pins that can be configured eithor as an input or an output. Unused I/O pins should be connected to V_{CC} or GND.

NOTES:
1. Proper power decoupling is required on all power pins. A 0.01 μF decoupling capacitor is recommended between each power pin and ground.