JN5148 Module Development Reference Manual

JN-RM-2052
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Contents

About this Manual

This manual describes low-cost reference designs for modules based around a Jennic JN5148 wireless microcontroller.

The Jennic wireless microcontroller modules provide a compact, low-cost solution for 2.4-GHz IEEE 802.15.4 Low-Rate WPANs (Wireless Personal Area Networks).

The design considerations presented in this manual are equally valid for bespoke solutions where the wireless microcontroller is placed directly onto the product PCB.

Organisation

This manual consists of 3 chapters, as follows:

- Chapter 1 introduces the reference design.
- Chapter 2 outlines essential design considerations.
- Chapter 3 outlines design considerations for bespoke solutions.

Conventions

Files, folders, functions and parameter types are represented in **bold** type.

Function parameters are represented in *italics* type.

Code fragments are represented in the Courier typeface.

Acronyms and Abbreviations

PAN	Personal Area Network
PCB	Printed Circuit Board
SPI	Serial Peripheral Interface
TQFN	Thin Quad Flat No-lead
WPAN	Wireless Personal Area Network
EMC	Electro Magnetic Compatibility
RF	Radio Frequency
FCC	Federal Communications Commission
ETSI	European Telecommunications Standards Institute

Feedback Address

If you wish to comment on this manual, or any other Jennic user documentation, please provide your feedback by writing to us (quoting the manual reference number and version) at the following postal address or e-mail address:

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1 Reference Design

Jennic provide a comprehensive range of JN5148 module reference designs for standard and high-power modules with different antennae. Each reference design comprises a ZIP file containing the following information:

- Documentation
- Schematics
- PADS database
- Layout database
- Bill-of-Materials

The following table provides a summary of the JN5148 module reference designs available from the Support area of the Jennic web site (www.jennic.com/support).

Part Number	Description	Content
JN-RD-6015	JN5148 Module Reference Design Package	DR1111 Standard-Power PCB Antenna module DR1110 Standard-Power uFL module DR1112 High -Power uFL

1.1 Pinout

Pin	Signal	Primary Function	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4
1	DIO16	DIO16	RXD1	IP_DI	JTAG_TDI	
2	DIO17	DIO17	CTS1	IP_SEL	DAI_SCK	JTAG_TCK
3	VSS3	GND	-	-	-	-
4	DIO18	DIO18	RTS1	IP-INT	DAI_SDOUT	JTAG_TMS
5	DIO19	DIO19	TXD1	-	-	JTAG_TDO
6	VSS2	GND	-	-	-	-
7	VSSS	GND	-	-	-	-
8	XTAL_OUT	OSC	-	-	-	-
9	XTAL_IN	OSC	-	-	-	-
10	VB_SYNTH	REG	-	-	-	-
11	VCOTUNE	VCOTUNE	-	-	-	-
12	VB_VCO	REG 1V8	-	-	-	-
13	VDD1	SUP 3V3	-	-	-	-
14	IBIAS	BIAS 1V8	-	-	-	-
15	VREF	REF 1V8	-	-	-	-
16	VB_RF2	REG 1V8	-	-	-	-
17	RF_IN	ANT CON	-	-	-	-
18	VB_RF	REG 1V8	-	-	-	-
19	COMP1M	COMP1M	EXT_PA_B	-	-	-
20	COMP1P	COMP1P	EXT_PA_C	-	-	-
21	ADC1	ADC	-	-	-	-
22	ADC2	ADC	-	-	-	-
23	ADC3	ADC	-	-	-	-
24	ACD4	ADC	-	-	-	-
25	COMP2M	COMP2M	-	-	-	-
26	COMP2P	COMP2P	-	-	-	-
27	VB_A	REG 1V8	-	-	-	-

Pin	Signal	Function	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4
28	NC	-	-	-	-	-
29	DAC1	DAC OUT	-	-	-	-
30	DAC2	DAC OUT	-	-	-	-
31	DIO20	DIO	RXD1			JTAG_TDI
32	VSS1	GND	-	-	-	-
33	SPICLK	CLK OUT	-	-	-	-
34	SPIMISO	MISO	-	-	-	-
35	VB_RAM	REG 1V8	-	-	-	-
36	SPIMOSI	MOSI	-	-	-	-
37	SPISEL0	SLAVE SEL 0	-	-	-	-
38	DIO0	DIO	SPISEL1	-	-	-
39	RESETN	RESET	-	-	-	-
40	VB_DIG	RED 1V8	-	-	-	-
41	DIO1	DIO	SPISEL2	PC0	-	-
42	DIO2	DIO	SPISEL3	RFRX	-	-
43	DIO3	DIO	SPISEL4	RFTX	-	-
44	DIO4	DIO	CTS0	-	-	JTAG_TCK
45	DIO5	DIO	RTS0	-	-	JTAG_TMS
46	DIO6	DIO	TXD0	-	-	JTAG_TDO
47	DIO7	DIO	RXD0	-	-	JTAG_TDI
48	DIO8	DIO	TIM0CK_GT	PC1	-	-
49	VDD2	SUP 3V3	-	-	-	
50	DIO9	DIO	TIM0CAP	32KXTALIN	32KIN	-
51	DIO10	DIO	TIM0OUT	32KXTALOUT	-	-
52	DIO11	DIO	TIM1CK_GT	TIM2OUT	-	-
53	DIO12	DIO	TIM1CAP	ADO	DAI_WS	-
54	DIO13	DIO	TIM1OUT	ADE	DAI_SDIN	
55	DIO14	DIO	SIF_CLK	IP_CLK		
56	DIO15	DIO	SIF_D	IP_DO		

57	VSSA	GND	PADDLE	-	-	-

Note: For more detailed descriptions of the pin functions, please refer to the latest chip datasheet: JN-DS-JN5148.

1.2 Minimum Connection Requirements

The following connection requirements should be met:

- The module should be powered with V_{cc} between 2.3 and 3.6 volts.
- The GND and VSSA signals should be connected together and preferably onto the ground plane of the module motherboard.
- A decoupling ceramic capacitor of 100 nF should be placed between VCC and GND.
- SSZ and SSM should be tied directly together. This allows the SPI Select signal from the device to communicate with the Flash memory. This connection is not made on the module itself, in order to provide a way of booting from an external Flash device (useful when production testing modules) or to enable the on-board Flash device to be programmed directly via the SPI port.
- To reset the module, the reset circuit shown below in Figure 1 should be applied. If necessary, a switch can be applied between RESETN and GROUND.

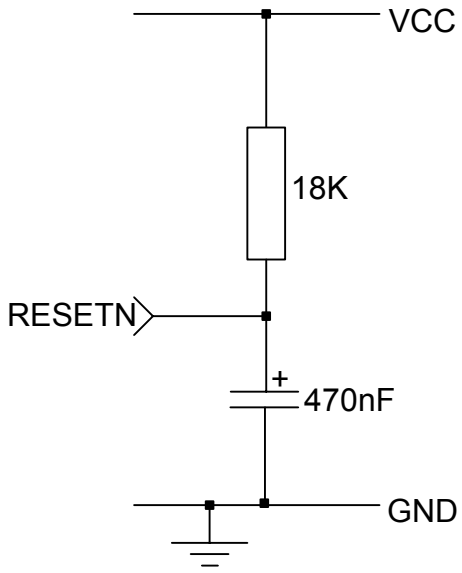

Figure 1: Recommended Reset Circuit

If programming of the Flash device is required, tie the SWP signal to VCC. Otherwise, to stop the Flash memory from being accidentally programmed, tie the SWP signal on the device to ground. It is also necessary to enable the Flash write-protect pin within the Flash device itself via software.

1.3 Entering Programming Mode

To put the module into programming mode, tie MISO to 0V while releasing RESET. This causes the device to read zeros back from the Flash memory during initialisation and, as a result, to enter programming mode. If you are using the module in conjunction with a serial dongle then the signal PGM is available to put the device into programming mode. To allow this signal to operate correctly from the Flash programming software, the signal should be connected to the module as shown below in Figure 2.

Figure 2: PGM Connection to the Module

To allow the Flash memory to be programmed, the SWP signal on the device should be tied to VCC.

1.4 PCB Decal

The PCB Decal can be found in the JN5148 datasheet: JN-DS-JN5148.

1.5 Screening Can

The module designs presented in the Module Reference Design JN-RD-6015 were devised to meet the requirements of FCC Part 15 and ETSI 300 – 328, when used with the screening cans shown below (in Figure 4).

1.5.1 Standard Power Module

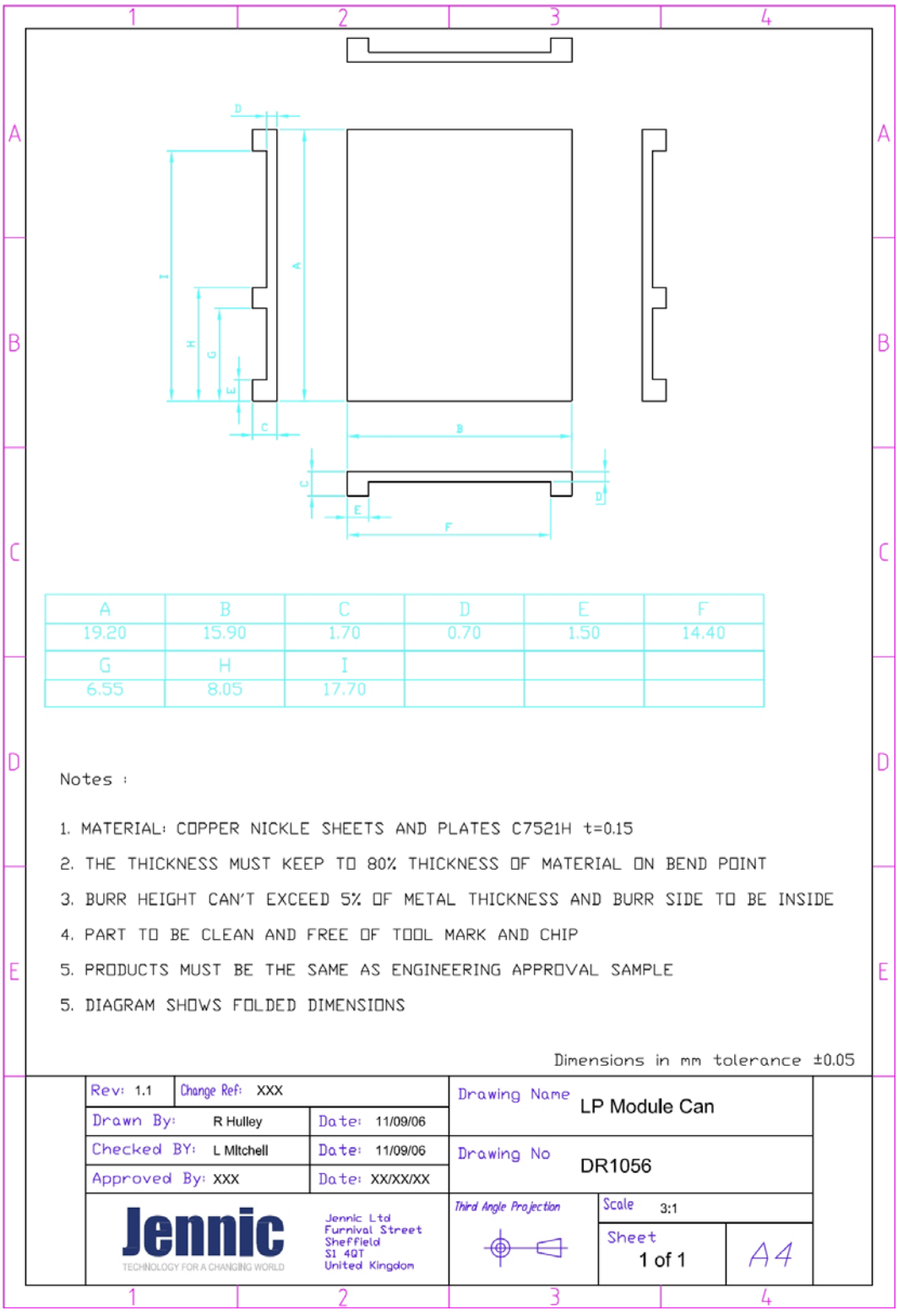

Figure 4: Standard Power Screening Can Drawing

1.5.2 High-Power Module

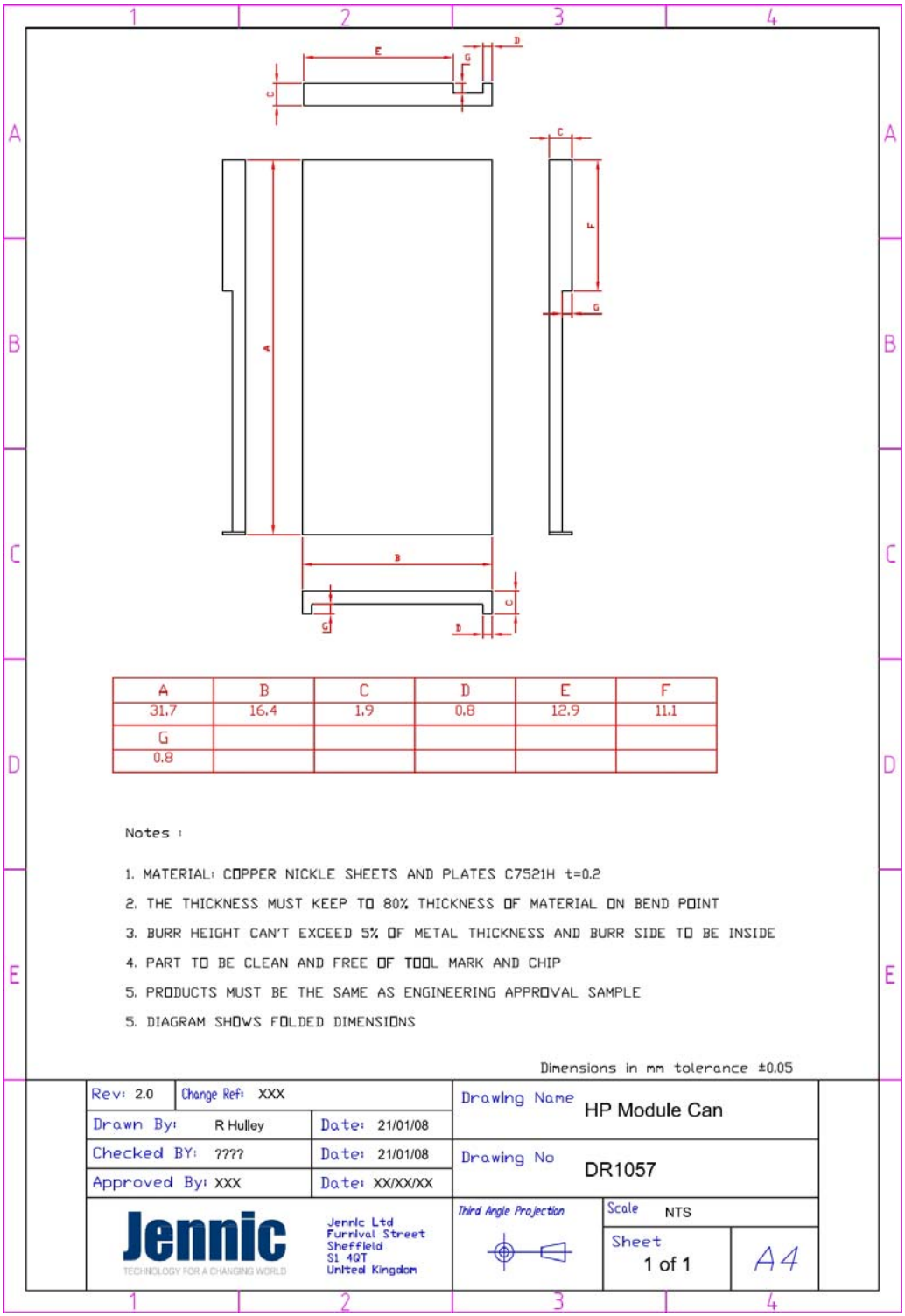

Figure 5: High-Power Module Screening Can Drawing

2 Design Considerations

2.1 PCB Requirements

2.1.1 Common Features: High- and Standard-Power Modules

From top to bottom, the layers are:

- Component
- Ground
- Digital tracks
- Power and tracks

The material is standard FR4.

While no special measures are required for the board design, it is recommended that Class 1 tolerances be used. Special attention should be paid to the input/output pads formed from half PTH vias. Figure 6 shows how to form the edge connectors correctly by cutting at the board edge profile line indicated. This board profile may be found on the upper paste mask layer on the DR1110, DR1111 and DR1112 gerbers provided in the design package. The pads are extended on the underside of the module to provide good solderability during reflow operations.

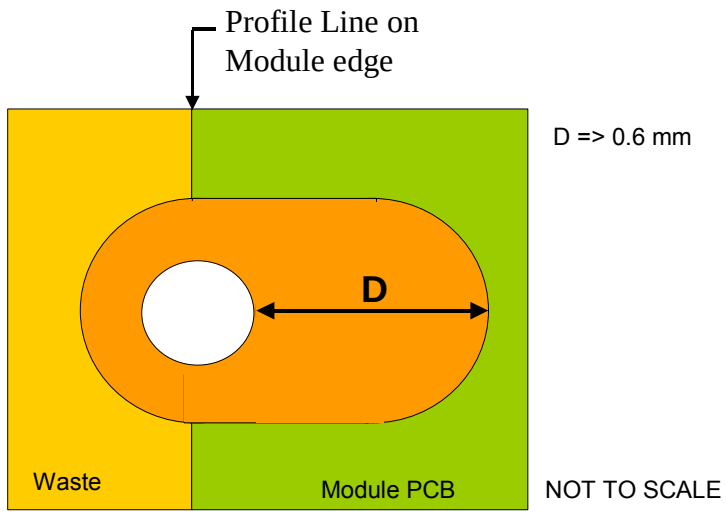

Figure 6: Edge Connector Details

2.1.2 Standard Modules – PCB Stack-Up

DR1110 and DR1111 are built on a standard 4–layer printed circuit board with the individual layers organised as shown below in Figure 7.

Top Copper - 0.7 mil - 0.018 mm - 1/2 oz
Pre-Preg - 2 x 2116 - 9 mil - 0.2286 mm
Layer 2 Copper - 0.7 mil - 0.018 mm - 1/2 oz
Core - 3 x 7628 - 20 mil - 0.51 mm
Layer 3 Copper - 0.7 mil - 0.018 mm - 1/2 oz
Pre-Preg - 2 x 2116 - 9 mil - 0.2286 mm
Layer 4 Copper - 0.7 mil - 0.018 mm - 1/2 oz

Figure 7: Standard Power Modules PCB Stack-Up

Note: The Jennic PCB layout assumes the layers defined above. If a different PCB stack-up is used then the RF track thickness and layout will need to be re-assessed.

2.1.3 High-Power Module – PCB Stack-Up

DR1112 is built on a standard 4–layer printed circuit board with the individual layers organised as shown below in Figure 8.

Top Copper - 0.7 mil - 0.018 mm - 1/2 oz
Pre-Preg - 1 x 2116 - 4.5 mil - 0.1143 mm
Layer 2 Copper - 0.14 mil - 0.036 mm - 1 oz
Core - 4 x 7628 - 27 mil - 0.68 mm
Layer 3 Copper - 0.14 mil - 0.036 mm - 1 oz
Pre-Preg - 1 x 2116 - 4.5 mil - 0.1143 mm
Layer 4 Copper - 0.7 mil - 0.018 mm - 1/2 oz

Figure 8: High-Power Module PCB Stack-Up

2.2 Supply Decoupling

The main decoupling capacitor (C13) has been placed as close as possible to the feed point.

C14 is the decoupling capacitor for the analogue areas of U1. It is placed as close as possible to the U1 pin VDD1.

C16 is the decoupling capacitor for the digital areas of U1. It is also used to decouple the supply on the Flash memory due to:

- placement of the Flash memory power pin (U2 Pin 8) next to the U1 Pin VDD2
- the fact that the Flash memory is only used during booting (unless reprogramming), so the RF areas of the device are not active.

2.3 Reference Oscillator

2.3.1 Reference Oscillator Requirements

The Jennic JN5148 device contains the necessary on-chip components to build a 32-MHz reference oscillator with the addition of an external crystal resonator. The DR1110 and DR1111 module schematics show the crystal circuit in the form of capacitors C10[1], C11[2] together with a crystal resonator Y1.

The reference crystal serves many purposes, including the provision of a reference for the 32-bit RISC processor, PHY controller, radio synthesiser and analogue peripherals. In addition, the crystal provides timing references for external I/O (e.g. on-chip UARTs) and timer counters. Thus, it is important that the crystal reference is specified and built correctly to ensure that the system functions properly.

The schematics show the external crystal resonator, Y1, connected to U1 via two coupling capacitors which, for the crystal chosen here, should be 15 pF ±5% and use a C0G dielectric. This is important, in order to ensure that the oscillator Q-factor and temperature stability are maximised.

The choice of crystal resonator is important for the following reasons:

- **Resonator tolerance:** A number of parameters, ranging from on-chip timings to radio centre-frequency, are derived directly from the tolerance of the crystal. As indicated in the component list, we recommend that a total tolerance of less than ±35 ppm is used, as the maximum permissible offset specified in IEEE 802.15.4 is ±40 ppm. Also, note that this tolerance should include both temperature and ageing effects imparted on the resonator.
- **Resonator load capacitance:** The active oscillator components on the JN5148 are designed for a crystal resonator with load capacitance of 9 pF. This is a standard loading and resonators of this type are widely available.

> **!** ***Caution****: Adherence to Jennic's recommendations will ensure that the module performs correctly. The substitution of components is not recommended, as this may lead to both oscillator start-up and frequency tolerance issues.*

[1] C21 on DR1112 High-Power Module

[2] C22 on DR1112 High-Power Module

2.3.2 Specific Layout Considerations

The layout of the oscillator circuit is such that the components are close together. This improves the performance of the oscillator by reducing parasitic impedance and the likelihood of cross-talk.

We also recommend that the symmetry of layout be maximised in order to avoid uneven loading of the crystal resonator.

2.4 RF Layout

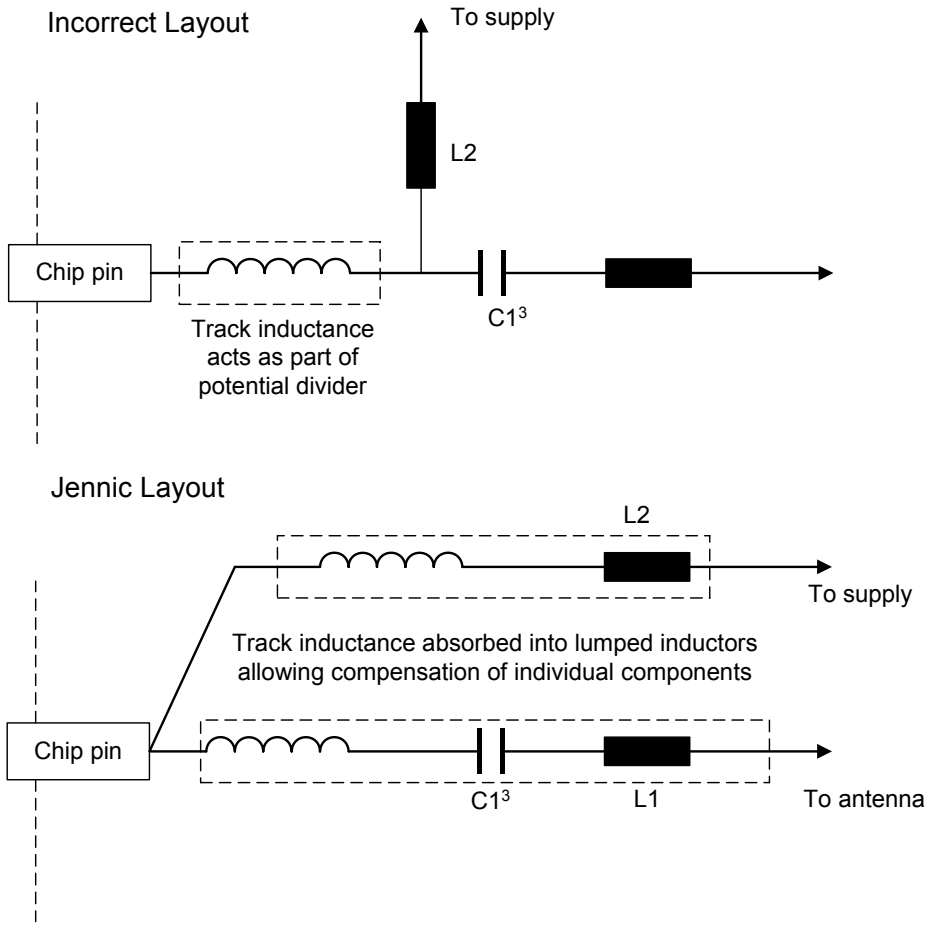

Figure 9: RF Layout Considerations

The separation of the PCB tracks to C1 and L2 is important so that the track inductance of the PCB can be compensated for. In the case of the Jennic layout, each component has an independent feed which allows the track inductance to be absorbed into L1 and L2. The total series inductance of each component can then be adjusted to an optimal value. When the approach used in the top layout is adopted, the components may not be optimised in this way, which results in a reduction of output power and a potential increase in spurious emissions.[3]

[3] C19 on DR1112 High-Power Module

2.5 Antenna Feed

The value of L1 has been chosen to match a 50-Ω impedance and therefore it is important that this impedance is controlled. This will ensure maximum power transfer to the antenna and minimum radiation from the track itself.

2.6 Other Layout Requirements

Component Designator	Value/Type	Function	PCB Layout Constraints
C13	10uF	Power source decoupling	
C14	100nF	Digital Power decoupling	Adjacent to U1 pin 13 (VDD1)
C16	100nF	Analogue power decoupling	Adjacent to U1 pin 49 (VDD2)
C15	100nF	VB Synth decoupling	As close as possible to U1 pin 10
C18	47pF	VB Synth decoupling	As close as possible to U1 pin 10
C2	100nF	VB VCO decoupling	As close as possible to U1 pin 12
C24	47pF	VB VCO decoupling	As close as possible to U1 pin 12
C3	100nF	VB RF decoupling	As close as possible to U1 pin 16 and U1 pin 18
C12	47pF	VB RF decoupling	As close as possible to U1 pin 16 and U1 pin 18
C8	100nF	VB A decoupling	As close as possible to U1 pin 27
C9	47pF	VB A decoupling	As close as possible to U1 pin 27
C6	100nF	VB RAM decoupling	As close as possible to U1 pin 35
C7	100nF	VB Dig decoupling	As close as possible to U1 pin 40
R1	43k	IBias Resistor	As close as possible to U1 pin 14
C20	100nF	Vref decoupling	As close as possible to U1 pin 15
Y1	32MHz	System Crystal Resonator	As close as possible to pin 8 and 9
C10	12pF +/-5% C0G	Crystal Load Capacitor	Adjacent to pin 8 and Y1 pin 1
C11	12pF +/-5% C0G	Crystal Load Capacitor	Adjacent to pin 9 and Y1 pin 3
C1	47pF	DC Block / AC short	Position and track lengths must be copied directly from the reference design.
L1	5.6nH	RF Matching component	
L2	2.7nH	RF Matching component	

Table 1: Layout requirements (Component References for DR1110, DR1111)

Table 1 details important layout considerations. This reference design has implemented the above guidelines - if the design is copied exactly then these criteria will be met.

Note: The layout of the external radio connections and associated power supplies are very important. In this respect, the tolerances indicated in Figure 7 and Figure 8 are particularly important.

2.7 Ground Planes

The module has been designed for four layers. This allows the best use of the ground planes. The following restrictions were placed on the layout:

- All RF signals are confined to the top layer.
- The second layer is Ground and has no tracks on it. This allows the best return path for all RF signals and will ensure optimum EMC performance.
- The bottom layer contains all other signals and the V_{cc} power supply for the module.
- In the case of DR1111, the ground planes on all layers stop BEFORE the antenna, so that the performance of the antenna is not affected. The recommended antenna clearance for the PCB antenna is shown in Figure 10 below. Note that this clearance should be maintained when mounting the module on a motherboard.

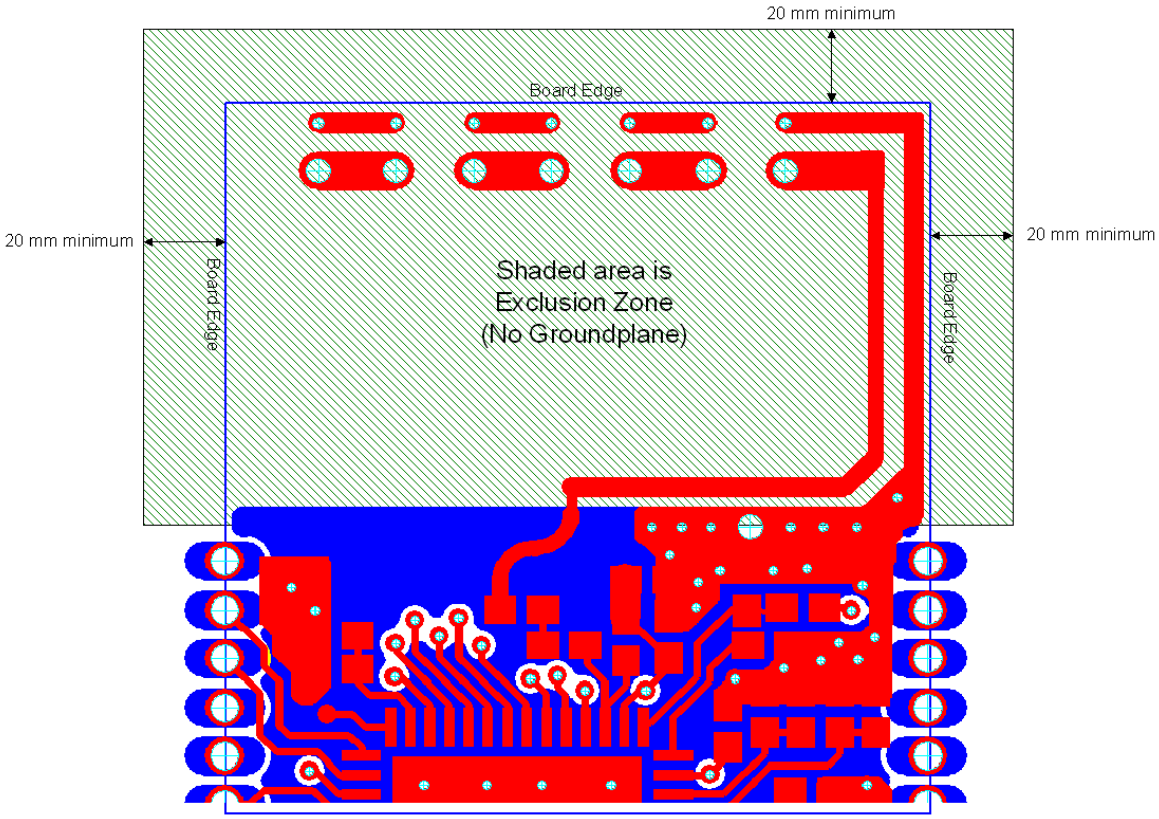

Figure 10: Antenna Clearance Recommendations

- The schematics contain six pads, labelled ‘screen lug’. These pads are located in the four corners of the board determined by the corner of the ground plane. One additional pad is located down each side of the module. These allow the metal screening cans in Figure 4 and Figure 5 to be connected on to the module.

2.8 Manufacturing Considerations

The TQFN package must be considered carefully when using reflow solder techniques. The following are recommendations:

- The decal is shown in Figure 11. The pad stacks used are 0.25 mm by 1 mm for the smaller pads, and a 6.4-mm square pad for the paddle.

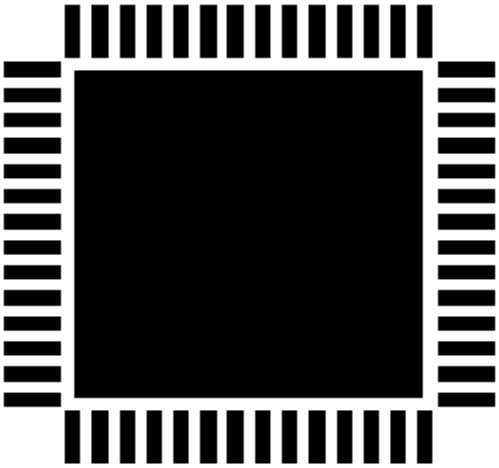

Figure 11: Recommended PCB Decal for 56TQFN Package

- The solder mask used is shown in Figure 12. The pad stacks used are 0.25 mm by 1 mm for the smaller pads, and four 2.5-mm square pads to apply paste to the paddle. The solder paste mask has a thickness of 6-thou (0.152 mm). If the paste thickness needs to deviate from that used by Jennic then it may be necessary to change the number of pads that the paste is applied to. Paste thickness may be dictated by other components used in a design.

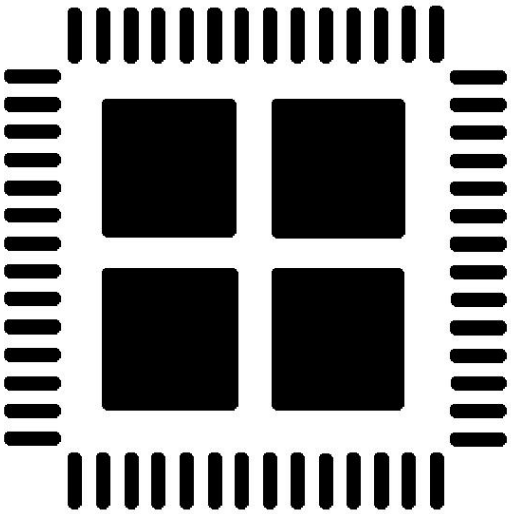

Figure 12: Recommended Solder Paste Mask for 56TQFN Package

- Sixteen vias are applied to the paddle. These allow excess solder paste and heated air to be vented away from the device, preventing the device from being lifted during soldering. In addition, these vias ensure that a low impedance ground is maintained, which is vital for optimum RF performance.

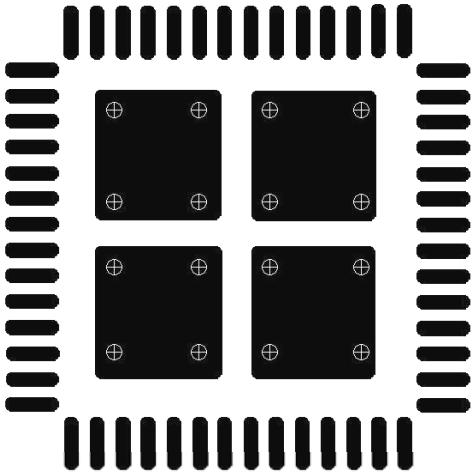

Figure 13: Vias on the Paddle of the 56TQFN Package

3 Bespoke Solutions - Design Considerations

3.1 PCB Layout Issues

The list presented below provides some key suggestions when using a wireless microcontroller on a bespoke, multi-layer PCB. Clearly, the list is not exhaustive and you may have more detailed considerations in using mixed-signal integrated circuits.

- **Shared vias**: Often in layout, it is convenient for a number of components to share a return to Analogue Ground. Examples include bypass capacitors and reference setting resistors. We recommend that all components be given a separate via to Ground. This avoids noise feed-through and poor isolation issues that often occur when vias are shared.
- **Oscillator circuit**: We recommend that tracks from the oscillator pins are kept to the same length and, ideally, on the top layer. This avoids asymmetrical loading of the crystal resonator. The placement of the two capacitors should be symmetrical to the crystal. This also avoids asymmetrical loading of the reference oscillator.

3.2 Decoupling Capacitors

Three decoupling capacitors should be used:

- Two ceramic 100-nF capacitors - one should be placed close to pin VDD1, the other should be placed close to pin VDD2
- One 10-µF multi-layer ceramic capacitor connected to Ground - if the PCB is a module then place this capacitor close to the point where the power enters the module.

3.3 IBIAS

A 43-kΩ resistor should be connected as close as possible to the IBIAS pin.

3.4 EMC

For good EMC performance, it is necessary to minimise any ground loops when laying out the PCB. This is achieved by having an uninterrupted ground plane on layer 2 and keeping all ground paths as short as possible.

The stack-up should be similar to those provided in the design guides. It is important that all controlled impedances are adhered to.

Individual vias for each component should be used whenever possible. It is also advisable to fit a screening can.

Revision History

Version	Date	Description
1.0	09-June-2009	First release

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