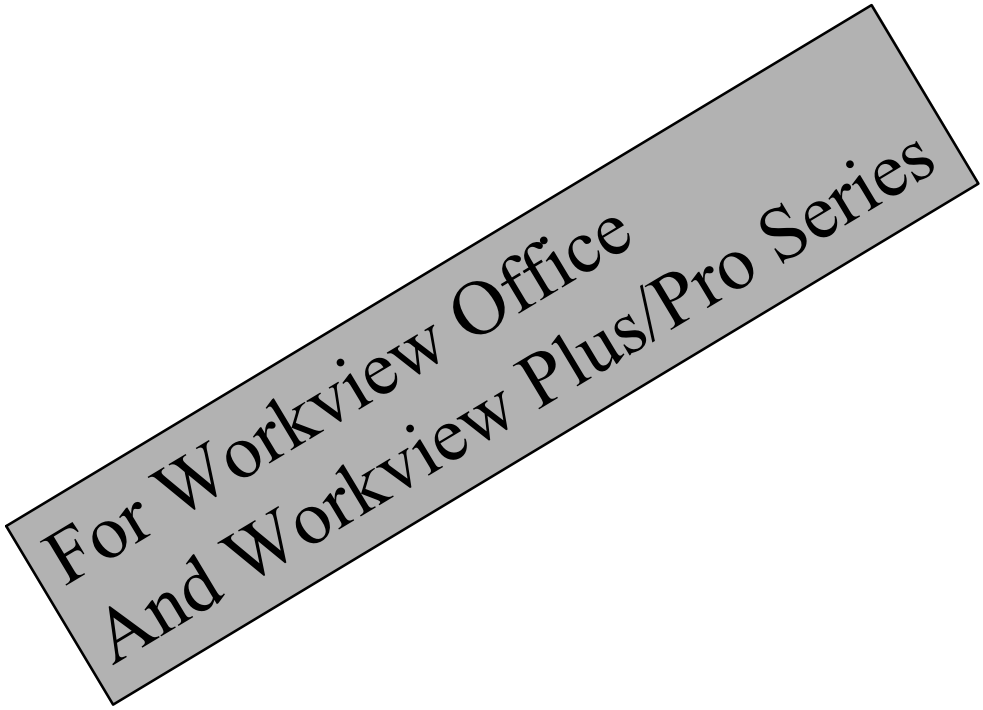
QUICKLOGIC

QuickLogic -Viewlogic Interface User's Guide

Revision 6.0, November 1996



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Workview Plus/Pro Series Interface (Chapter 7 and Chapter 8)

Chapter 1 - Introduction

Welcome to QuickLogic's Viewlogic Design Interface for the PC environment. This interface allows you to use your existing Viewlogic software to easily design QuickLogic devices.

Viewlogic schematic capture, synthesis and simulation are fully supported, as well as full integration into the SpDE environment for automatic placement and routing, static timing analysis, post-layout delay modeling and back annotation, ATVG, device programming and device checking.

This manual is divided into two independent sections. Chapters 2 through 6 cover all the technical information relative to the Workview Office interface while Chapter 7 and 8 are dedicated to Workview Plus/Pro Series.

This manual contains information specifically for Viewlogic users. Please refer to the QuickTools or QuickWorks User's Guide for information about other aspects of the SpDE environment.


For Workview Office Interface

Chapter 2 - Software Installation

Before installing the QuickLogic-Viewlogic Interface software, make sure that both Viewlogic's Workview Office and QuickTools (or QuickWorks) are installed. For instructions on installing Workview Office, refer to the Viewlogic documentation. For instructions on installing QuickTools or QuickWorks, refer to Chapter 1 in their respective user's guides.

System Requirements

- QuickTools (or QuickWorks) version 6.1 or higher
- Workview Office version 7.2 or higher
- Operating systems: Windows NT or Windows 95

Installation Instructions

Insert the QuickLogic-Viewlogic Interface (for Workview Office) disk and run the INSTALL program. Note that the executable, INSTALL.BAT, is a DOS program which runs at the command line. If C:\WVOFFICE and C:\PASIC\SPDE are the existing directories for Workview Office and QuickLogic's SpDE, respectively, then the installation will proceed automatically and it will place the interface files under a default directory called C:\QUICK. Otherwise, the directory paths can be specified at the command line.

A typical installation on the command line is as follows:

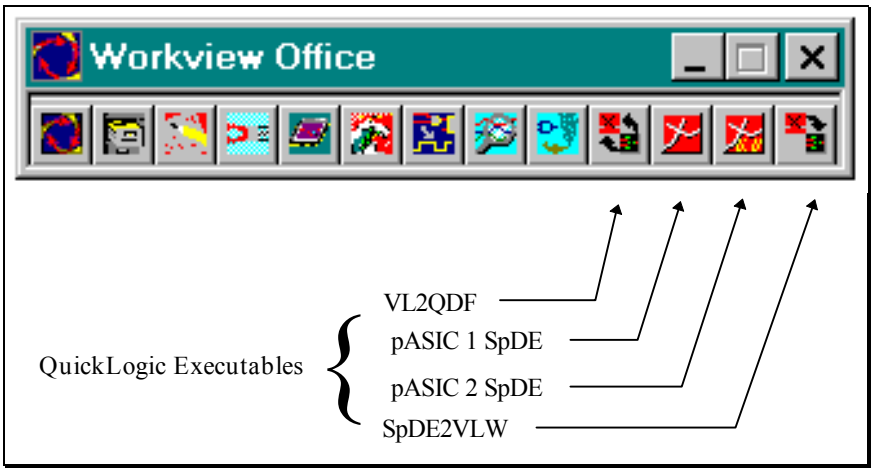
```
INSTALL  C:\QUICKLIB  C:\WVOFFICE  C:\PASIC\SPDE
```

where QUICKLIB is the directory for the QuickLogic libraries, WVOFFICE is the main Workview Office directory and SPDE is where the QuickLogic place and route tools are located.

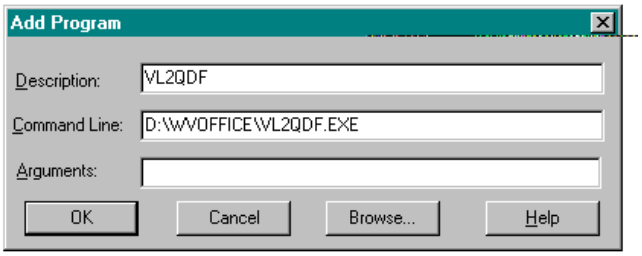
If neither QuickTools nor QuickWorks is installed on your PC, you may leave the "SpDE directory" blank on the command line for INSTALL. You will get the message WARNING: default path C:\PASIC\SPDE forQuickLogic does not exist. Press any key to continue with installation… Ignore it!

QuickLogic Icons in Toolbar

If the install program finds the Workview Office and SpDE directories, then it automatically appends the QuickLogic icons to the Viewlogic toolbar. After installation the Workview Office toolbar may look like the figure shown below.



If for any reason the QuickLogic icons were not automatically installed, they can be added manually. The icons for "VL2QDF", "pASIC 1 SpDE", "pASIC 2 SpDE", and "SpDE2VLW" should be included in the Workview Office toolbar. Click on the "Workview Office" icon and then execute the Add→Program...command. You will see a dialog box as shown below. Note that the QuickLogic-Viewlogic Interface executables, VL2QDF.EXE and SPDE2VLW.EXE are installed into the WVOFFICE directory. SPDE1.EXE and SPDE2.EXE are in the PASIC\SPDE directory.



Setting Up a Design Project

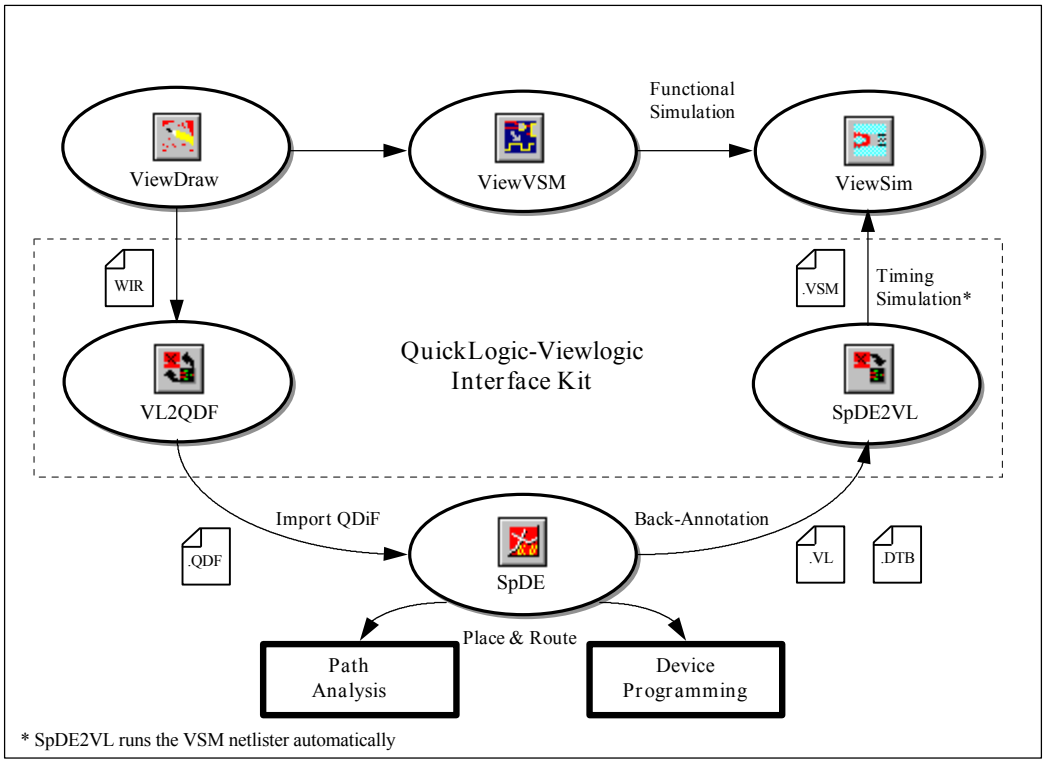
In order to utilize the QuickLogic Macro Library symbols, you must ensure the VIEWDRAW.INI file for the project contains the appropriate search paths. Invoke the Project Manager and execute File→New to clear the existing libraries. Use the "Browse" button to select a new Primary Directory. After doing so, run Project→Import Existing Searchorder and find the VIEWDRAW.INI file installed in the QuickLogic libraries directory (e.g. C:\QUICKLIB\VIEWDRAW.INI). Save the project file.

Chapter 3 - Getting Started

Schematic Design Flow

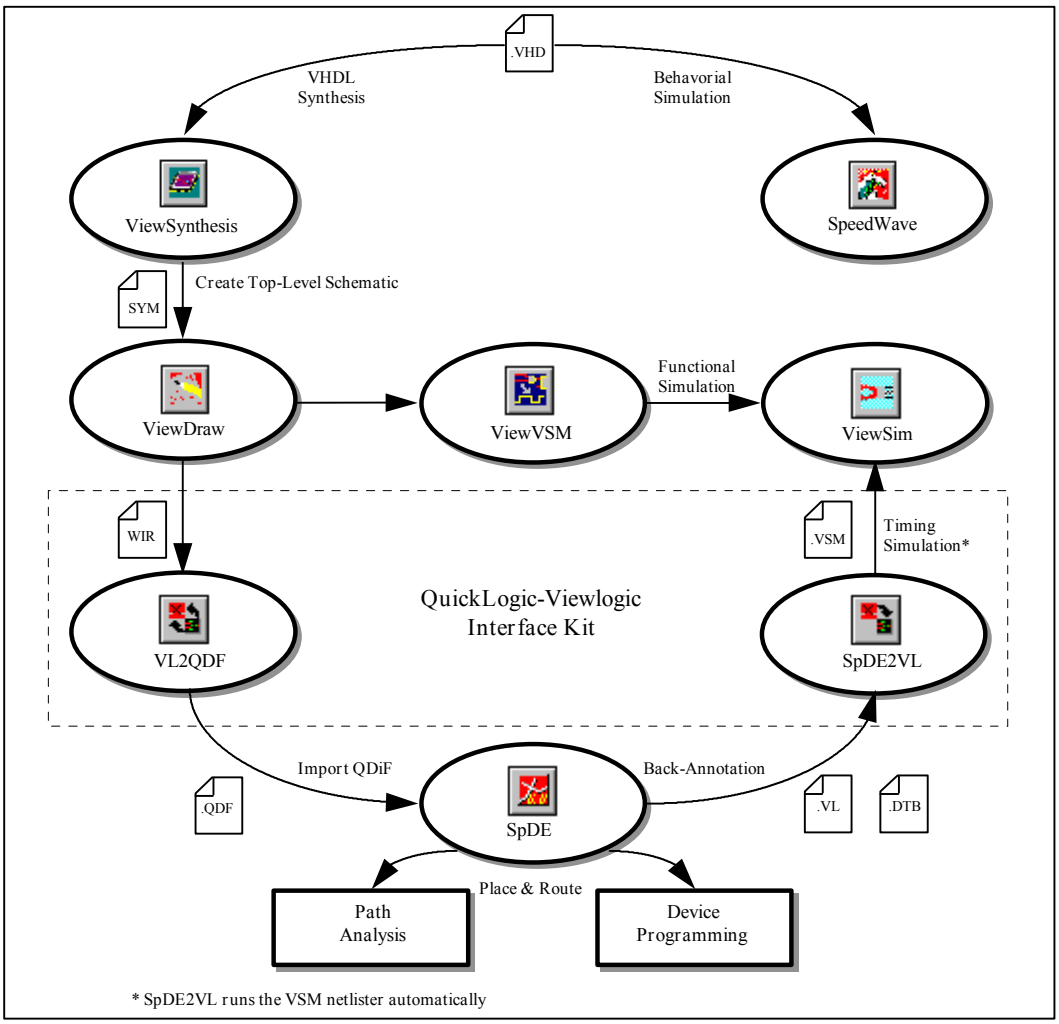
The diagram below shows a typical schematic design flow. Schematics are drawn with QuickLogic macros (installed by the interface kit) using ViewDraw. Then QuickLogic's VL2QDF netlist translator converts your Viewlogic design from the WIR format to QuickLogic's QDF. The QDF is then imported into SpDE (from QuickTools or QuickWorks) for FPGA "Place and Route". SpDE is actually more than just a place and route tool. It also performs logic optimization based on your design requirements for speed or area. Other special features include auto-buffering, timing-driven placement, and (static timing) path analyzer.

Since SpDE has post-layout simulation support for many 3rd-party simulators, make sure that ViewSim is specified as the simulator for "Back Annotation". The back annotation tool will then generate the simulation files with extensions .VL and .DTB. The QuickLogic SpDE2VL is used to take the post-layout design back in the Viewlogic environment ready for simulation using ViewSim.



VHDL Design Flow

The VHDL design flow is very similar to the schematic design flow with the exception of the added procedure using ViewSynthesis for VHDL compilation. Regardless of whether the Viewlogic design is entered only in VHDL or in mixed VHDL/schematics, the top-level must be a schematic done in ViewDraw. Since automatic pad insertion is not supported by ViewSynthesis, a VHDL-only design must be placed as a symbol in a top-level schematic. Appropriate QuickLogic pad symbols are then attached to the symbol representing the VHDL design. From this point on, the design flow is identical to the schematic design flow. Please refer to the previous section for further discussion on using the QuickLogic-Interface Kit and SpDE with the Workview Office environment.



Chapter 4 - Design Procedures

QuickLogic Schematic Macros

Viewlogic schematic designs targeted for QuickLogic devices must be entered using symbols from macro libraries installed by the interface kit. These macros range from simple pads and combinational gates to more complex functions like adders and multipliers.

The macros are categorized logically by their types such as "AND", "FF", and "ADDER". However, there are other categories of macros which may require some explanation. The "PAD" type macros are important because every (including VHDL) design requires them. Pads are required for all the (input, output, and bi-directional) ports of the top-level schematic. The "OTHER" category contains miscellaneous, but important, macros for inverter, buffer, and special functions. The "BUILTIN" library is actually part of the Viewlogic environment. This library provides functions such as "IN" and "OUT" markers or "VCC" and "GND" symbols. The "MCELL" library contains primitives used to create custom hard macros. For detailed information regarding the contents and usage of QuickLogic macros, refer to the User's Guide for QuickTools or QuickWorks.

Please note that symbols from the "PRIM" library must not be used in schematic designs.

pASIC 2 Macros

There are pASIC 2 specific macros such as INPADff, LOGIC2, and GCLKBUFF in the QuickLogic macro library. These symbols, indicated by "p2", can not be used in designs targeted for pASIC 1 devices. On the other hand, all other generic macros are supported for pASIC 1 or pASIC 2 designs. For details, refer to The pASIC 2-Specific Macros section in the Macro Library Reference chapter in the User's Guide for QuickTools or QuickWorks.

Custom Hard Macros

If you make your own custom hard macros from QuickLogic primitives (the MCELL library), you need to add an attribute "LEVEL" with the value "QMACRO" to the symbol properties.

> Note - The attribute LEVEL=QMACRO is required only when you create a symbol using the MCELL library only.

Device and Package Assignments

This can be accomplished in two ways: adding the "PART" and "PACKAGE" attributes to the schematic properties or let the VL2QDF program prompt you with the selections. The valid arguments for the PART and PACKAGE attributes are as follow:

PART

pASIC 1*			pASIC 2		
p8x12b	-	1000-gate FPGA	ql2005	-	5000-gate FPGA
p12x16b	-	2000-gate FPGA	ql2007	-	7000-gate FPGA
p16x24b	-	4000-gate FPGA	ql2009	-	9000-gate FPGA
p24x32b	-	8000-gate FPGA			

*NOTE: Each pASIC 1 device has a 3.3V equivalent. These low-power devices have part numbers that end with "BL". For example, the 3.3V version of the p8x12b has a p8x12bl device type.

PACKAGE

Plastic				Ceramic			
PL44	-	44-pin	PLCC	CF100	-	100-pin	CQFP
PL68	-	68-pin	PLCC	CF160	-	160-pin	CQFP
PL84	-	84-pin	PLCC	CF208	-	208-pin	CQFP
PF100	-	100-pin	TQFP	CG68	-	68-pin	CPGA
PF144	-	100-pin	TQFP	CG84	-	84-pin	CPGA
PQ208	-	208-pin	PQFP	CG144	-	144-pin	CPGA
PQ208	-	208-pin	PQFP				
PB256	-	256-pin	PBGA				

Valid combinations of PART and PACKAGE

p8x12b	-	PL44, PL68, CG68, PF100
p12x16b	-	PL68, PL84, CG84, PF100, CF100
p16x24b	-	PL84, PF100, PF144, CG144, CF160
p24x32b	-	PF144, PQ208, CF208
ql2005	-	PL84, PF144, PQ208
ql2007	-	PL84, PF144, PQ208
ql2009	-	PF144, PQ208, PB256

Fixing I/O Pad Locations

Change the pad symbol's attached attribute PLACE to the desired pin number. Consult the Pinout Diagrams in the Appendices in the User's Guide or QuickLogic's Data Book for proper pin locations for these cells. Example: PLACE=22.

> Note - It is not required that any pads be pre-placed. Those without placement information will be auto-assigned by SpDE.

Fixing Flip-Flop Locations

Change the flip flop symbol's attached attribute PLACE to the desired cell location. Example: PLACE=A1. The logic cell locations can be viewed by loading a .QDF or .CHP file for the appropriate QuickLogic device into SpDE.

Simulation Support

It is always possible to use any Viewlogic simulator to run pre-layout functional verifcation of schematic or VHDL designs. And post-layout timing simulation is fully supported for ViewSim. However, SpeedWave is not supported at this time. Please call the QuickLogic Hotline if you have any questions.

General Design Techniques

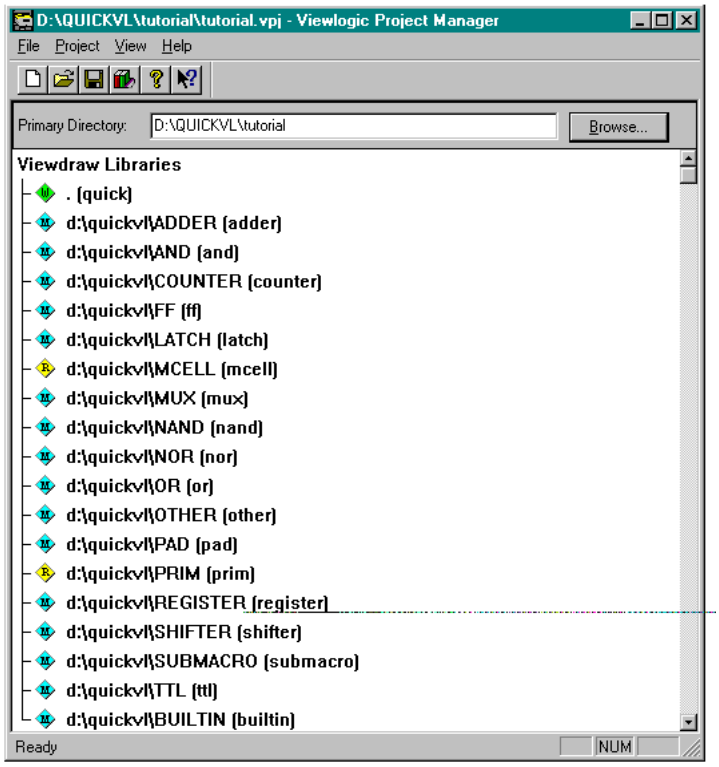
- Use only the QuickLogic macro library when designing with QuickLogic pASIC devices. Do not use any standard Viewlogic or other third party libraries. As an aid in this, it is recommended to remove any references to any other schematic libraries from the Viewdraw environment.
- The high drive input macros HD2PAD, HD3PAD, and HD4PAD are supported under Viewlogic for automatic placement only. If you need to fix the placement for one of these, use the non-bus HDPAD version. For high-speed drive recommendations based on fanout, see the Macro Library Reference chapter in the QuickTools or QuickWorks User's Guide.
- The macros INPADx, OUTPADx, TRIPADx, and BIPADx, where x is 4, 8, or 16, are supported for automatic placement only. If you need to fix the placement for one of these, use the non-bus version (INPAD, OUTPAD, TRIPAD, or BIPAD).

Chapter 5 - Schematic Tutorial

This tutorial is designed to quickly help you get started designing for pASIC devices using schematic entry. You will learn the steps required to complete a schematic design from adding QuickLogic macro symbols to simulating the design after place and route using SpDE. We assume the user is already familiar with the Workview Office tools (Project Manager, ViewDraw, ViewSim, etc.) The example is based on assumptions that the QuickLogic libraries are installed into a directory called D:\QUICKVL and Workview Office resides under the C:\WVOFFICE directory.

Setup Project Directory

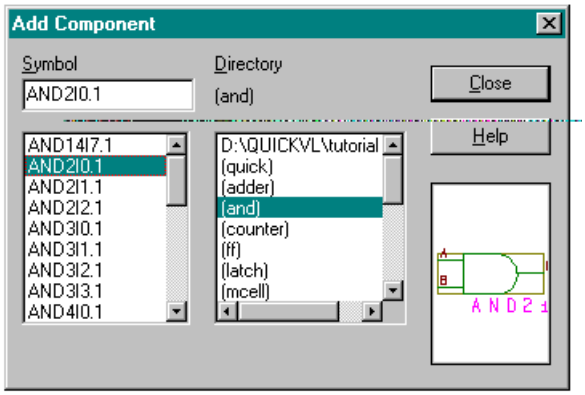
1. Invoke the Workview Office Project Manager.
2. Execute File→New and "Clear all libraries"
3. Use Browse… to change the Primary Directory to D:\QUICKVL\TUTORIAL
4. Run Project→Import ExistingSearchorder
5. Open the VIEWDRAW.INI file in the D:\QUICKVL directory.
   Your Project Manager window should be similar to the one shown below.



6. Run File→Save As and type "tutorial" as the filename.
7. Exit the Project Manager.

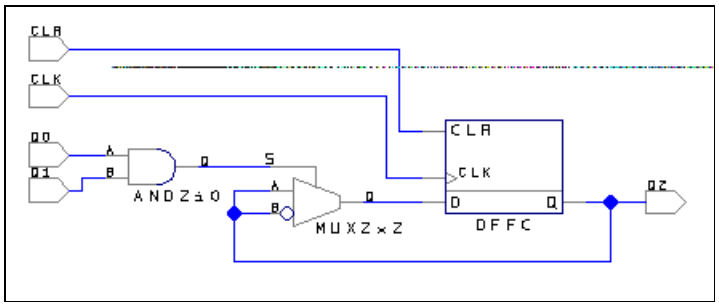
Schematic Entry

1. Launch the Workview Office Viewdraw.
2. Open a new schematic and name it "SBIT2".
3. Execute Add→Component.
4. Select the "[and]" directory from the middle window in the Add Component dialog box.
5. Place the "AND2i0" symbol onto the schematic. See figure below.



(Refer to the QuickTools or QuickWorks User's Guides for more information on the QuickLogic Macro Library.)

6. Pick and place the "MUX2x2" and "DFFC" symbols from the "[mux]" and "[ff]" directories, respectively.
7. Connect the symbols together as shown in the figure below.

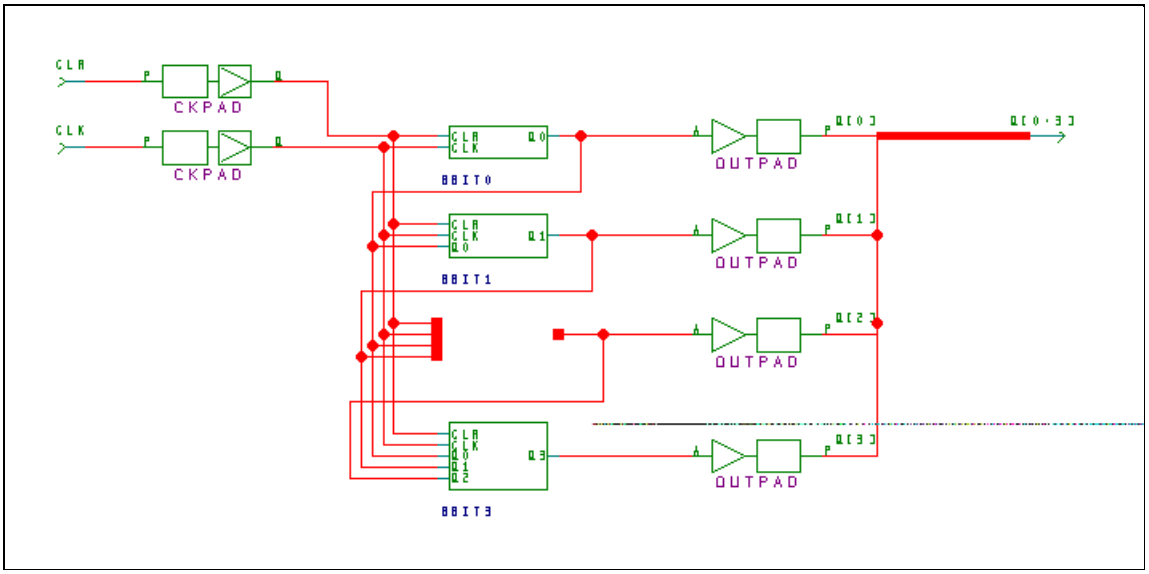


8. Execute Add→Component and locate the "IMARKER" symbol in the "[pad]" directory. Attach the "IMARKER" and "OMARKER" symbols to input and output nets, respectively.
9. Double-click to add the Labels (CLR, CLK, Q0, Q1, and Q2) to the I/O markers. (Note that we have not added I/O PADs to this schematic because this design will be used in the top-level schematic which will require I/O PADs for the external ports.)
10. Save and Check the design.

11. Normally, in doing a hierarchical design, the user will create (automatically using ViewGen) a symbol for the lower-level schematic. But to simplify this tutorial's design flow, we have already created the SBIT2 symbol for you.

Completing the Top-level Schematic

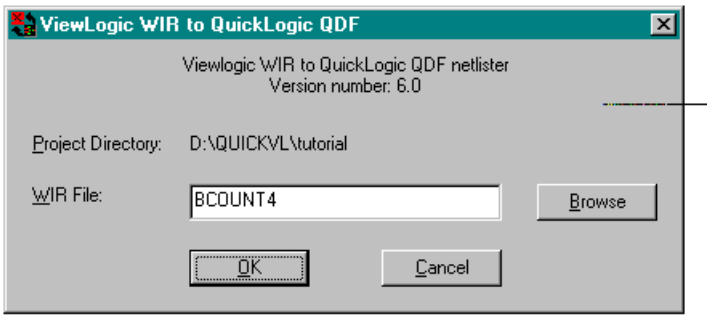
1. Open the schematic called BCOUNT4.
   (Notice there is a symbol missing in this schematic.)



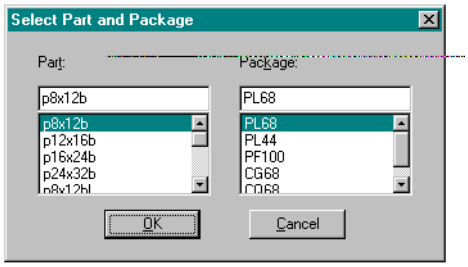
2. Complete the schematic by adding the SBIT2 symbol.
3. Save and check the design.

Converting Viewlogic WIR to QuickLogic QDF

1. Launch VL2QDF from the Workview Office toolbar or run VL2QDF.EXE directly from the WVOFFICE directory. Use the Browse button to select the BCOUNT4 WIR file.



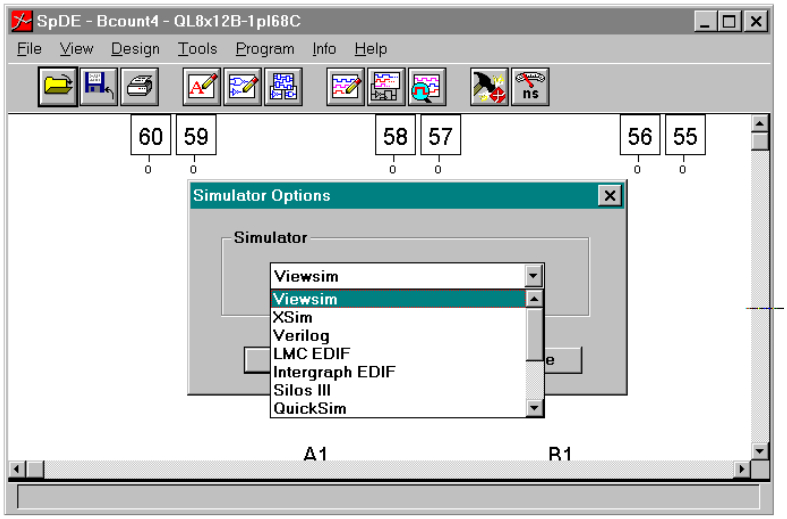
2. Set the "part" and "package" parameters to "p8x12b" and "PL68", respectively.



3. You are ready to import the design into QuickLogic's SpDE tools if there are no errors.

Place & Route UsingSpDE

1. Launch pASIC 1 SpDE from the Workview Office toolbar or run SPDE1.EXE directly from the SPDE directory.
2. Execute the File→Import→QDIF command and select the BCOUNT4.QDF file.
3. Before running the tools, you must specify Viewsim for post-layout simulation. From SpDE execute Tools→Options→Simulator… Choose "Viewsim" for simulator.



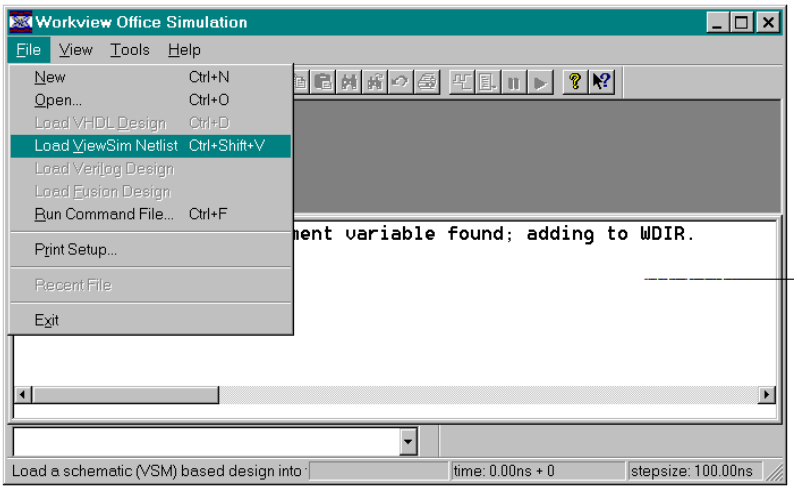
4. Execute Tools→Run Tools…and proceed with all options enabled. You will get a VL0000 Warning "Could not open file: c:\wvoffice\standard\vf\project.lst". Ignore it! After all the tools ran successfully, you may view the physical chip layout in the SpDE window. The files you'll need for Viewsim simulation are BCOUNT4.VL and BCOUNT4.DTB.

SpDE to Viewlogic VSM

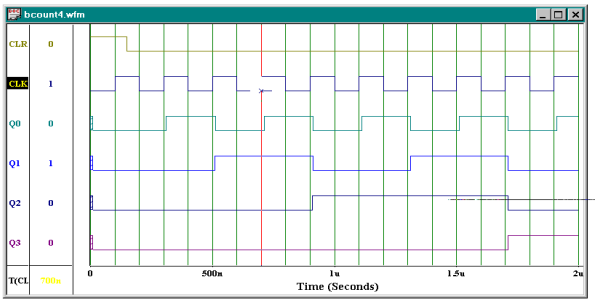
1. Launch SpDE2VLW from the Workview Office toolbar or run SPDE2VLW.EXE directly from the WVOFFICE directory.
2. Use Browse… to locate the BCOUNT4.VL file generate by SpDE's back annotation tool.
3. You will get the message WARNING: Output WIR file already exists Overwriting the WIR file will allow simulated values to appear in the schematic drawing. Otherwise, type in a new name for the output WIR file which will result in a VSM file of the same name. For this tutorial, allow the WIR to be overwritten.

Viewsim Simulation

1. Launch Viewsim from the Workview Office toolbar.
2. Execute File→Load ViewSim Netlist and select the BCOUNT4.VSM file.



3. Invoke File→Run Command Fileand select the BCOUNT4.CMD file.
4. ViewTrace will be launched automatically and the data from BCOUNT4.WFM will be displayed. As of the time of this writing, you will need run View→Full in order for the waveforms to be displayed properly.
5. Verify that the results match a four-bit binary up counter as shown below.

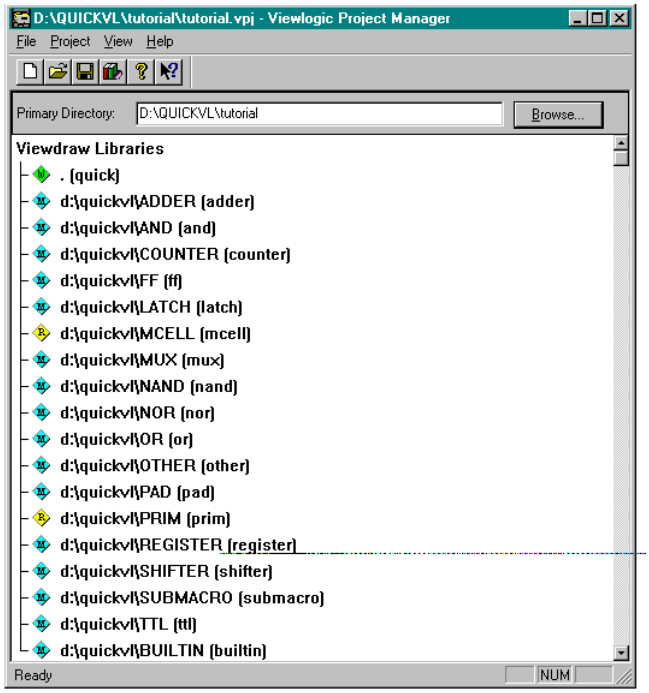


Chapter 6 - VHDL Tutorial

This chapter shows you how to easily get started designing for pASIC's using VHDL or mixed schematic-VHDL entry. This tutorial assumes the user is already familiar with the WVOFFICE Viewdraw schematic capture tool and ViewSynthesis VHDL compiler. This tutorial also assumes that the QuickLogic libraries are installed into a directory called D:\QUICKVL and Workview Office resides under the C:\WVOFFICE directory.

Setup Project Directory

1. Invoke the Workview Office Project Manager.
2. Execute File→New and click "OK" on "Clear all libraries"
3. Use Browse... to change the Primary Directory to D:\QUICKVL\STANDARD
4. Run Project→Import ExistingSearchorder
5. Open the VIEWDRAW.INI file in the D:\QUICKVL directory.
   Your Project Manager window should be similar to the one shown below.



6. Run File→Save As and type "tutorial" for the filename.
7. Exit the Project Manager.

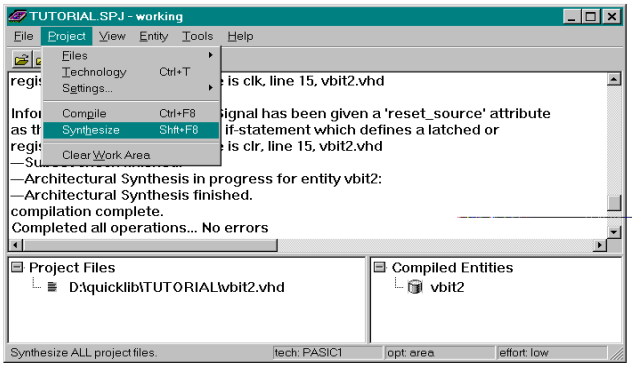
Entering the VHDL Code

1. Open a new text file and save it as VBIT2.VHD in the TUTORIAL directory.
2. Enter and save the source code shown below.

```
library ieee;
use ieee.std_logic_1164.all;

entity vbit2 is
  port( CLR : IN  std_logic;
        CLK : IN  std_logic;
        Q0  : IN  std_logic;
        Q1  : IN  std_logic;
        Q2  : OUT std_logic);
end vbit2;

architecture tutor of vbit2 is
signal Q2node : std_logic;
  begin

  process (CLR,CLK)
    begin
    if CLR = '1' then
      Q2node <= '0';
    elsif (CLK'event and CLK = '1') then
      Q2node <= Q2node xor (Q0 and Q1);
    end if;
  end process;

  Q2 <= Q2node;

end tutor;
```

ViewSynthesis Processing

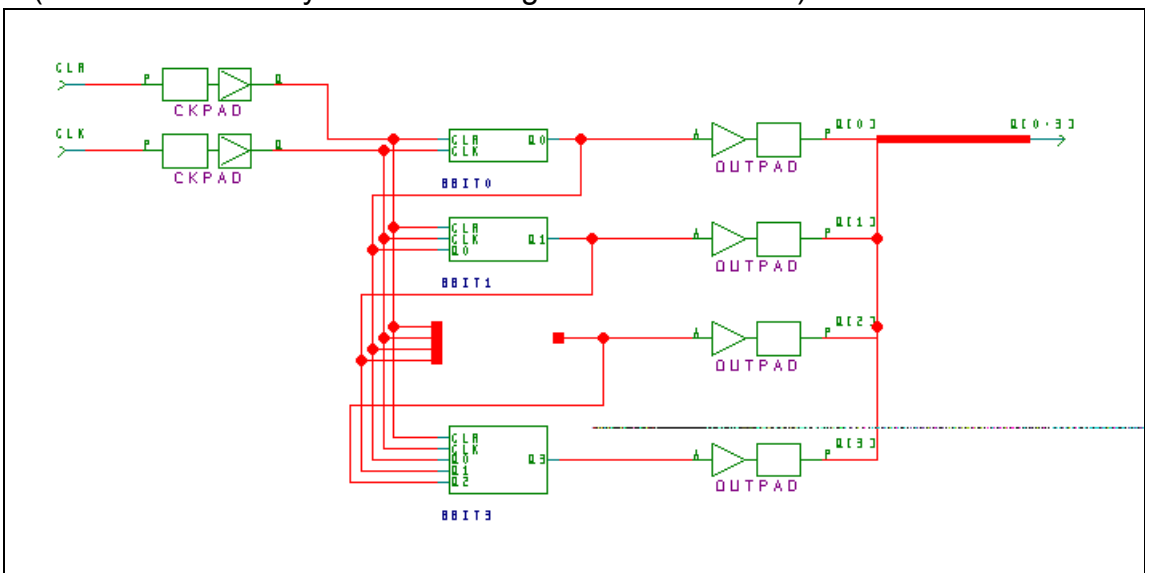
1. Invoke ViewSynthesis from the Workview Office toolbar.
2. Start a new project by running File→New and select "Project".
3. Execute File→Save As and name the project TUTORIAL.
4. Use Project→Files→Add to read in the VBIT2.VHD file you created.
5. Execute Project→Technology and choose "PASIC1" as the target.
6. Run Project→Compile to process the VHDL file.
7. Click on Project→Synthesize to map design into the pASIC technology.



8. Save file and exit ViewSynthesis.

Completing the Top-level Schematic

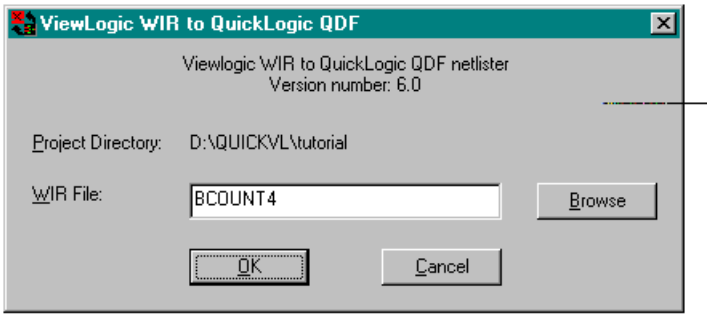
1. Open the schematic called BCOUNT4 (installed in the TUTORIAL directory). (Notice there is a symbol is missing in this schematic.)



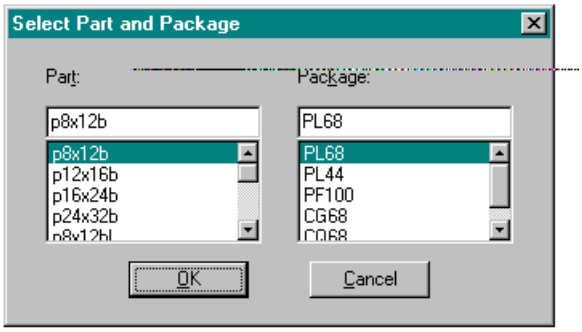
2. Complete the schematic by adding the VBIT2 symbol (provided).
3. Save and check the design.

Converting Viewlogic WIR to QuickLogic QDF

1. Launch VL2QDF from the Workview Office toolbar or run VL2QDF.EXE directly from the WVOFFICE directory. Use the Browse button to select the BCOUNT4 WIR file.



2. Set the "part" and "package" parameters to "p8x12b" and "PL68", respectively. Coincidentally, these are also the defaults.



3. You are ready to import the design into QuickLogic's SpDE tools if there are no errors.

Place & Route UsingSpDE

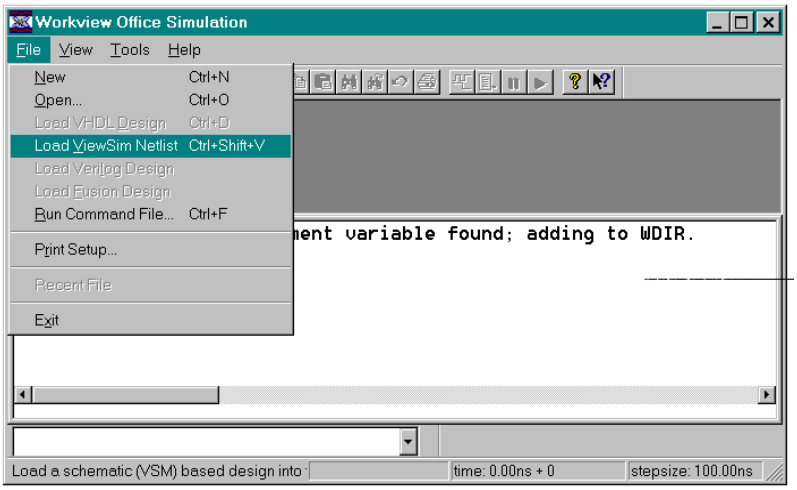
1. Launch pASIC 1 SpDE from the Workview Office toolbar or run SPDE1.EXE directly from the SPDE directory.
2. Execute the File→Import→QDiF command and select the BCOUNT4.QDF file.
3. Before running the tools, you must specify Viewsim for post-layout simulation. From SpDE execute the Tools→Options→Simulator... Choose "Viewsim" for simulator.
4. Execute Tools→Run Tools...and proceed with all options enabled. You will get a VL0000 Warning "Could not open file: c:\wvoffice\standard\vf\project.lst". Ignore it! After all the tools ran successfully, you may view the physical chip layout in the SpDE window. The back annotated files you'll need for Viewsim simulation are BCOUNT4.VL, BCOUNT4.DTB.

SpDE to Viewlogic VSM

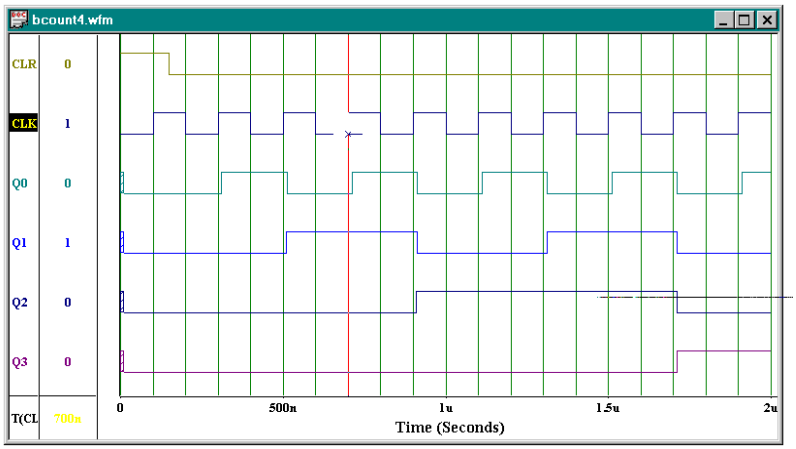
1. Launch SpDE2VLW from the Workview Office toolbar or run SPDE2VLW.EXE directly from the WVOFFICE directory.
2. Use Browse... to locate the BCOUNT4.VL file created by SpDE's back annotation tool.
3. You will get the message WARNING: Output WIR file already exists Overwriting the WIR file will allow simulated values to appear in the schematic drawing. Otherwise, type in a new name for the output WIR file which will result in a VSM of the same name. For this tutorial, allow the WIR to be overwritten.

Viewsim Simulation

1. Launch Viewsim from the Workview Office toolbar.
2. Execute File→Load ViewSim Netlist and select the BCOUNT4.VSM file.



3. Invoke File→Run Command Fileand select the BCOUNT4.CMD file.
4. ViewTrace will be automatically launched and the data from BCOUNT4.WFM will be displayed. The version of ViewTrace we tested had a problem with the initial waveforms displayed. Running View→Full will resolve this problem.
5. Verify that the results match a four-bit binary up counter as shown below.



This concludes the VHDL tutorial which illustrated the QuickLogic-Viewlogic VHDL design flow.

For Workview Plus/Pro Series Interface

Chapter 7 - Software Installation

Before installing the Viewlogic pASIC Design Interface, make sure that both Viewlogic's software and QuickTools are installed. For instructions on installing Viewlogic's software, refer to Volume 1 of the Viewlogic manual set. For instructions on installing QuickTools, refer to Chapter 1 in the QuickWorks User's Guide.

Software Requirements

- QuickTools or QuickWorks
- One of the following Viewlogic platforms:
  Full capability Workview Plus
  Full capability Workview Pro (Pro Series)
- ViewSynthesis version 2.2 or higher for VHDL entry

Additional software recommendations for the Workview version for DOS:

- Quarterdeck's QEMM386 memory manager version 6.02 or higher
- Smartdrive disk caching software from Windows 3.1 or higher

Installation Instructions

1. Insert the QuickLogic-Viewlogic Interface (for Workview Plus/Pro Series) disk and run the install.bat file. For a list of all options, type install with no parameters.
2. Reboot your machine and installation is complete.

Post Installation Notes -Workview Plus

NOTE: This is done automatically for you forWorkview Plus on the PC.

The Viewlogic pASIC Design Interface installs a customized toolbox to seamlessly integrate the SpDE tools with your Viewlogic environment. The SpDE drawer adds three new buttons: one for the QDIF writer (vl2spde), one for SpDE, and one for back annotation (spde2vl). The files needed are located in spdedir/tools, where spdedir is the directory that you installed the Viewlogic pASIC Design Interface. Three steps are required to use them:

- Create a tools subdirectory in your local WDIR and make it the current directory. Your WDIR directory can be found by typing "set" (PC).

```
cd wdir
md tools
cd tools
```

- Copy the files from the interface installation tools directory to your local WDIR directory.

```
cp /spdedir/tools/* .
```

- Move the file standard.tbx from the tools directory to your local WDIR directory.

```
mv standard.tbx ..
```

Post Installation Notes -Workview Pro/Pro Series

The Viewlogic pASIC Design Interface installs Workview custom menu files (viewdraw.mnX and procaptu.mn) in the WDIR directory to save keystrokes for running the QuickLogic interface programs. The commands that are added are:

- "Export QDF". This runs the vl2spde interface program.
- "Import SpDE". This runs the spde2vl interface program.

To undo the installation of these customized Workview menus, please refer to Appendix VLB of this manual.

Chapter 8 - Getting Started

This chapter shows you how to easily get started designing for pASIC's using both schematic entry and synthesis.

Schematic Entry

An example design (appropriately called exsch.1) is included in spdedir/examples, where spdedir is the directory that you installed the Viewlogic pASIC Design Interface. To use it, copy the file exsch.1 to the sch subdirectory of your current project. The following information will take you through a complete design cycle for a QuickLogic pASIC design.

Stage 1: Design

1. Load exsch.1 into Viewdraw.
2. Check the design for errors (check).
3. Always save the design before running the netlister because the netlister loads the design from the disk, not from the current design in memory.

Stage 2: Simulation - Functional

4. Export the Viewsim netlist.
5. Run the Viewsim simulator.
6. You can now simulate. Keep in mind that at this point simulation has only unit delay information, and is for functional debug purposes only.

Stage 3: QuickTools

7. Run the QuickLogic QDIF netlister (tool vl2spde from the Cockpit or Workview menu). This step creates the files exsch.qdf and exsch.neq. If you have made changes in your design, make sure you run check before exporting QDIF (see 2, above).

   Note: Notice the "Pre-layout information" given at this point by the netlister. Keep in mind that the cell utilization number is an estimate, as logic optimization from withinSpDE can significantly improve it.

8. Workview users now need to exit, and run Microsoft Windows. Powerview and Workview Plus users do not require this step. If you are running Viewlogic and QuickTools on different machines, you will need to transport the exsch.qdf file to the QuickTools machine at this point.
9. Run SpDE by double clicking on its icon, or pressing the SpDE button from within Cockpit.
10. Import the QDIF file exsch.qdf (File, Import QDIF).
11. Run the QuickLogic tools (Tools, Run all Tools). When the back-annotation tool is run, it creates three files: exsch.dtb, exsch.var, and exsch.vl. The first two files contain the back-annotated delay information for Viewsim. The third file is

an ASCII netlist description file that generates a wire file when you run spde2vl (step 14, below). If you use SpDE on a different machine from Viewlogic, these three files will need to be transported back to the Viewlogic project directory.

12. Save the design (File, Save), and view your completed design. (View, Full Fit).
13. Exit SpDE (File, Exit). Workview users now need to exit Windows and restart Workview.

Stage 4: Simulation - Timing Analysis

14. Import the SpDE delay files (tool spde2vl from the Cockpit or Workview menu). This step requires a file called exsch.neq from step 7 that contains all the net equivalence names you will need to back-annotate simulation information to all levels in the original schematic. This step also creates the exsch.vsm file with complete timing information.

> Note - If VSM gives you a help screen at this point, consult thereadme.txt file on your installation disk for instructions.

> Note - If your top level design has multiple sheets, running spde2vl will prompt you for a new name for the generated wire file. This is done to prevent VSM from creating an invalid simulation file. If you don't want to rename the wire file, create a single sheet schematic layer above your current top level. Renaming the output wire file will still allow complete back annotation to all levels of the original schematic.

15. Before you simulate your design, check your viewsim.ini file to ensure the DELAY SCALE parameter is set to 1.0 This parameter must be set to one to ensure accurate timing simulation, because the .DTB file generated by SpDE contains all the timing information needed for accurate timing simulation. Setting DELAY SCALE to any thing other than one will modify the timing information contained in the .DTB file, resulting in false timing simulation information. After ensuring the DELAY SCALE is set to one, You can now simulate the design from within Viewsim. See the Viewsim manuals for instructions on design simulation.

    Do not run VSM at any time after this point. If you do, you will overwrite the back-annotated Viewsim netlist file that was automatically created for you in step 14, above.

VHDL Entry

An example design is included in spdedir/examples, where spdedir is the directory that you installed the Viewlogic pASIC Design Interface. To use it, copy the file exsynth.vhd (example VHDL file) to your current project directory, and extop.1 (top level schematic) to the sch subdirectory. The following information will take you through a complete design cycle for synthesizing a QuickLogic pASIC design.

Stage 1: Analysis

1. Run ViewSynthesis.
2. Select pasic1 as the current technology by pressing the "Set Technology" button or typing "tech pasic1". If pasic1 is not listed as a selection, make sure that the file pasic1.sml is located in your WDIR path.
3. Load the example VHDL file by pressing the "Analyze VHDL..." button and selecting the exsynth.vhd file, or typing "vhdl exsynth".
4. Synthesize the design by pressing the "Run Synthesize" button, or typing "synth". At this point you will be given a list of QuickLogic macro cells that were used to generate your design, in this case a single OR gate.

Stage 2: Schematic Integration

Because ViewSynthesis does not currently add I/O pads automatically, you need to integrate your synthesized design into a top level schematic.

5. Create the wire file, which allows connectivity to a top level schematic so the QDIF file can be generated. This is done by pressing the "Wire..." button from within ViewSynthesis, or typing "wire".
6. Generate a schematic and symbol by running Viewgen on the wire file from step 4, above. To automatically create a symbol, make sure that the Make Symbol parameter is set to ON, or use the -makesym command line parameter.
7. Load the top level schematic example, extop.1, into Viewdraw. Note that an instance of your synthesized design, exsynth, is already placed and connected for you.
8. From this point on follow the Schematic entry steps 2-14 from page 5, substituting extop.1 for exsch.1. Note that SpDE's logic optimizer is optimized for synthesis, so the pre-layout information given by the netlister will be far more pesimistic than for schematic entry only.

> Note - Because you are now at the schematic level, you can do anything that the schematic entry only users can, including pre-placing I/O pads, and attaching a part and package to your design as described in the next section..

Design Entry Specific Tips

Defining theQuickLogic Part and Package: This is accomplished by adding two unattached attributes to your top-level schematic, PART and PACKAGE. For both, choose from those listed in the QuickLogic pASIC User's Guide. This prevents the QDIF netlister from prompting you for a part every time you export a QDIF file.
Example: PART=p8X12B
PACKAGE=PL68

Pre-Placement of I/O Pads:Change the pad symbol's attached attribute PLACE to the desired pin number. Consult the respective data sheets in the QuickLogic data book or the pinout appendices in the QuickLogic pASIC User's Guide for proper pin locations for these cells.
Example: PLACE=22.

> Note - It is not required that any pads be pre-placed. Those without placement information will be auto-assigned bySpDE.

Pre-Placement of Flip Flops:Change the flip flop symbol's attached attribute PLACE to the desired cell location.
Example: PLACE=A1.

Custom Hard Macros:If you make your own custom hard macros fromQuickLogic primitives (the MCELL library), you need to add an unattached attribute: LEVEL=QMACRO. To do this, push into the symbol level, make sure nothing is selected, then add attribute LEVEL=QMACRO. ViewDraw will report an unattached attribute. Write file and exit.

> Note - The unattached attribute LEVEL=QMACRO is required only when you create a symbol using the MCELLlibrary only.

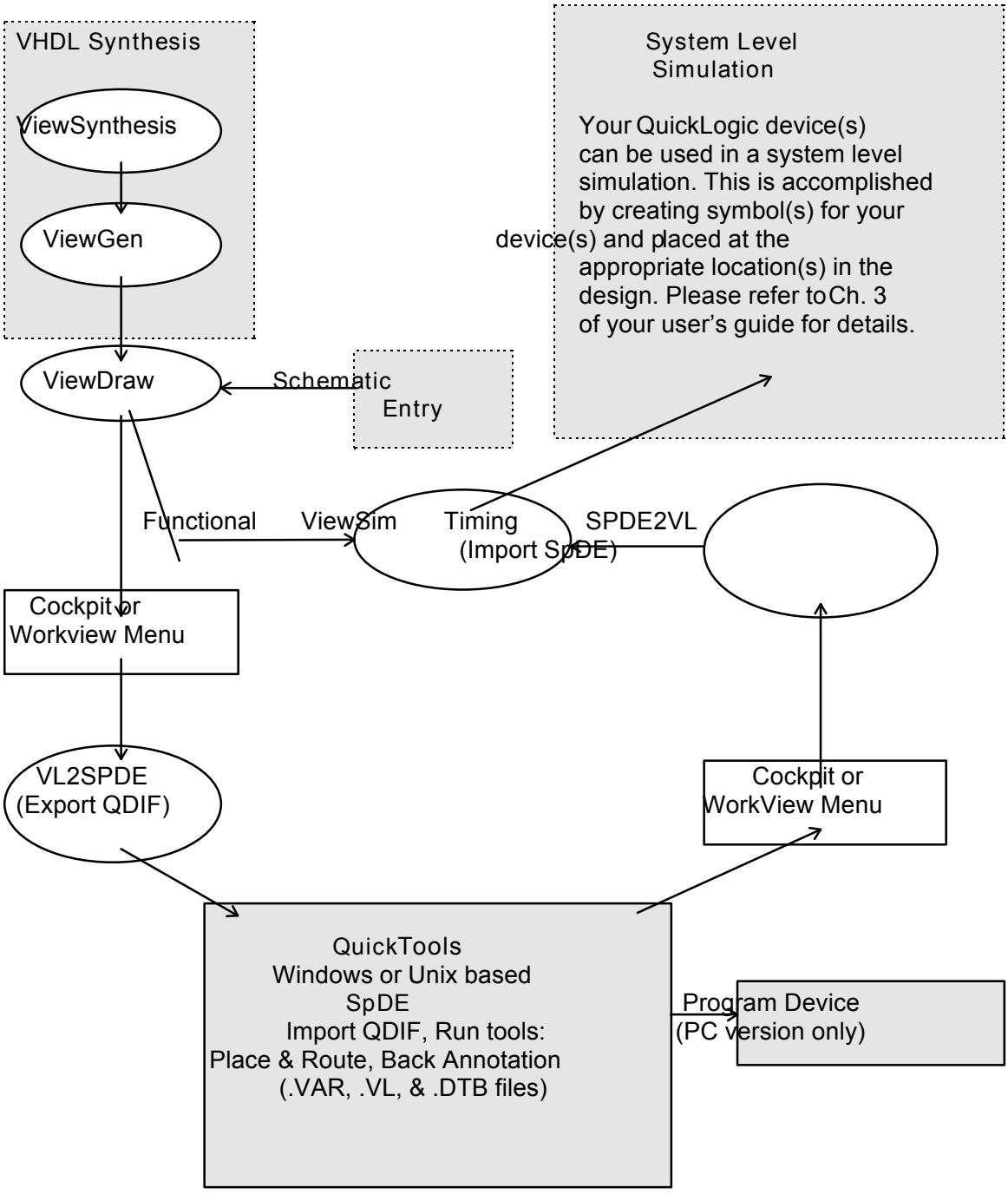
Important General Tips

- Use only the QuickLogic macro library when designing with QuickLogic pASIC devices. Do not use any standard Viewlogic or other third party libraries. As an aid in this, it is recommended to remove any references to any other schematic libraries from the Viewdraw environment.
- The high drive input macros HD2PAD, HD3PAD, and HD4PAD are supported under Viewlogic for automatic placement only. If you need to fix the placement for one of these, use the non-bus HDPAD version. For high-speed drive recommendations based on fanout, see table 5-5 in the pASIC Toolkit User's Guide.
- The macros INPADx, OUTPADx, TRIPADx, and BIPADx, where x is 4, 8, or 16, are supported for automatic placement only. If you need to fix the placement for one of these, use the non-bus version (INPAD, OUTPAD, TRIPAD, or BIPAD).

- Multichip and board-level simulation is available. See System Level Simulation section of this chapter for details.

The diagram on the following page illustrates the entire design flow of the Viewlogic pASIC Design Interface.

QuickLogic -Viewlogic Design Flow



System Level Simulation

It is sometimes desired to simulate a design where the Quicklogic device is not the top-level design. To do this, you need to first create a symbol for your QuickLogic design, then insert this at the appropriate position in your design hierarchy.

Functional simulation is performed normally, by running VSM on the top-level design.

In order to perform timing simulation using the Quicklogic timing numbers after place and route, you will need to create a top-level DTB file which references Quicklogic's DTB file. (DTB files contain all the dealy information from the QuickLogic place and route tools.) The format of the top level DTB file is as follows:

```
.BA
C instance_name_of_QuickLogic_symbol_in_design
A DTB = QuickLogic_design_name.dtb
.AB
```

for example, if you have a top-level design called "topdes", a QuickLogic design called "quick1", and the quick1 symbol is inserted into the topdes design with the instance name $1I1/$1I3/$1I5, then you would create the following file called "topdes.dtb"

```
.BA
C $1I1/$1I3/$1I5
A DTB = quick1.dtb
.AB
```

if you use the quick1 design twice in topdes, and the second instance was $1I1/$1I7, then the topdes.dtb file would look like the following:

```
.BA
C $1I1/$1I3/$1I5
A DTB = quick1.dtb
C $1I1/$1I7
A DTB = quick1.dtb
.AB
```

You can see how you can easily perform a multi-chip simulation this way. Now, in order to use this top-level DTB file, you need to specify it when you run VSM to create a Viewsim netlist for the top-level design. In this case, the VSM command line would be:

```
vsm topdes -d topdes.dtb
```

(the "-d" command line option specifies which DTB file to use).

If you are running VSM from the PowerView or WorkView Plus cockpit, then you can use the user interface to specify the DTB file instead.

Appendix - Error Messages

This appendix is a reference of all QuickLogic Viewlogic Design Interface messages. The messages are generated from either the Windows, DOS or Sun platforms, and are classified into Warnings and Errors.

Windows Platform

Warnings

Warnings are intended to bring a situation to the designer's attention. The situation is probably not a problem, but should be verified nevertheless.

VL0001 Warning: The WDIR environment variable is not set.
The VIEWSIM.INI in current directory has the correct 'delay scale' for the selected k-factor.
Workview either isn't installed correctly, or is not installed at all. This could be the case if you run SpDE and Workview on two separate computers or workstations. The correct k-factor is normally stored in the viewsim.ini as "delay scale <k-factor>". A viewsim.ini is in the current working directory with the correct information. Make sure you update the viewsim.ini in your Viewlogic project directory before doing post-layout simulation.

Errors

Errors flag genuine error conditions which will prevent the designer from continuing.

VL0002 Error: Cannot open file: <file name>
SpDE could not open the specified file because it either doesn't exist, or the specified path is invalid.

VL0003 Error: Cannot write to file: <file name>
An output file could not be written to. Check to ensure that the hard drive has enough space on it.

DOS/Sun Platforms

Warnings

Warnings are intended to bring a situation to the designer's attention. The situation is probably not a problem, but should be verified nevertheless.

VLD001 Warning: Component <component> has unconnected pin(s). (schematic <schematic>, symbol <symbol>, pin <pin>) The specified component has pins that are unconnected. The second line gives detailed information to find the component.
VLD002 Warning: Net <net> connects pins <pin1> and <pin2> of symbol <symbol>. The net is connected to more than one interface pin. Because of this, a unique name for this signal cannot be determined.
VLD003 Warning: Global net <net> onsubcircuit <schematic> is being ignored. Using signal name from level above. A global net which occurs on the sub circuit was defined on a different level as local, and is being ignored. This may not be what the user wants. Make sure that the specified net is supposed to be marked as global.
VLD004 Warning: Global net <net1> onsubcircuit <schematic1> is tied to global net <net2> on schematic <schematic2> above. Global nets with different names are tied together. This may be a design error.

Errors

Errors flag genuine error conditions which will prevent the designer from continuing.

VLD005 Error: Out of Memory. If this occurs, reboot the computer and try again.
VLD006 Error: The WDIR environment variable is not set. See Viewlogic manuals. When Workview is installed, the DOS environment variable WDIR is set. This is necessary for the QuickLogic netlister to run.
VLD007 Error: This wire file was created by SpDE. Run check on the design first. You must check the design before running the netlister. This updates the wire file. This can happen if the design wasn't saved since the last IMPORT|SPDE with the same design (the netlister reads the design from disk, not from memory).
VLD008 Error: You entered an invalid <part | package> name: <string>. You entered an invalid part or package name. This can occur either by typing in an invalid value on the QDIF netlister command line, or placing invalid values on the schematic with the PART= or PACKAGE= attribute.
VLD009 Error: Cannot have fragments in upper levels for <component>. Do not mix the QuickLogic fragments (in the MCELL library) with any macros on the same hierarchical level.

VLD010 Error: Illegal fragment: <comp>.
VLD011 Error: Error loading fragment for <comp>.
VLD012 Error: Error loading fragment for <comp>, owner <comp>. Could not load the fragments for a hard macro. Make sure that all hard macros and no soft macros have the unattached attribute LEVEL=QMACRO.
VLD014 Error: Symbol <symbol> defined as type MODULE. Do not define any symbols as block type module. Only define them as composite.
VLD015 Error: Cannot open file <file>. The specified file was not found, or the path was invalid.
VLD016 Error: Cannot write to file. An error occurred while writing to a file. Check to make sure that the hard drive is not full.
VLD017 Error: Invalid input file. VLD018 Error: Invalid string in file: <string> VLD019 Error: Invalid function call: <num> The data file <design>.VL has become corrupted. Re-run back annotation from SpDE to re-create the file.
VLD020 Error: Could not initialize VIEWBASE. Viewlogic is not set up correctly. Consult the Viewlogic documentation. Check the path, INI locations, and WDIR environment variable.
VLD021 Error: Invalid part file. The part file is corrupted or incorrect for the current version of vl2spde. Contact QuickLogic for the latest part list file.
VLD022 Error: Old version of part file. The part list file is from a previous version of vl2spde. Contact QuickLogic for the latest part list file.
VLD023 Error: A design name must be entered. If no default design was found in the spde.dat file, you must enter a design name. Check to see that the spde.dat file is in the current project directory.
VLD024 Error: Design <design> has multiple top level sheets. You must rename your new wire file created from spde2vl to keep VSM from creating an invalid simulation file. On the DOS platform, you will be prompted for a new name. On the SUN platform, you need to re-run the spde2vl program with the parameter set to a new name.
VLD025 Error: Cannot connect <VDD|GND> to top level net <net>. VDD or GND nets must be driven from the top of the net heirarchy. Rename net <net> to VDD or GND. If you are driving a bus net with VDD or GND, drive it through a buffer (which will be stripped by the Tech Mapper).