QUICKLOGIC

QuickNews

Issue #1 · Winter 1994

Welcome to our First Issue!

Welcome to QuickNews - QuickLogic's quarterly user's newsletter. In this issue you will be introduced to our Customer Engineering and Customer Service groups (if you haven't already met us in person!). Hopefully, we will also be able to convey to you some very valuable and useful information about our product, and our commitment to serve you. You will no doubt find our Hotline Q&A section very informative, as we have compiled a summary of the most frequently asked technical questions (and, of course, their answers).

Please let us know your opinion concerning this first issue of QuickNews. We need to know what topics and information can be most useful to you. Any comments can be directed to the QuickLogic Hotline. 408-987-2100. Ask for Ben, Brian, Kevin, or Randy.

Words from QuickLogic's CEO

First, let me personally thank you for your continuing interest in QuickLogic and our family of high speed FPGAs. We believe providing value to you, our customers, is the primary focus of our business. This newsletter is just one example of the many activities we undertake to help you realize our value.

I'm new to the QuickLogic Team, joining in June 1994 as the President and Chief Executive Officer.
Since then it has become very apparent to me that this dedicated, talented team is committed to offering you superb value through superior products and services. Just one example is the Customer Engineering group, which

CEO Tom Hart

assists you in the design process. These folks are the experts when it comes to using QuickLogic FPGAs, and helping you gain advantage with your products. Their success is based on helping you achieve "time to market" solutions, which enable you to win in your marketplace.

Our recent introduction of Quick*Works*™ establishes the definitive benchmark for a tightly integrated, "best of breed" design tool for QuickLogic FPGAs. Synplify-Lite™ answers your growing need for world-class, cost-effective FPGA synthesis. Quick*Works* is one more example of our commitment to providing you with the best overall value in choosing QuickLogic as your partner for FPGAs.

We hope you find this newsletter interesting and useful. Please know that we value your insight on how QuickLogic may better serve you. Don't hesitate to call me directly.

All the best,

Tom

Tom Hart
President and Chief Executive Officer

Contents

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OOPS!

The "Package Pin Bonding Cross Reference" tables on pages 5-41 to 5-43 of the 1994 QuickLogic Databook contain errors. To quote from an internal e-mail from one of our designers:

> **"...I recommend that you either rip them out of your book, or put a large black X over them." -PK**

Please contact the QuickLogic Hotline at (408) 987-2100 if you want an updated table. (Corrected in Latest Re-Print)

BETA-sites Needed for Upcoming Products!

QuickLogic will be introducing a wide range of new product support in the next year. Beta-Sites will be needed to test out these new interfaces:

- **QuickLogic** SpDE on HP Workstations
- **Intergraph** AceSyn, MacroSyn, and AdvanSIM
- **Synplicity** VHDL and ABEL Synthesis
- **Cadence** Synergy, Composer, and Leapfrog SIM
- **Synopsys** VSS VHDL Simulator
- **Mentor Graphics** Falcon Schematic, and QuickSim
- **ALDEC** ActiveCAD and SUSIECAD

We can only support a small number of BETA sites for each one of these products. Please call the QuickLogic Hotline if you are interested. (Mention this article!)

Check out our QuickLink BBS!

If you have a modem, a terminal program (like *Terminal* in Windows) and an interest in what's new from QuickLogic, you have all that's necessary to check out the QuickLink BBS. The QuickLink BBS is available 7 days a week, 24 hours a day.

If you are using Windows Terminal:
Load the file "QUICK.TRM" from the c:\pasic\spde\data directory. This file contains all the configuration data for the QuickLogic BBS.

If you are using some other terminal program:
First of all, we don't blame you for not using Windows *Terminal*, because it doesn't even support ZMODEM. Any baud rate up to 14.4 K-baud will work. We recommend 8 data bits, no parity, and 1 stop bit.
QuickLink BBS phone number: **(408) 987-2080**.
Our European BBS number is **+49-89-899-0399**

If you are a new user, you will be asked to answer a few questions to set up an account. Then you can call the QuickLogic Hotline to have one of the Customer Engineers upgrade your account to full customer access status, so you can take advantage of new App-Notes (with schematics), Software, and Library Macros.

The QuickLink BBS is still growing. The Sysop would appreciate any feedback you might have about the BBS so we can make it the best BBS in the FPGA community.

Customer Engineering

As manager of the Customer Engineering group at QuickLogic it is my privilege to work with the brightest, most innovative, hard working applications engineers in the programmable logic industry. Their job is to be there when you have a technical question about QuickLogic products. Your questions may regard QuickLogic devices or development tools. There will be a highly skilled, motivated engineer at the other end of the line, ready to help you. When you call you get a human being, not voicemail.

Customer Engineers
(left-right) Ben, Don, Randy, Kevin, Brian

The capabilities of QuickLogic products are extraordinary. The customer engineers derive great satisfaction from showing you how to use the full extent of these capabilities. The pASIC devices are the fastest FPGAs in existence and getting faster with each new family we release. The QuickLogic tool set is hands down the easiest to use programmable logic development system in the industry. This combination allows you to do things you never thought possible. New levels of design performance and logic utilization are available to the designer. New methodologies of fast design iteration can now be explored. Let the customer engineers guide you to these new levels of performance. They love to push the envelope.

If you are a registered QuickLogic customer with our full design package, get ready to receive a brilliant upgrade. The upgrade is to Quick*Works* the most revolutionary FPGA design package ever introduced. Quick*Works* includes a PC-based Verilog synthesis tool that exceeds the performance of other synthesis tools available from expensive workstation-based CAE tool vendors. Quick*Works* also includes a Verilog simulator as well as a variety of other handy utilities and improvements. Registered designers as of Dec. '94 with our full design kits will get this upgrade free of charge. If you are not registered, call and get registered ASAP, so we can ship you Quick*Works*.

Don Alexander
Customer Engineering Manager

Our Customer Service Team

Today's knowledgeable customers expect expedient and personalized service. Our Customer Service team is there to meet those needs. Customer Service is available to answer product questions and solve problems of a non-technical nature. (Customer Engineering is available for Technical questions).

If there is a problem, we want to know about it and resolve it as quickly and as efficiently as possible.

Our Customer Service line is open from 7^{30} AM to 5^{30} PM PST. You can reach either Linda or Suzanne at (408) 987-2033/2032. If you have any issues regarding software registration or maintenance, please call Kristy McAbee at (408) 987-2035.

✓ *Don't forget to make sure that your software maintenance agreement is up-to-date. If your yearly maintenance fee is due, you may want to take care of it soon to take advantage of the* Quick*Works free upgrade.*

QuickLogic Sales Managers

Our Regional Sales Managers are always available if you need to get hold of a QuickLogic employee in your area. Contact your local QuickLogic Sales Representative or Distributor for product pricing and availability questions (Refer to the 1994 Databook for Sales Offices).

East US, East Canada *New England,NY,MD,VA,NJ,MS, AL,DE,NC,SC,GA,FL,East PA*	**Bill Greeley** **(617) 631-4279**
Mid-West US *ND,SD,MN,WI,MI,IO,IN,OH, IL,NE,TN,LA,AR,OK, TX,KS,MO,WV,KY, West PA*	**Danny Gow** **(214) 414-6908**
North-West US, West Canada *WA,OR,NV,AK,Northern CA*	**Bill Hassett** **(408) 987-2007**
South-West US, Pacific Rim *MT,WY,ID,UT,CO,AZ,NM,HI, Southern CA*	**David Pegan** **(310) 546-5589**
Europe, UK	**Bruce Kleinman** **+49-89-899-143-28**

New Products

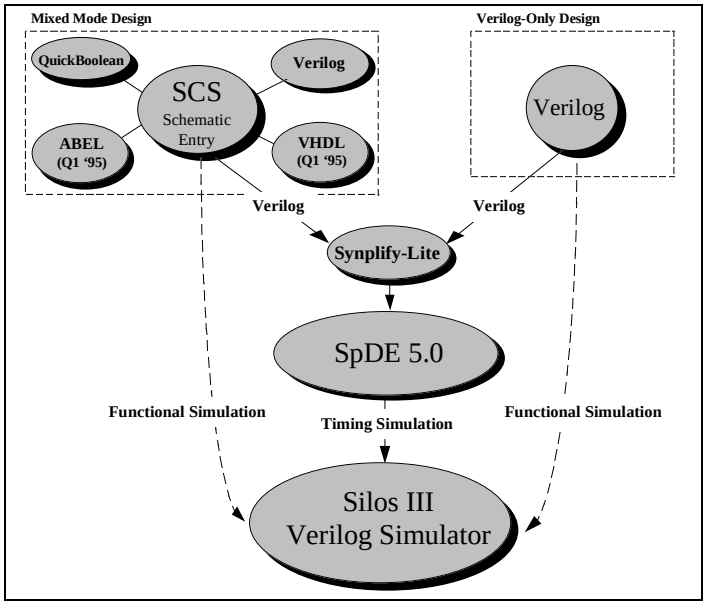
QuickLogic Corporation has just announced the next

Quick*Works*™ Sets The Standard

generation in FPGA Design Tools - **Quick*Works***. For years QuickLogic has provided an integrated, easy to use toolset to guide designers through their FPGA designs with maximum speed and flexibility. We have continued to live up to this commitment.

The Quick*Works* toolkit contains a suite of tools that is unprecedented in today's market, with prominent features such as:

- Verilog® HDL Synthesis (VHDL in Q1 '95)
- Context Sensitive HDL Editing
- Color Coded HDL Template Expansion
- Mixed-Mode Design Entry
- Enhanced Schematic Capture
- Comprehensive Verilog Simulation
- Interactive Cross-Probing Between Tools



Quick*Works* Design Flow

Design Flow

As illustrated in the Quick*Works* design flow diagram, designers can mix a combination of schematic, boolean, and/or Verilog (VHDL coming in Q1 '95) using the Synario Capture System design entry tool. Symbols within the schematic editor can reference boolean files or Verilog files allowing a mixture of schematic design and HDL design. The designer can then simulate functionally (zero-delay) or produce a Verilog netlist, synthesize, place, and route the design, and then simulate with full timing information. The static timing analyzer, timing driven placement and other features (design optimizer and compiler) are still available to aid in the design process.

Product Features

- **TurboWriter™ Editor**

  The **TurboWriter**™ editor offers a host of features - from emulation of a variety of text editors to context sensitive and color coded entry. Common editors such as vi, Epsilon, or others can be emulated. Context sensitive editing provides a variety of synthesis templates for language constructs, keyword-based template entry and syntax generation. Color coding aids in easy readability and syntax verification. In addition, automatic generation of test-benches aids in Verilog or VHDL simulation.

- **Synplify-Lite™**

  A highly integrated Verilog HDL synthesis tool. Honestly said, Synplify-Lite is "Simply Better Synthesis™", providing:

  a) **Quality results** - better performance and density implementations than other vendors
  b) **Ease-of-Use** - no vendor specific directives required, just OVI compliant Verilog,
  c) **Speed** - fastest run time of any synthesizer on the market - a 4K design in minutes

- **Synario Capture System (SCS™)**

  An easy-to-use Windows schematic capture utility. With the same touch, feel, and functions of the ECS schematic capture we've offered before, SCS offers a wide breadth of enhancements from waveform entry to back-annotation. Mixed mode entry (schematic, boolean, and/or Verilog/VHDL) is supported, providing a variety of entry methods. In addition, an updated Waveform Editor is included for graphical waveform entry, and will export Verilog test-fixtures for simulation.

New Products

- **SpDE™ 5.0**

Quick*Works*™ (continued...)

SpDE 5.0 offers preliminary design support for the new *Wild*Cat™ 8000(QL24X32B). Improved simulator timing models and faster programming algorithms for all existing devices have been implemented. Programming times have decreased by up to 66%.

- **Silos III™ Verilog Simulator**

Silos III provides the Verilog simulation power demanded by designers. Rated one of the top simulators by ASIC and EDA magazine, this OVI-compliant simulator is both fast and easy-to-use. Silos III supports graphical waveform entry as well as Verilog test benches. Designers who have previously used QuickLogic's Waveform Editor to enter stimulus can use the same files for Verilog simulation.

Quick*Works* requires 8 MB of RAM, and a 16 MB Permanent Swap File in Windows. Approximately 30 MB of disk space is necessary for a full installation. Quick*Works* will be available as a free upgrade to all registered customers with a current maintenance agreement (as of Dec. '94) for QuickLogic's ECS-PC product. Call our customer service department (408-987-2035) if you have any questions.

Keys? We don't need no stinkin' keys!

Quick*Works* does not require a software key! We had to perform some tricky negotiating with our third party design tool and simulation vendors in order to continue to offer our customers the easiest to use, *easiest to install* development tools in the FPGA business. Besides that, we're guessing you probably don't have enough room for yet another key on your COM port anyway!

The New *Wild*Cat 8000

In efforts to provide bigger. better, and faster devices, QuickLogic will soon be introducing the latest in the *Wild*Cat family of devices - the ***Wild*Cat 8000**.

Manufactured on a 0.65 micron CMOS process, this new device will have the architecture and speed of the existing pASIC 1 family of devices with at least twice the density. With an array of 24-by-32 logic cells, the *Wild*Cat 8000 will provide 8000 usable gates with 768 available flip-flops and a total of 172 inputs/outputs. It will be available initially in the 144 pin TQFP and the 208 pin PQFP packages with other packages to follow. The 8K device will be pin-for-pin compatible with its smaller counterparts (true of all QuickLogic devices). I/O Buffers will be fully compliant with the Peripheral Component Interconnect (PCI™) local bus I/O pin drive specification.

The QL24x32B will be sampling in Q1 '95. Designs can be entered targeting the QL24X32B with Quick*Works*.

*Wild*Cat 8000 Product Summary

Device Order Code:	QL24X32B
Number of Usable Gates:	8000
Number of I/O pins:	172
Number of Logic Cells:	768
Number of Flip-Flops:	768
Number of Latches:	1536
Packages:	144 TQFP 208 PQFP More to follow
Engineering Samples:	Q1 '95
Production Shipment:	Q2 '95

Hotline Corner

The QuickLogic Hotline is always available for any technical questions about any QuickLogic Product. We can be reached by Phone, Fax, E-Mail, or BBS:

Phone: 408-987-2100
8:00 AM to 5:00 PM PST Mon-Fri

Fax: 408-987-2012
BBS: 408-987-2080
E Mail: support@qlogic.com

If you call the Hotline telephone number, you will always have a real-live QuickLogic Customer Engineer answering the phone (assuming you call during Pacific standard time business hours). Our Customer Engineering group is committed to providing the industry's most effective technical assistance.

Popular Hotline questions

Q When I perform back-annotated simulation I get unknowns on some of my internal signals even though the outputs appear to be working.

A *When SpDE generates the back-annotated simulation files, it creates a physical netlist of the design as it was implemented in the QuickLogic device. This means that some nets will be absorbed into a logic cell and basically "disappear" from the simulation netlist. In unit delay simulation all signal nets will be present.*

Q I laid out my PC board using a TQFP package and my pins do not line up.

A *As shown in the 1994* ***QuickLogic Databook****, the TQFP packages have controlling dimensions in millimeters. If you lay out the board using a pad pitch of .020 mils instead of .50 mm, the pad layout will not match.*

Q When I try to simulate back-annotated delays in ViewLogic I only get unit delay simulation.

A *QuickLogic generates all required back-annotated simulation files during the back-annotation portion of chip compilation. The difficulty can be caused by one of three problems.*

1. *The* ***Back-Annotation*** *tool was not run in* ***SpDE****: In order to generate the necessary back-annotation files, it is required that the* ***Back-Annotation*** *tool is run during chip compilation.*
2. *SpDE may not know you are using Viewsim: Under the* ***Tools*** *menu, in SpDE, choose* ***Options-Simulator*** *and select* ***Viewsim****. After setting this option, you must re-run the SpDE back-annotation tool on the design. From the Tools menu select Run Tools, click on the back-annotation check box and click on the Run button. This will generate fully back-annotated .VL, .DTB and .VAR files.*
3. *After running* ***SPDE2VL****, you are re-running the Viewsim netlister (vsm): This will cause Viewlogic to overwrite the back-annotated simulation netlist with a unit delay netlist.*

Q Sometimes I get the error message "SQ0000: Sequencer could not complete. Re-run the Router with a different seed.

A *While trying to determine the sequence in which links will be programmed, the Sequencer tool "painted itself into a corner" and could not find a way to isolate each and every link. From the* ***Tools*** *menu select* ***Options-General****. In the* ***Router*** *section click on the* ***Custom*** *radio button. In the box just to the right enter any random number and click on the OK button. Re-run the tools from the router on.*

Q If the sequencer fails, I'd like SpDE to automatically re-run the router with a new seed until it successfully completes

A *Me too... (Seriously, though, we are planning on adding this feature in a future version.)*
[ed. note: This has been added to **Quick***Works!]*

Q I need a 6-bit counter for my design, but I don't see one in your macro library. I know that I could use an 8-bit counter and ignore the extra bits, but I don't want to waste the extra logic cells. Could you build one for me?

A *Too bad (just kidding). If you need to use a smaller macro than what's available in our library, you're not out of luck. Just use the bigger macro, and leave the unneeded outputs hanging. By default, when you import your design into SpDE, the unused logic will be automatically stripped out of your design, in effect reducing the "full-sized" macro into a smaller one. Unused inputs should be tied to VCC or GND. This technique works not only with counters, but also with the adders, registers, shift registers, and the TTL library -- any macro with multiple outputs.*

New QuickNotes Available

We've been at it again! A large number of QuickNotes are now available to be faxed on request (or mailed if desired) from the QuickLogic Hotline. QuickNotes are helpful documents that explain how to use various aspects of QuickLogic devices and development tools. Please request the QuickNote by number according to the table below:

QuickNotes Available

ID#	Title
QN1	Design Flow
QN2	Using High Drive Pads Efficiently
QN3	Design Rules for Improving ATVG Results
QN4	Designing with QuickLogic
QN5	File Generation
QN6	Fixing I/O Cells and Flip Flop Locations
QN8	Updates and Corrections to the pASIC Toolkit User's Guide
QN11	Designing w/CUPL, Palasm, and ABEL Design Tools
QN12	Understanding SpDE's ATVG
QN13	Simulating QuickLogic Devices at 3.3 Volts
QN15	Implementing a One-Hot State Machine using QuickBoolean
QN16	Analyzing & Optimizing Performance using QuickBoolean
QN20	System Level Simulation for ViewLogic
QN21	Maximum power dissipation for QL devices
QN25	ECS Simulation with Bi-directional Busses
QN26	Programming QuickLogic Designs with the Data I/O Unisite and 3900
QN27	Instantiating CKTPADS and HDDPADS in Synopsys using VHDL

At the time of this newsletter's release, a number of additional QuickNotes were in the plans. Call the QuickLogic Hotline for an updated list, or check Bulletin #1 on the QuickLink BBS.

Third Party Tool Support!

QuickLogic wants to work inside *your* design environment, not force you into ours. Because of this philosophy, we have introduced many new third party tool interfaces. The table below lists the third party tool interfaces we support, along with the official QuickLogic product code.

Product	Order Code
Synopsys Interface for SUN	QS-SYN-SUN
Synopsys Interface for HP	QS-SYN-HP Call for Availability
Viewlogic Interface for PC	QS-VL-PC
Viewlogic Interface for SUN	QS-VL-SUN
Intergraph Interface	QS-INTG-PC
Cadence "Concept" Interface for SUN	QS-CNC-SUN
Mentor Graphics Interface for HP	Call

For the above products, you must also have A QuickLogic toolset which includes the SpDE placement and routing utility. The QuickLogic toolset will include utility libraries to interface with all the following third party tools without additional products.

LMC SmartModels
Verilog XL Simulation
Silos III Simulation
QuickSim Simulation
Intergraph Simulation
Unisite/3900 Programming

The following QuickLogic interfaces are sold by the respective vendors directly.

Exemplar Logic Interface	Sold by Exemplar Logic
Synario Interface	Sold by Data I/O
ABEL Interface	Sold by Data I/O
LMC SmartModel Library	Sold by Logic Modeling
Intergraph Interface	Sold by Intergraph
CUPL Interface	Sold by Logical Devices

Are you Current?

QuickLogic has introduced new devices and design tools on a very aggressive schedule this year. Please use the following table to determine if you are currently up to date.

Current Software

Note: Check software revisions by checking the revision numbers printed on the installation disks, or by the method indicated...

✓	Quick*Works* Version: 5.0 (previously 4.21) • (Select **About SpDE** from SpDE's **Help** menu)
✓	Synopsys Library: 0.7 (disks labeled as 1.0) • Synopsys 'report_lib *library_name*' command
✓	ViewLogic Library SUN: 4.1
✓	ViewLogic Library PC: 4.2 • Reported when VL2SPDE or SPDE2VL is run
✓	Cadence Library: 1.1 • Check installation disk label
✓	Intergraph Library and Interface: 1.0 • Check installation disk label

Current Programming Hardware

Note: Check hardware revisions by looking for the revision code on the bottom side of the product.

✓	QuickLogic Designer Programmer	: R1
✓	QP-PF100 (100 pin TQFP adapter for the QL8X12B or QL12X16B)	: R1 or R3
✓	Other Hardware	: (no revisions)

If you require a newer version of software, or a hardware update, please contact our Customer Registration number: (408) 987-2035.

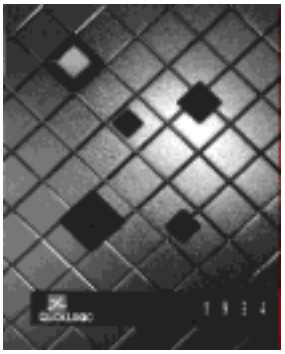
Using the Right Socket Adapter?

Remember that different devices in different package combinations may require a special socket adapter. The table below shows which socket adapter you will need for each package and device. Verify the adapter name on the bottom of your QuickLogic socket adapter.

Package	**Device**	**Adapter Needed**
44 pin PLCC	QL8X12B	QP-PL44
68 pin CPGA	QL8X12B	QP-CG68
68 pin PLCC	QL8X12B QL12X16B	QP-PL68 QP-PL68
84 pin CPGA	QL12X16B	QP-CG84
84 pin PLCC	QL12X16B QL16X24B	None Needed QP-PL4084
100 pin TQFP	QL8X12B QL12X16B QL16X24B	QP-PF100[1] QP-PF100[1] QP-PF4100
100 pin CQFP	QL12X16B QL16X24B	QP-CF100 QP-CF4100
144 pin CPGA	QL16X24B	QP-CG4144
144 pin TQFP	QL16X24B	QP-PF4144
160 CQFP	QL16x24B	QP-CF4160

[1] Revision R1 or R3 needed for this adapter

Do you have the 1994 Databook?



If you don't already have a 1994 Databook, or if you have a QuickLogic Databook and it doesn't have the cover displayed on the right, then contact our Literature Department at 1-800-832-FPGA (3742) and ask for our 1994 Databook. We will mail one out to you immediately. For faster service, contact your local QuickLogic Sales Office. Our 1994 Databook includes information on our 0.65 micron devices, introduced earlier this year. Also the Databook now contains a wealth of product information and Applications Notes.

Happy Holidays

from all of us at QuickLogic!