Versa Ware JTAG



Software User Guide

This user guide addresses the features, setup and operation of the Versa Ware JTAG software for Flash programming and debugging of Ramtron's high performance VRS51L2xxx and FRAM-enhanced VRS51L3xxx microcontroller series.

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1 Versa Ware JTAG Software Overview

Versa Ware JTAG is a user-friendly, Windows®-based tool for system prototyping and design development with Ramtron microcontrollers that feature a JTAG interface (VRS51L2xxx/3xxx and future derivatives).

Versa Ware JTAG has two primary functions:

• Versa Ware JTAG Programmer

The Versa Ware JTAG Programmer provides a comfortable interface to perform operations such as erase, program, read, etc. on the target device's Flash memory.

• Versa Ware JTAG Debugger

The Versa Ware JTAG Debugger is a user interface that links the in-circuit debugger to the source code. All Ramtron microcontrollers with a JTAG interface include an integrated debugger that enables in-application debugging of the device through its JTAG interface.

1.1 Minimum System Requirements to run Versa Ware JTAG

Versa Ware JTAG has been developed for Windows XP[™], but it will also run on Windows 2000[™], Windows Millennium[™], Windows 98[™] and Windows NT[™] 4.0 operating systems, on a PC that meets the following system requirements:

- Intel Pentium® III 400MHz
- 128MB of RAM
- 10MB of hard drive space
- 1 free IEEE 1284 parallel port
- A session of Windows running in administrator mode for installation (except Windows 98[™])

Only built-in motherboard parallel port and ISA parallel port cards are supported. A Versa-JTAG interface must be connected on LPT1. Please see Section 9 for more details on parallel port setup and supported modes.

1.2 Target Environments

Versa Ware JTAG Software is used the Versa JTAG - a parallel port to JTAG interface supplied by Ramtron. The Versa JTAG is connected to a VersaKit-20xx or VersaKit-30xx devboard, or to a PCB that incorporates a Ramtron JTAG-based device, such as the VRS51L2070 and the FRAM-enhanced VRS51L3074.



2 Versa Ware JTAG Software Installation Procedure

After downloading the Versa Ware JTAG Software setup file, begin the installation process by double-clicking on the icon below:



Figure 1: Versa Ware JTAG Setup Screen

When the setup process is complete, the following icon will appear on the Windows™ desktop. Click it to launch the Versa Ware JTAG Software.





3 Using the Versa Ware JTAG Programmer

3.1 Interface Overview

The application window provides a quick and easy reference to all JTAG operations. These include:

- Toolbars
- Status bars
- Menus

🖪 Versa Ware JTAG - Your_Applicatio	n.ihx 📃 🗖 🔀	
<u>File Flash Device View Window H</u> elp		
≒ 🚅 🗣 🖉 🐚 🦊	🛧 🛨 🕨 🛞 👫 🛈	
File	Toolbar	
Name: Your_Application.ihx	File Information Window	
Size: 6973 Bytes		
CRC: A87E8796	Info	
File Status Bar check.	Erase Prog	
VRS51L2070-40-Q waiting for instruction	CLK MAX DBG VER 💥	

Figure 2: Versa Ware JTAG User Interface

3.2 General Toolbar

The Versa Ware JTAG Programmer Software can perform 11 main functions, which are grouped onto a general toolbar. These functions are accessible when the software is in Programmer Mode.



Figure 3: General Toolbar

The toolbar can be moved from its default position at the top of the software's main window Grab the general toolbar by left clicking the mouse and dragging the toolbar to your preferred location. The toolbar will return to its default position when the program is closed.

3.3 Status Bar

The status bar is located at the bottom of the Versa Ware JTAG Programmer window. It indicates the status of all Versa Ware JTAG Software activities.

🔁 Versa Ware JTAG - Your_Application.ihx	
File Flash Device View Window Help	
⇆ҝ┙҈⊉⊉т►®	11 🛈
R Your_Application.ihx	
c File	
Name: Your_Application.ihx	
Size: 6973 Bytes	
CRC: A87E8796	D
File passes integrity check.	Prog
Inc	dicators
_	
Programming (Ctrl+Z to cancel)	1AX DBG VER 🛒

Figure 4: Versa Ware JTAG While Performing an Erase and Program Operation

3.3.1 Indicators

The status bar indicators describe current device options. For more information on how to change them, see Section 3.8.

- Clock speed indicator: Displayed as CLK / n, shows the connected device's boot-up clock divider setting. If the divider is 1, CLK MAX will be displayed.
- **Option indicator:** If debugging is enabled, **DBG** will be displayed. If security is enabled, **SEC** will be displayed. If neither is enabled, this area will be blank.
- Verification indicator: If verification is enabled, VER will be displayed; otherwise this area will be blank.



3.4 Programmer Command Overview

The following table shows all of the possible programmer commands:

Command	Toolbar button	Menu	Keyboard Shortcut
Synchronize		File	F2
Open		File	Ctrl + O
Info		File Information Window	Alt + I
Erase	Ø	Flash	
Erase Page		Flash	
Erase then Program	₽	Flash	F5, Alt + E
Program	4	Flash	Alt + F5
Read		Flash	
Reset	Ш	Device	Ctrl + Alt + R
Run		Device	F8
Debug		Device	F9
Options	ti	Device	
Toolbar		View	
Cascade		Window	
Tile		Window	
About	()	Help	

Table 1: Programmer Command Summary

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The Versa Ware JTAG Programmer controls are grouped by function in the following locations:

- File Information Window and file menu
- Flash menu
- Device menu

3.5 File Information Window

The File Information window provides information about Hex file to be loaded. Versa Ware JTAG Software supports program files in the Intel Hex file format. These files typically end in .HEX or .IHX and consist of lines that begin with colons (:) followed by hexadecimal digits (A-F and 0-9). Most C compilers and cross assemblers are capable of generating Intel Hex files, but on some suites this may not be the default option. Consult the development environment's user manual for more details.

R	R Your_Application.ihx		
	File Name: Your_Application.ihx Size: 6973 Bytes CRC: A87E8796 File passes integrity check.	Info Erase Prog	

Figure 5: File Information Window

The first line contains the filename. The file name, including the path, cannot exceed 1024 characters.

The second line is the size of the program in bytes. It is not the size of the file, but a calculation of how much space the program would occupy in the device's Flash memory, if it were in one contiguous block. Empty space within the program is not counted. If the file is invalid, an error message will appear here.

The third line refers to the checksum. The checksum consists of 8 hexadecimal digits calculated using the CRC32 standard. A difference of even 1 bit between files will result in a different checksum. This is particularly useful to determine whether a file has been modified or corrupted, and is a good way to keep track of different versions with the same file name.

The fourth line refers to the integrity of the file. Each line of a properly-formed file has a checksum byte, which is the 2's complement of the least significant byte of the sum of bytes of the rest of the line.

Formula for Calculating the Checksum in an Intel Hex File			
(Sum of bytes after the colon except for last) mod 0x100 + (Last byte) = 0x100			
Example: :0E0055007820439308E59B759BFF759D4F75C2			
(0E + 00 + 55 + 00 + 78 + 20 + 43 + 93 + 08 + E5 + 9B + 75 + 9B + FF + 75 + 9D + 4F + 75) mod 100 + C2			
= 73E mod 100 + C2			
= 3E + C2			
= 100			

Table 2: Checksum of an Intel Hex File

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A file that fails the integrity check can still be used to program the device. Files that were modified by hand, or do not have the correct CRC value at the end of a given line, will cause an integrity failure. Corrupted files will also cause integrity failures. Files created by a Flash read will pass an integrity check, as the CRC is calculated and inserted at the end of each line created in the output file.

A file is automatically reloaded before programming, so that the most recent data is used.

Up to 16 file names and paths are retained between application sessions. These can be selected from the File menu.

3.5.1 Erase Prog Button

This button provides a quick shortcut to the "Erase then Program" command. See Section 3.6.1 for more details.

3.5.2 Extended File Information

Clicking the Info button on any File Information window will open a File information dialog.

File information			
General Path: B:\Demo\Your_Application.ihx			
CRC: A87E8796			
Created: May 02, 2006 02:32 PM	Attributes		
Modified: May 02, 2006 02:32 PM	Read Only Hi	dden	
Accessed: May 04, 2006 02:18 PM	Archive Sy	stem	
Device Size on device: 6973 Bytes (7 KB) File passes integrity check.			
This program can be debugged.			
Flash usage (debug):	1	1%	
Flash usage (release):	1	0%	
	C	ОК	

Figure 6: Extended file information

The File information dialog provides general file information and device file information:

- **General** information includes:
 - The complete file path
 - The CRC (see Section 3.5 for more details)
 - o When the file was created, modified and accessed
 - File attributes: If the file is read-only, hidden, archive or system. Figure 6 displays an archive file.
- Device information includes:
 - Size of the file on the device (see Section 3.5 for more details)
 - Whether the file passed the integrity test (see Section 3.5)
 - Whether the program can be debugged. A program can be debugged if it does not refer to addresses above 0xFC00 in the program memory.
 - Flash usage: The bars indicate how much of the Flash is being used by the current program. Ramtron MCUs with a JTAG interface typically have 64KB of Flash memory for user programs. These indicators do not take into account empty space or the space occupied by a file already in the Flash.

- RAMTRON
- Debug. How much space the program occupies, taking into account that debugging requires 0xFC00 to 0xFFFF for mapping.
- Release. How much space the program occupies without reserving space for debugger mapping.

3.5.3 Working with Multiple Files

To use multiple files simultaneously, the Versa Ware JTAG Programmer allows more than one file information windows to be open at once. However, only one file can be programmed at a time. The selected file is displayed in the title bar of the main application window, and is the active window in the program. In Figure 7, the active window is *YourCode.ihx*. This will be the file used to program the device until the window is closed, another window is opened, or another file is opened.



Figure 7: Two file information windows open

3.5.4 Synchronize



Synchronize configures the communication protocol between the software and the target device, resetting the target device in programmer mode. If the power is not being controlled automatically, there may be a prompt requesting a power cycle.



Figure 8: Manual Power Control

3.6 Flash Menu

3.6.1 Erase then Program

This will erase the entire Flash memory and load the current file onto the device. This is the recommended method to program the target device: Erase then Program is the only way to debug a program or apply a security setting.



3.6.2 Erase

This erases the entire Flash: It wipes the device clean for storage and is the only way to eliminate a security setting on a device (see Section 3.9 for more details on securing a device).

3.6.3 Erase Page



This erases one or more blocks of memory. The Flash on Ramtron's VRS51L2070/3074 is separated into 128 distinct blocks of 512 bytes for the purpose of partial erasing. A dialog box will ask for the page(s) to erase.

Erase Page	×
Select page(s) to erase From: Page 10 (0x1400) 12 pages To: Page 21 (0x2BFF)	
<u>E</u> rase <u>C</u> ancel	

Figure 9: Erase Page Dialog

3.6.4 Program

Program loads the file specified in the File Information Window onto the device without performing a Flash Erase. This is useful for loading supplemental data or code into the Flash after it was initially programmed with the Erase then Program function and for unsynchronized loading of data and programs. For example, Program can be used to load a sensor look-up table into the Flash.

A write error may occur during programming if the current files are written to locations that were not previously erased. If the Verification option is activated (this is strongly recommended, see Section 3.8.4), and an overlap condition occurs between two files, an error message will appear. An overlap will occur between two or more files that contain different data at the same address.



3.6.5 Read Flash

This will download the Flash contents into a text file compatible with the Intel Hex file format. A dialog box will be displayed indicating the destination and portion of the Flash to be read. After reading the Flash, the result can be displayed in Notepad automatically, if this option is selected.

Read Flash	×
Reading range From: 0x2200 20480 Bytes To: 0x71FF Read <u>A</u> I	
Save location Untitled.hex View File in Notepad after reading	
Read Cancel]

Figure 10: Dialog Box for Flash Reading

3.7 Device Operation Control Menu

3.7.1 Run

Executes the program loaded onto the target device: The device is placed in JTAG Run Mode, which will allow communication via the JTAG while the device is running. In this mode, the boot-up clock divider is capped to a minimum of Main Clock / 128. For more details, see Section 3.8.1.

3.7.2 Debug

Debug runs the loaded program in JTAG Debug Mode. Please see sections 4 to 6 for more information.

3.7.3 Reset

Reset sends a reset pulse to the target device. An MCU reset does not affect the JTAG circuitry, therefore, communication is unaffected. Reset works best when the device is in JTAG Run Mode.

3.7.4 Device Options



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This button opens the Device Options dialog for configuring the device. Please see Section 3.8 for more information.



3.8 Versa Ware JTAG Device Options

Device Options		
Boot-up Clock Divider: Off	Verification Verify entire flash Verify programmed file only Do not verify (not recommended)	
Programming ✓ Enable debugging ✓ Automatic power control ✓ Run device after programming Close previous file when opening	Security Do not secure flash Secure flash this time only Always secure flash Warn when removing security Warn when secured device is found	
MCU: VR551L3074-40-Q	OK Cancel	

Figure 11: Device Options Dialog for the VRS51L3074

3.8.1 Boot-up

Configure the target device via the Device Options dialog box (see Figure 11). These settings cannot be changed without a properly connected target device.

- **Clock Divider:** This sets the speed at which the device will boot up. This is useful for applications that require low power consumption upon device startup.
 - Off will boot the device at the maximum speed
 - The clock divider is adjustable in factors of 2 down to 32768.
 - Note that when the device is in JTAG Mode, the clock divider is limited to main clock / 128.
- **FRAM is read only:** This will disable writes to the onboard FRAM. This option is only applicable to FRAMenhanced devices, such as the VRS51L3074.



For example, if using the self-oscillator on a VRS51L2070, the frequencies at boot-up for the clock dividers are:

Clock divider	Frequency
Off	40 MHz
2	20 MHz
4	10 MHz
8	5 MHz
16	2.5 MHz
32	1.25 MHz
64	625 kHz
128	312.5 kHz
256	156.25 kHz
512	78.2 kHz
1024	39.1 kHz
2048	19.5 kHz
4096	9.8 kHz
8192	4.8 kHz
16384	2.4 kHz
32768	1.2 kHz

Table 3: Boot-up Clock Divider settings for the VRS51L2070 Self-Oscillator

3.8.2 Enable Debugging

This option enables debugging of the program loaded onto the device. Activation of the in-circuit debugger and the Flash security functions are mutually exclusive.

3.8.3 Automatic Power Control

An MCU reset does not affect the JTAG circuitry; therefore, a power cycle may be required to ensure that the device is in JTAG Mode. When a VersaKit development board is being used, the software can control the power of the device automatically. Otherwise, the Automatic Power Control checkbox must remain unchecked in order to synchronize with the device. (See section 3.5.4)

3.8.4 Verification of Flash Content

After programming, the Flash memory is read back to ensure that it was programmed correctly. Verification settings include:

- Verify the Entire Flash: Every value is read back and areas that were not programmed are checked to ensure that they are set to 0xFF.
- Verify Programmed File Only: This will only inspect for programming errors. Areas that were not programmed will not be checked. This is the default option, and is faster than verifying the entire Flash.
- **Do Not Verify:** This skips the verification process. It is not recommended, but offers the fastest programming.

During a Program operation, if activated, the Flash verification process will only be performed in the section of Flash referenced in the Hex file that was used as a source for the programming, even if Verify the Entire Flash is selected.

3.9 Security



The Versa Ware JTAG Programmer includes a Flash security option to prevent further reading/writing. If security is enabled, the next time a program is loaded into the Flash, the memory will be inaccessible. Any attempt to program or read the Flash will always result in 0xFF. A user program can still modify the Flash and access the Flash via code. Secure devices cannot be debugged.

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There are three options to secure a device, accessed via the Programming Options window:

- **Do Not Secure Flash:** The default option. No protection is applied.
- Secure Flash This Time Only: This enables security options for the next programming operation only. The security option will not be applied to the next device programmed.
- Always Secure Flash: This enables security for all subsequent devices until this setting is changed.

The device will not be secure until the next Erase then Program is executed (see Section 3.6.1).

SEC will be displayed on the bottom right of the window when the security option is enabled (see Figure 12).



Figure 12: Security Option Enabled

3.9.1 Synchronizing with a Secured Device

When the JTAG software synchronizes with a secured device, the following message is displayed:



Figure 13: A Secured Device

3.9.2 Removing Security

The security setting can be changed by clicking Flash Erase. Upon the first attempt to remove security, a warning message will be displayed:

Versa Ware JTAG	×	
Is this the intent?	remove security settings. E MADE VIEWABLE BY THIS	
<u>Y</u> es	No	
Don't ask me again (re-enable in Device Options)		
Figure 14: A Protected Device		

Click <No> to maintain device security. Click <Yes> to erase the device and remove its security.

Note: The contents of a secure device cannot be made viewable by removing device security.



4 Using the Versa Ware JTAG Debugger

The Versa Ware JTAG Software incorporates a friendly user interface to interact with the in-circuit debugging features of all Ramtron microcontrollers equipped with a JTAG interface.

The Versa Ware JTAG Debugger provides a link between the in-circuit debugger and the source code. It allows the user to monitor program execution, set breakpoints, single step through the code, and read/modify memory locations. The in-circuit debugger also provides advanced features such as program tracing and variable watch.

The following figure shows the Versa Ware Debugger in action:

ersa Ware JTAG - Watch						_ 7
e Edit View Breakpoint Watch Window Help						
= Þ M 🔗 🎧 🔕 🔍 🍭 🍭 🍬 💊 = 34 🧶 🚭 🗟 🗟 🗟 🧮 🚍 🖽						
unsigned int dacdata BP1: Program 0x00E0 BP2: DPS BP3: not set						
'our_Application.ihx	RAM					-0
C [213] PWMCFG = 0x17; //Point to MSB MID	Name	Address	Bin	Dec	Hex	ASCII
a 00DD mov PWMCFG,#0x17		0x2D	0000 0000	0	0x00	0
C [214] PWMDATA = 0xA2; //		0x2E	0000 0000	0	0x00	0
00E0 mov _PWMDATA,#0xA2		0x2F	0000 0000	0	0x00	0
C [215]	char fircoefh[]	0x30	0000 0010	2	0x02	0
C [216] PWMCFG = 0x07; //Point to LSB MID	+>	0x31	0000 0100	4	0x04	0
	+>	0x32	0000 1000	8	0x08	0
$ \begin{bmatrix} 217 \end{bmatrix} PWMDATA = 0xC2; $	+>	0x33	0000 1101	13	0x0D	0
a 00E6 mov _PWMDATA,#0xC2	+>		0001 0010	18	0x12	л П
C [218]	1	1 112.14			1812	
	R SFR Page 0					
C [220] //Configure and Enable PWM as timer Interrupt to monitor PWM5 o: [221] INTSRC2 &= 0xDF; //PWM7:4 Timer module Interrupt	Name	Address	Bin	Dec	Hex	ASCII
	PO	0x80	1111 1111	-1	0xFF	ÿ
					1.0000010.	y y
00E9 anl _INTSRC2,#0xDF	SP	0x81	0000 0111	7	0x07	
OE9 anl _INTSRC2,#0xDF	SP DPL0		0000 0111	7	0x07 0x00	9 0 0
		0x81		200		0
	DPLO	0x81 0x82	0000 0000	0	0x00	0 0 0
four_Application.c	DPL0 DPH0	0x81 0x82 0x83	0000 0000	0	0x00 0x00	0 0 0
	DPL0 DPH0 DPL1	0x81 0x82 0x83 0x84	0000 0000 0000 0000 0000 0000	0 0 0	0x00 0x00 0x00	0 0 0
Your_Application.c Image: Constraint of the second secon	DPL0 DPH0 DPL1 DPH1	0x81 0x82 0x83 0x84 0x84 0x85 0x85	0000 0000 0000 0000 0000 0000 0000 0000	0 0 0 0 0	0x00 0x00 0x00 0x00 0x00	0 0 0 0
Our_Application.c Image: Constraint of the second seco	DPL0 DPH0 DPL1 DPH1 DPS PCDN	0x81 0x82 0x83 0x84 0x84 0x85 0x85	0000 0000 0000 0000 0000 0000 0000 0000	0 0 0 0	0x00 0x00 0x00 0x00 0x00 0x00	
Our_Application.c Image: Construction of the second se	DPL0 DPH0 DPL1 DPH1 DPH1 DPS	0x81 0x82 0x83 0x84 0x84 0x85 0x85	0000 0000 0000 0000 0000 0000 0000 0000	0 0 0 0	0x00 0x00 0x00 0x00 0x00 0x00	
our_Application.c Image: Comparison of the second seco	DPL0 DPH0 DPH1 DPH1 DPS PCDN R Watch Name	0x81 0x82 0x83 0x84 0x84 0x85 0x85	0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 01110 0000 Memory	0 0 0 0 0 0 8 0 0 0 0 0 0	0x00 0x00 0x00 0x00 0x00 0x60 nx60	
our_Application.c Image: Comparison of the second seco	DPL0 DPH0 DPH1 DPH1 DPH1 PF0N PF0N ₹ Watch Name +->	0x81 0x82 0x83 0x84 0x84 0x85 0x85	0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0111 0000 Memory IRAM	0 0 0 0 1 0 1 0 0	0x00 0x00 0x00 0x00 0x00 0x00 nx60 ress	
Your_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (will be monitored by interrupt) // // PWM Timer 7 counts from 0000 to A2C2h PWMCFG = 0x17; //Point to MSB MID PWMDATA = 0xA2;	DPL0 DPH0 DPH1 DPH1 DPS PCDN R Watch Name	0x81 0x82 0x83 0x84 0x84 0x85 0x85	0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 01110 0000 Memory	0 0 0 0 0 0 0 0 0 0	0x00 0x00 0x00 0x00 0x00 0x60 nx60	
'our_Application.c Image: Construct of the second seco	DPL0 DPH0 DPH1 DPH1 DPH1 PCDN PCDN ₹ Watch Name +-> +-> +-> +->	0x81 0x82 0x83 0x84 0x84 0x85 0x85	0000 0000 0000 0000 0000 0000 0000 0000 0110 0000 II10 0000 IRAM IRAM IRAM IRAM	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x00 0x00 0x00 0x00 0x00 0x60 0x60 x68 x68 x68	
Your_Application.c PWMCLKCFG = 0x10; //PWM Timer 7 Prescaler = Sys Cl //Configure PWM7 as Timer (will be monitored by interrupt) // PWM Timer 7 counts from 0000 to A2C2h PWMCFG = 0x17; //Point to MSB MID PWMDATA = 0xA2; // PWMDATA = 0xC2; //Point to LSE MID	DPL0 DPH0 DPH1 DPS PCDN R Watch Name +-> +-> +-> +->	0x81 0x82 0x83 0x84 0x84 0x85 0x85	0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0110 0000 III 00	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x60 0x60 x68 x68 x68 x68 x68 x68	
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Your_Application.c PWMCLKCFG = 0x10; //PWM Timer 7 Prescaler = Sys Cl //Configure PWM7 as Timer (will be monitored by interrupt) // PWM Timer 7 counts from 0000 to A2C2h PWMCFG = 0x17; //Point to MSB MID PWMDATA = 0xA2; // PWMDATA = 0xC2; //Point to LSE MID	DPL0 DPH0 DPH1 DPS PFGN R Watch Name +-> +-> +-> +-> +-> +-> +-> +->	0x81 0x82 0x83 0x84 0x85 0x86 0x86	0000 0000 0000 0000 0000 0000 0000 0000 0110 0000 II10 0000 II10000 II1000 II10000 II1000 II100000 II1000 II10000 II100000 I	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x00 0x00 0x00 0x00 0x00 0x60 0x60 0x60	U U U Value
Your_Application.c PWMCLKCFG = 0x10; //PWH Timer 7 Prescaler = Sys Cl //Configure PWM7 as Timer (will be monitored by interrupt) // PWM Timer 7 counts from 0000 to A2C2h PWMCFG = 0x17; //Point to MSE MID PWMCFG = 0x17; //Point to LSE MID PWMCFG = 0x07; //Point to LSE MID PWMCFG = 0x02; // //Configure and Enable PWM as timer Interrupt to monitor PWM5 or INTSRC2 &= 0xDF; //PWM7:4 Timer module Interrupt	DPL0 DPH0 DPL1 DPH1 DPS PCDN R Watch Name +-> +-> +-> +-> +-> +-> +-> +-> +->	0x81 0x82 0x83 0x84 0x85 0x86 0x86	0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0110 0000 IRAM IRAM IRAM IRAM IRAM IRAM IRAM	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x60 x68 x68 x64 x68 x65 x66 x66 x66	

Figure 15: Versa Ware JTAG Debugger



4.1 General Requirements for the Debugger

In order for the Versa Ware Debugger to work properly, all the files generated by compiling or assembling should be grouped into the same directory. No changes are made to these files.

The following development environments, compilers and assemblers are currently supported by the Versa Ware JTAG Debugger:

- Keil µVision3 development suite
- Raisonance RIDE 51 development suite
- MetaLink Cross Assembler
- AS31 Cross Assembler
- ASX8051 Cross Assembler
- SDCC (Small Device C Compiler)

4.2 Required Files for Debugging

Each development environment produces different file outputs for use with the debugger. The following table lists the files required for optimal debugging. All files must have the same root name (see Section 4.2.1) and all files must be in the same directory.

Development Environment	Required Files
SDCC	.ASM for each source file
	.C for each source file
	.IHX
	.RST for each source file
Raisonance RIDE 51	.AOF
	.HEX
	.LST for each source file
	.M51
	Assembler source files
	C source files
Keil µVision3	(No extension)
	.HEX
	.LST for each source file
	.M51
	.UV2
	Assembler source files
	C source files
MetaLink Cross Assembler	.ASM
	.DBG
	.HEX
AS31 Cross Assembler	.HEX
	.LST
ASX8051 Cross Assembler	.ASM
	.IHX
	.RST

Table 4: Files Required for Proper Debugging

Consult the preferred development suite user guide for instructions on generating the required outputs.

4.2.1 Example Projects

Your_Application.C (as seen in all figures) was created using SDCC. These files are necessary to run the debugger:

- Your_Application.C
- Your_Application.ASM
- Your_Application.IHX
- Your_Application.RST

If a project named Example was created using Keil µVision3, and consisted of File1.C and File2.C, the required files for debugging are:

- Example (no extension)
- Example.HEX
- Example.M51
- Example.UV2

- File1.C
- File1.LST
- File2.C
- File2.LST

4.2.2 Variable Extraction

All of the supported environments, with the exception of ASX8051 and AS31, can have the variable names used in development automatically extracted and placed next to their mapped addresses. For SDCC, the --debug option must be used when compiling to create a .CDB file for variable extraction, but this is not mandatory. Symbols in the assembler that are assigned using the EQU statement are not extracted. SFR names are extracted according to the connected device, not the development environment.

4.2.3 Multiple File Projects

SDCC, Raisonance RIDE 51, and Keil µVision3 can have multiple source files to generate a Hex file. All files must be in the same directory. Follow the development environment's user guide for setup instructions. For SDCC, if there is more than one source file, the --debug option must be used when compiling to create a .CDB file.

4.3 Debugger Commands Overview

The following table shows all of the possible commands for the debugger:

Command	Toolbar	Toolbar button	Menu	Keyboard Shortcut
Run	Debugger		Action	F7
Step	Debugger		Action	F6
Halt	Debugger		Action	Ctrl + Backspace
Restart	Debugger	1	Action	
Jump	Debugger	Ŕ	Action	
Stop Debugging	Debugger		Action	
Сору			Edit	Ctrl + C
Find			Edit	Ctrl + F
Find next			Edit	F3
Go to			Edit	
Refresh	Debugger		View	Ctrl + R
View SFR	Debugger	Q	View	Ctrl + Shift/Alt + S
View IRAM	Debugger		View	Ctrl + Shift/Alt + I
View XRAM	Debugger	8	View	Ctrl + Shift/Alt + X
View Program Trace	Debugger		View	Ctrl + Shift + T
View Watch	Debugger	Q	View	Ctrl + Shift + W
View C files	View	C	View	
View Assembler files	View	a	View	
View Address Tree	View		View	Ctrl + Shift + S
View Toolbars			View	
View Options			View	Ctrl + Shift + V
Toggle Breakpoint 0			Breakpoint	Ctrl + B
Toggle Breakpoint 1 - 5			Breakpoint	Ctrl + F1 to Ctrl + F5
Breakpoint Settings	Debugger	2	Breakpoint	Ctrl + Shift + B
Add Watch	Debugger	•	Watch	
Edit Watch	Debugger	N	Watch	
Force Watch	Debugger	34	Watch	
Remove Watch	Debugger		Watch	
Break on Value	Debugger		Watch	
Disable Value Breakpoint			Watch	
Cascade	View	F	Window	
Tile	View		Window	
60:40 Horizontal	View		Window	
75:25 Vertical	View		Window	
About			Help	
Erase then Program	Program	&	Flash	F5
Erase page	Program	8	Flash	
Read flash	Program		Flash	

Table 5: Debugger Command Set



4.4 Processor Controls

4.4.1 Run

This command lets the program operation continue at full speed from the current program counter location.

4.4.2 Single Step

This command serves to execute one line of code at a time. This is like setting a breakpoint after each instruction.

4.4.3 Halt Execution

This command unconditionally stops the processor. While the program is running, it may be useful to stop the processor in order to verify where the program is currently running.

4.4.4 Restart

This command restarts the program from address 0x0000. This is particularly useful if the program has passed a breakpoint, or if multiple analyses of the program are being performed. Restart does not reset memory locations.

4.4.5 Jump

Use this command to jump anywhere in the program unconditionally. A dialog will open requesting a location in Flash to jump to. Be careful when using this command, because no check is performed to verify if the target location is valid. For instance, if a jump to location falls between instructions or within a data block, device operation might become erratic.

4.5 Memory Controls

Industry standard 8051 derivatives, such as Ramtron MCUs, include four main types of memory locations.

- **Program Memory:** Also known as code space, this is where the program resides. Any operation on code space is done by the programmer (see Section 3 for more details). Debugging is interrupted when reading the Flash, erasing a page or reloading a program.
- Internal SRAM: Also known as data and idata, this memory space provides the fastest access. It is referred to by the debugger as IRAM.
- External SRAM: Also known as xdata and pdata, this memory area refers to the 4KB of SRAM mapped from 0x0000 to 0x0FFF on the external data memory bus, and provides more storage. It is referred to by the debugger as XRAM, although it is integrated into the device.
- **Special Function Registers:** Also known as SFR's, these registers provide access to on-chip peripherals. Ramtron JTAG devices, such as the VRS51L2070/3074, have two SFR pages.

These controls serve to monitor and modify the memory content:

- SFR
- View IRAM
- View XRAM
- • View Program trace

Each of these controls opens a window that displays a selected portion of the device's memory. Portions of SFR, IRAM, and XRAM can be viewed simultaneously via the Watch List. Please see Section 5 for more details.



4.6 Memory List Views

When the View SFR, View IRAM or View XRAM commands are applied, a window showing a grid is displayed with the current contents of each memory space:

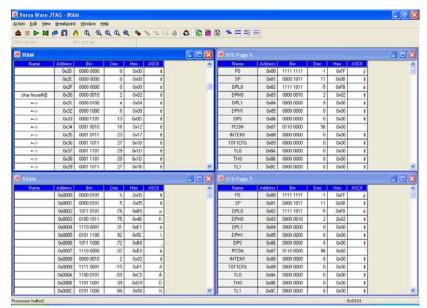


Figure 16: Memory List Views (Code Minimized)

4.6.1 Changing Memory / SFR Content:

It is possible to manually change the memory content by double clicking any cell, making the change and pressing <Enter>. If this is an SFR window, the entire contents will be refreshed, otherwise, only the cell will be refreshed. The displayed value is always guaranteed to be current. The editor will try to format according to the current display type. For more information on display types, see Section 4.6.3.



Warning:

- Changing content directly may have unintended consequences on program flow or peripheral operation.
- Some SFR addresses are partially or completely read-only and cannot be overwritten. The device will not be damaged if you attempt to write to a read-only register.
- Some peripherals must be enabled before their associated SFR can be changed.
- If the processor is stopped within a program segment that is executing from XRAM, the debugger will not display correct XRAM values because the hardware has disabled the external memory. For more information on how code can be run from the XRAM, please consult the device datasheet.
- Do not edit XRAM values if the processor is stopped within a program segment that is executing from the XRAM. For more information on how code can be run from XRAM, please consult the device datasheet.

4.6.2 Variable Names

As shown in Figure 16, it is possible to enter text next to a location in IRAM or XRAM. This can be a variable name or a meaningful comment. To do so, double click any cell, make the change and press <Enter>. Where possible, variable names are automatically extracted, and any changes will automatically update the Watch List.



4.6.3 Changing the Display

The View menu can be used to alter the display by checking the appropriate menu item. Checking an item from the View Column menu will display the column, unselecting the item will remove the column from display. At least one address column and at least one value column must remain visible.

The menu items are as follows:

- Name: The name of the location
- Address: The name address of the location
- ASCII: The ASCII character associated to the value
- Bin: The value of the SFR in binary
- Hex: The value of the SFR in hexadecimal
- Decimal: There are two ways to display values in decimal
 - **Unsigned:** Values of bytes are displayed between 0 and 255
 - Signed: Values of bytes are displayed between -128 and 127

4.7 Memory Table Views

When View XRAM Table or View XRAM Table commands are applied, a grid will be displayed with the contents of each memory space.

tion Edit	Yew I	reakpoint	: <u>Window</u>	r Help													
		n 1	0	6 8 0	10 Q	· · ·	1253	0		e 👟							
		-	PI not per					and the second									
		_		_		-											600.000
IRAM																	
00	0 0.4F	0.00	2 0x10	0x30	4	5 0x00	0.00	0.00	8 0.FF	9 0x0F	0.02	B 0x00	0.01	0.01	0,00	0.00	
10	DIFB	0x02	0x10	0x30	0x00	0.00	0x00	0.00	De4F	0.00	0x01	0x35	0.01	0x00	0x00	0.00	
20	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0.00	0x00	0x00	0x00	0x00	0x00	0x00	0.00	0x00	
30	0.02	0,04	0x08	0.00	0x12	0x17	0x18	0x1D	0x1D	0x1B	0x17	0x12	0.00	0x08	0x04	0x02	
40	0x30	0,90	0.64	0.00	0.63	0,52	0x30	0,51	0,51	0x30	0,52	0x63	0x20	0.64	0,90	0x30	
50	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	
60	0.FF	0xFF	0xFF	0.FF	DuFF	0.FF	D.FF	0.FF	DJFF	DJFF	0.FF	0.FF	D.FF	0.FF	0.FF	DuFF	
70	0xD3	0x0F	0x00	0.00	0x00	0x00	0x00	0x00	0.00	0x00	0x00	0x00	0x00	0x00	0x00	0,00	
80	0.00	0.00	0.00	0.00	0x00	0.00	0.00	0.00	0.00	0.00	0,00	0.00	0.00	0.00	0.00	0.00	
90	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0.00	0x00	0x00	0x00	0x00	0x00	0.00	0x00	
AD	0.00	0.00	0x00	0.00	0.00	0.00	0м00	0.00	0.00	0x00	0.00	040	0.00	0.00	0.00	0.00	
80	000	0.00	0x00	0x00	0+00	0.00	0x00	0x00	0.400	0x00	0H00	0x40	0640	0x00	0.400	0.400	
C0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0.00	0x00	0x00	0x00	0x00	0x00	0.00	0.00	
XRAM																	- 0
	0 1	1	2 1			5 1	6	7 1	8 1	9	A	8	c 1	0	E I		Loff Lo
000	0.05	0.05	0.85	Ox4B	0xE1	0.50	0.88	0.£0	0.02	0xF1	0xC5	D _b D9	0,58	0.50	0x4C	DiFA	
010	0xC9	Dx9A	0xE1	0.60	0.87	0x88	0xAB	0x8A	0.F8	0.00	0.DC	0xE6	0x72	0x7F	0xEA	0x6C	
020	0x3C	0x30	0x08	0x36	0x98	0x36	0x00	0.50	0xDE	DEE	0x7C	Dx1D	0x43	0x75	0x2A	0x32	
030	0x49	0.SE	0.01	0x5A	0x20	0x64	0xF4	0.02	0.AG	OxA4	0xE1	0.24	0,29	0.63	0x61	0x04	
040	0x63	0.06	0xF2	0xF6	0x0A	0xEE	0x19	0xC9	0.06	0x01	0x53	0x52	0xAE	DeAF	0x01	0x42	
050	0x2F	0x58	0x9E	0xC5	Qv4C	0x4D	0.00	0x7A	0x77	0x58	0x1C	0xFC	0xFC	0+43	0xC7	0xC2	
060	0xE7	0x8A	0x48	0x61	0x06	0.400	0x4E	0x85	0x77	0x0F	0xCE	0x68	0x27	0x30	0x33	0x79	
070	0xBC	0x03	0x51	0.56	0x5E	0.63	0x20	0x23	0xED	0x59	0xAC	0.FB	0xAA	0x0C	0×79	0x1D	
080	0x54	0x72	0x58	0x66	0xAC	0x83	0x58	0x4D	0x0F	0x83	0x2F	0x65	0x8E	0x9F	0x88	0xF1	
090	0x34	0x2C	0.0F	0.63	0.40	0.05	0x07	0+03	0x70	(h/SF	0x2C	0x26	0x2E	(b/2)E	0x2C	0x77	
040	0x8D	OxA1	0x1D	0x62	8x95	0x37	0x89	0.65	0.07	OxAF	0x49	0x20	0xE8	0xFA	0xA8	0xFD	
080	0.80	0.65	0,68	0x1D	0.05	DvE7	0x21	0xD1	0x24	0.61	0,59	0x1F	0xF1	0,69	0x10	0x64	

Figure 17: External Memory and Internal Memory Table Views (Code Minimized)

4.7.1 Changing Content:

It is also possible to manually change the memory content when table view is activated. To do so, double click any cell, make the change and press <Enter>. The cell will then be refreshed.



Warning:

- Changing content directly may have unintended consequences on program flow or peripheral operation.
- If the processor is stopped within a program segment that is executing from XRAM the debugger will not display correct XRAM values. This is due to the hardware disabling external memory. For more information on how code can be run from external RAM, please consult the target device datasheet.
- Do not edit XRAM values if the processor is stopped within a program segment that is executing from the XRAM. For more information on how code can be run from XRAM, please consult the target device datasheet.

4.7.2 Changing the Display

The View menu can be used to alter the display by checking the appropriate menu item. Clicking an item from the View Type menu will change the display accordingly. The menu items are:

- **ASCII:** The ASCII character associated to the value
- **Bin:** The value of the SFR in binary
- **Hex:** The value of the SFR in hexadecimal
- Decimal: There are two ways to display values in decimal
 - **Unsigned:** Values of bytes are displayed in between 0 and 255
 - Signed: Values of bytes are displayed in between -128 and 127

4.8 Program Trace

Clicking on the program trace button will show the last 23 branches taken. The most recent branch is #23 and the least recent is #1. Double-click on any address to scroll the tree view to the appropriate address.

	AG - Your_Application.ihx		
	Breakpoint Watch Window Help		
	۵ ۵۵ – ۲۰۰۰ ۲۵ ۹۹ ۹۹ ۹۹ ۹۰ ۲۰۰۰ ۲۰۰۰ ۱۵		
BPO not set	BP1 not set		
R Your_Applica	tion.ihx	💶 🗖 🔀 🗷 Program Trace	
-C [226]	// Copy FIR filter Coefficients to IRAM	Branch Address	
B C [227]	CopyFIRCoef();	1 0x01A1	
- OOF5	lcall _CopyFIRCoef	2 0x018F	
- C [228]		3 0x01A1	
C [229]	//Activate the PHM modules and configure the PHM m	odules as Time: 4 0x01E6	
B € [230]	PihEN = 0x00; //Enable Pih 7	5 0x026A	
-8 00F8	or1 _PWMEN,#0x80	6 0x0246	
B C [231]	PERIPERIA = 0x00; //Enable PER 7 as	Timer 7 0x0101	
- 8 00FB	orl _PUMTMPEN, #0x80	8 0x01A1	
C [232] ■ C [233]	GENINTEN = 0x01: //Enable Global interrupt	9 0x018F	
- 0 00FE	nov _GENINTEN, #0x01	10 0-0141	
C [234]	LOV _OEMINIEN, POXOI	11 0x018F	
C [235]		12 040141	
□ C [236]	while(1):	13 0x018F	
0 0101	001024:		
C [237]		14 0x01A1	
C [238]		15 0x018F	
B > [239])//	f End of main	16 0x01A1	
> 0101	sjmp 001024	17 0x01BF	
-C [240]		18 0x01A1	
	Interrupt Function(s)		
		2.1 000101	
-C [244]		22 0x01A1	
· · · · · · ·		23 0x018F	
-C [246] //			
	DESCRIPTION:		
C [249] //			
C [250] //			
C [230] //	and the state of t	× .	
<	U		

Figure 18: Program Trace

When in JTAG Debug Mode, the target device records the address of the instruction when it performs a jump with any of the following 8051 instructions: AJMP, LJMP, SJMP, JC, JNC, JB, JNB, JBC, JMP, JZ, JNZ, CJNE, and DJNZ. This is done without a performance hit to the processor.



The display is only refreshed when the processor stops or when the window is first displayed. If the program is running when the window is opened, the processor will halt.

4.8.1 Looping Modes:

The Program Trace features two looping modes: repeat and skip. Skip Mode, the default, will only record a branch once per loop. Repeat Mode will record all of the branches. The following example shows the difference between the two modes:

ORG 20	00h	
Start:		
	MOV	A, $\#10$; Load ACC with 10
Loop:		
	DEC	A
	JNZ	Loop
	LCALL	Function ; Call a function
	JMP	Start
ORG 30	00h	
Functi	on:	
	RET	; Dummy function

Branch	Loop Repeat	Loop Skip
1	0x2003	0x2003
2	0x2003	0x2005
3	0x2003	0x2008
4	0x2003	0x2003
5	0x2003	0x2005
6	0x2003	0x2008
7	0x2003	0x2003
8	0x2003	0x2005
9	0x2003	0x2008
10	0x2003	0x2003
11	0x2005	0x2005
12	0x2008	0x2008
13	0x2003	0x2003
14	0x2003	0x2005
15	0x2003	0x2008
16	0x2003	0x2003
17	0x2003	0x2005
18	0x2003	0x2008
19	0x2003	0x2003
20	0x2003	0x2005
21	0x2003	0x2008
22	0x2003	0x2003
23	0x2005	0x2005

Table 6: Difference between Program Trace Modes

Notice that repeat mode records each time JNZ jumps, except when ACC is equal to 0. Loop Skip Mode will only show that there was a branch taken at 0x2003, but not how many times it was taken.

To use Skip Mode, select menu item "No Duplicate Addresses" in the Edit menu. Uncheck this item to repeat loops. Every time this is done, the program trace is cleared.

The program trace can also be cleared by selecting Clear from the Edit menu.

To determine how many times a section of code has looped, set a breakpoint both before and after the loop in the program memory. When the first breakpoint hits, open the Program Trace window, and uncheck "Do not repeat loops"

(if it is already unchecked, select Clear from the Action menu). Disable the breakpoint and click Run. When the second breakpoint hits, the Program Trace window will display how many times the program looped. This works best for small loops.

Note:

- Interrupts are not recorded by the program trace, but the jump to the ISR from the interrupt vector is.
- Function calls (ACALL and LCALL) are not recorded by the program trace.

4.9 Source Views

These views (assembler source and C source views) are copies of the raw source file, and contain embedded debugger information. The syntax is highlighted for easy viewing. Clicking on a line will show where the line of code is mapped to the address in the status bar. This allows for easy breakpoint setting. See Section 4 for more information on breakpoints.

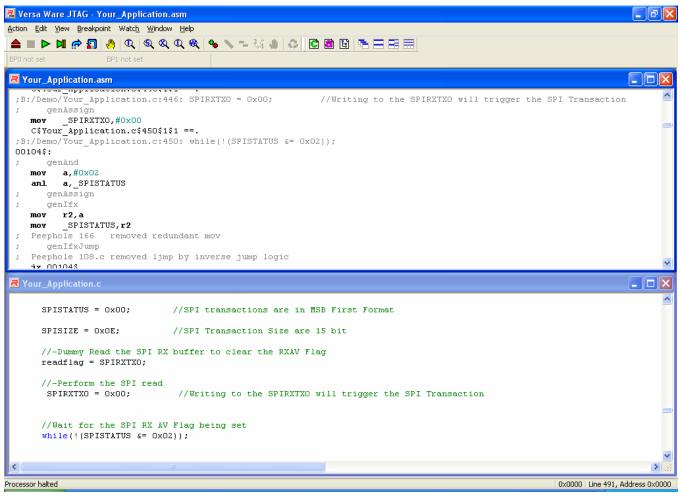


Figure 19: The Assembler View and C Source View

amr



4.10 Address Tree

This view provides a better visual of how C source code is mapped to instruction addresses. Clicking on a line will show where the line of code is mapped to the address in the status bar. This allows for easy breakpoint setting. See Section 4 for more details on breakpoints. At any time, a tree can be expanded or contracted. This view is only available for projects using C as the primary language.

<pre>BOD: Program Du024F BOD: Program Du024F BOD: Program Du024F C [455] C [456] C [457] C [458] C [459] C [459] C [459] C [451] D DD: c [451] D DD: c [452] C [453] C [453] C [453] C [454] C [455] C</pre>	🛽 Versa Ware JT/	AG - [Your_Appli	ation.ihx]				
<pre>SPD: Program Du024F 091 rot set C [157] //Heast 4 System clock cycles after the White operation to the SFIRXIX0 register C [157] //Heast 4 System clock cycles after the White operation to the SFIRXIX0 register C [159] //-Wait for SFIROCS Flag have time to be updated C [160]ema C [161] BDP: C [162]endamn: C [163] C [164] C [164] //-Wait activity stops on the SFI interface C [165] //-Wait activity stops on the SFI interface C [166] //-Wait activity stops on the SFI interface C [167] */ C [168] C [167] // Sead SFI data accidate (SFIRXIX1 << 0); accidate (SFIRXIX1 <</pre>	Rtion Edit View	w <u>B</u> reakpoint Wato	<u>n W</u> indow <u>H</u> elp				_ 8 >
<pre>PD: Program Du024F BP: not set C [457]</pre>	📤 🔳 🕨 🕅 🧬) 🛐 🤚 🔍 🔍	l & Q & 💘 🐅 🔪 🖘 i	4 🌒 🛟 🖸 🔕			
C [456] //No that the reading of the SPISTATUS register must be done at C [457] //Least 4 System clock cycles after the Write operation to the SPIRATX0 register C [458] //-Tait for SPIRACS Flag have time to be updated C [460]	PO: Program 0x024F	BP1 not set				<u> </u>	
C [437] //Least 4 System clock cycles after the Write operation to the SPIRTX0 register C [439] //-Wait for SPINOCS Flag have time to be updated C [461]earn C [463]endasm: C [463]endasm: C [463]endasm: C [464] //-Wait activity stops on the SPI interface C [466] //-Wait activity stops on the SPI interface C [467] */ C [468] C [469] //Read SPI data C [470] adicdata = (SPIRXTX1 << 0);	-		that the reading of th	SPISTATUS regist	ter must be done a	at	
C [458] C [459] //-Wait for SPINOCS Flag have time to be updated C [461]							
<pre>C [459] //-Nait for SPINOCS Flag have time to be updated C [460]asm C [461]asm C [463] C [463] C [464] C [464] C [464] C [465] //Wait activity stops on the SPI interface C [466] //Wait activity stops on the SPI interface C [467] */ C [468] C [469] //Read SPI data a cov r2., SPINTX1 << 0; a co241 mov r2., SPINTX1 a co243 mov r3., 40000 a co245 mov (_adcdata + 1), r2 a co247 mov a, r2 b co248 mov r2., SPINTX0 a co241 mov a, r2 b co248 mov a, r3 a co251 movadcdata, a co253 mov a, r3 c [471] adcdata≤= KORFFF: //isolat the 12 lsb of the read value a co259 mov (_adcdata + 1), a c [473] C [473] //end of ReadGen_RDC c [473] //end of ReadGen_RDC</pre>		••			•	· · · · · · · · · · · · · · · · · · ·	
C [461] NOP: C [463]		//-Wait for SH	INOCS Flag have time to	be updated			
C [461] NOP: C [463]	C [460]	asm					
C [463] C [465] //-Wait activity stops on the SPI interface C [465] //-Wait activity stops on the SPI interface C [466] while(!(SPISTATUS 4= 0x00)); C [466] //Read SPI data C [469] //Read SPI data C [469] //Read SPI data C [470] adcdata= (SPIEXTX1 < C [469] //Read SPI data C [470] adcdata= (SPIEXTX1 < C [469] //Read SPI data C [470] adcdata= (SPIEXTX1 < C [470] adcdata= (SPIEXTX1 C [471] adcdata= SPIEXTX0; C [472] adcdata= SPIEXTX0; C [472] adcdata= SOUPE; //isolate the 12 lsb of the read value C [473] adcdata= SOUPE; //isolate the 12 lsb of the read value C [473] //end of ReadSen_RDC C [473]	C [461]						
<pre>C [464] C [465] //Wait activity stops on the SPI interface C [466] while(!(SPISTATUS &= 0x08)); C [467] */ C [468] C [479] adcdata= (SPIEXTX1 << 0); adcdata= (SPIEXTX1 << 0); adcdata= (SPIEXTX1 << 0); adcdata= (SPIEXTX1) adcdata= (SPIEXTX1) adcdata= SPIEXTX0; adcdata= SP</pre>	C [462]	_endasm;					
<pre>C [465] //Wait activity stops on the SPI interface C [466] while(!(SPISTATUS 4= 0x00)); C [467] */ C [468] C [469] //Read SPI data C [470] adcdata= (SPIEXTX1 << 0); C [470] adcdata= (SPIEXTX1 << 0); C [470] adcdata= 1),r2 C [470] adcdata= 1),r2 C [471] adcdata= SPIEXTX0; C [471] adcdata= SPIEXTX0; C [471] adcdata= SPIEXTX0; C [471] adcdata= SPIEXTX0; C [472] adcdata, a C [474] adcdata, a C [475] adcdata= 1),a C [475] adcdata= 1),a C [477] adcdata= 1), a C [477] adcdata= 1), a C [477] adcdata= 1), #ONOF C [477] adcdata= 0xEFF; //isolate the 12 lsb of the read value C [473] }//end of ReadGen_BDC C [473] }//end of ReadGen_BDC</pre>	C [463]						
C [466] while(!(SPISTATUS 4= 0x00)); C [467] */ C [469] //Read SPI data C [470] adcdata=(SPIRXTX1 << 0; adcdata=(SPIRXTX1 << 0; a 0241 mov r2,_SPIRXTX1 a 0243 mov (_adcdata + 1),r2 a 0247 movadcdata, \$0x00 a 0248 mov (_adcdata + 1),r2 a 0247 movadcdata, \$0x00 a 0244 mov r3, \$0x00 a 0244 mov r3, \$0x00 a 0242 mov a,r2 D 0244 add a_adcdata a 0251 movadcdata, a 0251 movadcdata + 1),a C [472] adcdata{= 0x0FFF; //isolat the 12 lsb of the read value a 0258 anl (_adcdata + 1), \$0x0F C [473] C [473] C [473]							
<pre>C [467] */ C [468] C [469] C [469] C [470] adcdata= (SPIRXTX1 << 8); a 0241 mov r2, SPIRXTX1 a 0 0243 mov r3, #0x00 a 0245 mov (_adcdata + 1), r2 a 0247 mov _adcdata, #0x00 a 0242 mov r2, SPIRXTX0 a 0244 mov r2, SPIRXTX0 a 0242 mov r3, #0x00 a 0242 mov r3, #0x00 a 0242 mov _adcdata, a a 0244 mov _adcdata, a a 0 0245 mov _adcdata, a a 0 0245 mov _adcdata + 1), a adcdata= 0 x0FFF; //isolate the 12 lsb of the read value a 0256 mov (_adcdata + 1), #0x0F C [473] C [473] C [473] C [473] C [473] </pre>		//Wait activ	ity stops on the SPI in	erface			
<pre>C [468] C [470] adcdata= (SPIRXTX1 << 8); accdata= (SPIRXTX1 << 8); accdata= (SPIRXTX1 << 8); accdata= SPIRXTX1 accdata= SPIRXTX1 accdata= synRXTX0; accdata= SPIRXTX0; accdata= SPIRXTX0; accdata= SPIRXTX0; accdata= SPIRXTX0; accdata= synRXTX0; accdata= s</pre>			TUS &= 0x08));				
<pre>C [469] //Read SPI data C [470] adcdata= (SPIRXX1 << 0);</pre>		*/					
<pre>C [470] adcdata= (SPIRXTX1 << 8);</pre>							
<pre> 0241</pre>							
<pre></pre>		-					
<pre> a 0245 mov (_adcdata + 1),r2 a 0247 mov _adcdata,#0x00 adcdata+= SPIRXTX0; a 024A mov r2,_SPIRXTX0 a 024A mov r3,#0x00 a 024E mov a,r2 b 024F add a,_adcdata a 0251 mov _adcdata,a a 0251 mov _adcdata,a a 0251 mov _a,r3 a 0254 addc a,(_adcdata + 1) a 0256 mov (_adcdata + 1),a adcdata6 0x0FFF; //isolate the 12 lsb of the read value a 0258 an1 (_adcdata + 1),#0x0F C [473] C [474] }//end of ReadGen_BDC a 025B ret </pre>			-				
<pre> d 0247</pre>							
<pre>> [471] adcdata+= SPIRXX0; a 024A</pre>			—				
<pre></pre>			-				
<pre> a 024C</pre>							
<pre> a 024E mov a,r2 b 024F add a,_adcdata a 0251 mov _adcdata,a a 0253 mov a,r3 a 0254 addc a, (_adcdata + 1) a 0256 mov (_adcdata + 1),a c [472] adcdata&= 0x0FFF; //isolate the 12 lsb of the read value a 0258 anl (_adcdata + 1),#0x0F c [473] c [473] c [473] c [473] c [475] </pre>							
<pre> 024F add a,_adcdata a) 0251 mov _adcdata,a a) 0253 mov a,r3 a) 0254 addc a,(adcdata + 1) a) 0256 mov (_adcdata + 1),a a) 0256 mov (_adcdata + 1),a c) [472] adcdata&= 0x0FFF; //isolate the 12 lsb of the read value a) 0258 anl (_adcdata + 1),#0x0F c) [473] c) [473] c) [473] c) [473] c) [473] c) [475] m</pre>							
<pre> 0251</pre>							
<pre>a 0253 mov a,r3 b 0254 addc a,(_adcdata + 1) b 0256 mov (_adcdata + 1),a c [472] adcdata&= 0x0FFF; //isolate the 12 lsb of the read value b 0258 anl (_adcdata + 1),#0x0F c [473] c [473] c [474] }//end of ReadGen_ADC b 025B ret c [475]</pre>	_						
<pre> a 0254 addc a,(_adcdata + 1) a 0256 mov (_adcdata + 1),a c [472] adcdata&= 0x0FFF; //isolate the 12 lsb of the read value a 0258 anl (_adcdata + 1),#0x0F c [473] c [473] c [474] }//end of ReadGen_ADC a 025B ret c [475] </pre>			-				
a) 0256 mov (_adcdata + 1),a C [472] adcdata&= 0x0FFF; //isolate the 12 lsb of the read value a) 0258 anl (_adcdata + 1),#0x0F C [473] C [474] J //end of ReadGen_ADC a) 025B c [475] m							
C [472] adcdata&= 0x0FFF; //isolate the 12 lsb of the read value a 0258 anl (_adcdata + 1),#0x0F C [473] C [473] C [474] }//end of ReadGen_RDC a 025B ret C [475]			-				
all (_adcdata + 1),#0x0F C [473] C [474] //end of ReadGen_ADC all 025B ret c [475]			—	12 lsb of the rea	ad value		
C [473] C [474] }//end of ReadGen_ADC 025B ret C [475]							
C [474] }//end of ReadGen_ADC 025B ret C [475]							
		}//end of Read	Gen ADC				
			_				
	C 14751						

Figure 20: Address Tree (Window Maximized)



4.11 Debugger View Options

This property dialog allows hundreds of configuration combinations for the Versa Ware JTAG Debugger:

View Options			X			
External RAM Display	Internal RA Assembler Font	M Ot C Font	her Settings SFR			
Windows Show on startu ♥Address tre Primary ass Primary ⊆ su	embler source file	Toolbars at startu Breakpoint 0 8 Breakpoint 2 8 Breakpoint 4 8 Debug Program	<1 <3			
Double-clicking Toggles Bre Does nothin <u>Asks</u> what t	akpoint <u>0</u> ig o do	 ✓ Yew ✓ Ask before exiting program ✓ Ask to stop if all windows close ✓ Ask before flash operations 				
Warn when n	ot all info is available	OK Cancel	Default Apply			

Figure 21: Debugger View Options

4.11.1 Display Options

This tab focuses on general display settings. In the "Windows" box, code view options are controlled.

- Show on startup: Indicates what views (if any) will be shown when debugging is first started.
- **Double-click options:** Determines the action to be executed when a code line is double-clicked.

The "Toolbars at startup" box shows which toolbars will be displayed, if any, when the debugger is launched. By default, they are docked to the top of the window.

The "Ask" and "Warn" checkboxes refer to pop-ups that may appear in special situations. These options may be unchecked here, or unchecked by checking "Don't ask/tell me again" when the dialog appears.

Warn when not all info is available: This will issue a warning if an attempt is made to debug C code compiled by SDCC without the "--debug" option. This situation does not prevent debugging, but prevents variable extraction.



4.11.2 Font Options

The "Assembler Font" and "C Font" tabs allow full control over the fonts and colors of syntax highlighting in code views. Tab stops can also be adjusted

View Options					
External RAM	1	Internal RAM		Oth	er Settings
Display	Ass	embler Font	⊂ Font		SFR
Font for text in wir	ndow:	Standard			Change
Font for key words		Key words			Change
Font for comments	:	Comments			Change
Font for character	strings:	Character S	tring		Change
Font for illegal char	racters:	Illegal			Change
Spaces per tab sto	p:	3			
					Default
		0	K C	ancel	Apply

Figure 22: Font Options

4.11.3 Memory View Options

The "External RAM", "Internal RAM", and "SFR" tabs control the operation of memory views.

View Options				
Display	Assembler Font	CF	=ont	SFR
External RAM	Internal RA	м	Ot	her Settings
 Automatically upd 	ate all locations			
When a break	point is reached			
	cessor <u>h</u> alts for any reason			
When any wir	ndow is enabled			
Never Never				
Toolbar button —				
Shows address	ses in <u>t</u> able format			
Shows address	ses in list format			
Asks which for	mat to show			Default
		ок	Cancel	

Figure 23: XRAM Options

Automatically Update All Locations: This setting allows the software to update views when stopped. Note that XRAM transfers can take about five seconds and can slow performance when stepping () through code.

Toolbar Button: This sets the behaviour of toolbar buttons **Q Q**. By default, clicking one of these buttons will ask which view to show.



4.11.4 Other Options

This is where the remaining options are located:

View Options				
Display	Assem	bler Font	C Font	SFR
External RAM		Internal RAM	0	ther Settings
Font for text in Add	fress Tree: 🛛	ſree		Change
Font for text in wat	ch list: 🛛	Watch List		Change
Auto-arrange win Off Cascade Tile 60:40 Horizon 75:25 Vertical Previous aran	tal			Default
L		ОК	Cance	

Figure 24: Other View Options

Fonts for the Tree Views and the Watch List can be adjusted here. Note that only the font is adjustable, style changes such as **bold**, *italic*, or <u>underline</u> are ignored.

Auto-Arrange Windows: This enables preferred window arrangement upon window opening. See Section 4.12 for more details.

4.12 Window Settings

From the Window menu, there are four main ways to arrange windows automatically.

4.12.1 Cascade

Windows are set to the same size and placed diagonally, overlapping each other. This is done without regard to the window type.

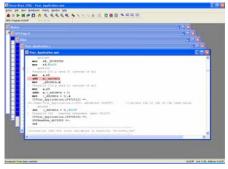


Figure 25: Cascade Arrangement



4.12.2 Tile

Windows are set to the same size and placed vertically next to each other. This is done without regard to the window type. See Figure 19 for an example.

4.12.3 60:40 Horizontal

Code views are tiled vertically in the left 60% of the application window, and the other views are tiled vertically in the right 40% of the application window. See Figure 15 for an example.

4.12.4 75:25 Vertical

E Code views are tiled in the top 75% of the application window, arranged vertically, and the other views are placed in the bottom 25% of the application window, arranged horizontally.

	JIAG - YOU	ır_Applio	cation.a	sm										_ 7
	v <u>B</u> reakpoint		_											
🗎 📕 🕨 🕅	i 🜈 🎧 🔞	<u>)</u> Q, 4	Q & (Q 🔍	% \	s == 34 🐽 😋	C 🗿 🗄) 🔁 🖂						
0: Program 0x02	24F B	P1 not set												
Your_Appli	ication.asm]												
; genCi														
mov r	2,_SPIRX	TXO												
	3,#0x00													8
; genP.	'lus .e 236.g 1	ugod ra	inata	and of	052									
	.e 230.g 1 ,r2	useu rz	. inste	au or	ar 2									
	, adcdata	a												
	adcdata,													
	e 236.g 1	used r3	3 inste	ead of	ar3									
	ι ,r3 ι,(adcdat	to + 11												
	adcdata													
					_									
Your_Appli	ication.c													
*/														1
														Ŀ
//Rea	id SPI dat													
//Read	ta= (SPI)	RXTX1 <	<< 8);											ļ
//Rea adcdat adcdat		RXTX1 < RXTXO;	• •	/isolat	te th	e 12 lab of t	he read v	alue						
//Read adcdai adcdai adcdai	uta= (SPI) uta+= SPI) uta&= OxO)	RXTX1 < RXTXO; FFF;	- 11	'isolat	te th	e 12 lsb of t	he read v	alue						Į
//Read adcdai adcdai adcdai	ta= (SPI) ta+= SPI)	RXTX1 < RXTXO; FFF;	- 11	'isolat	e th	e 12 lsb of t	he read v	alue						
//Read adcdat adcdat adcdat	uta= (SPI) uta+= SPI) uta&= OxO)	RXTX1 < RXTXO; FFF;	- 11	'isolat	te th	e 12 lsb of t	he read v	alue						ļ
//Read adcdat adcdat adcdat	uta= (SPI) uta+= SPI) uta&= OxO)	RXTX1 < RXTXO; FFF;	- 11	'isolat	e th	e 12 lsb of t	he read v	alue						l e
//Read adcdat adcdat adcdat)//end	uta= (SPI) uta+= SPI) uta&= OxO)	RXTX1 < RXTXO; FFF;	- 11		te th	e 12 lsb of t	be read v	alue						į
//Reau adcda adcda adcda	uta= (SPI) uta+= SPI) uta&= OxO)	RXTX1 < RXTXO; FFF;	// bc				the read v	alue						2
//Reau adcda adcda adcda	uta= (SPI) uta+= SPI) uta&= OxO)	RXTX1 < RXTXO; FFF;	// bc			e 12 lab of t	the read v			R Watch				
//Rear adcdar adcdar adcdar)//end	tta= (SPI) tta+= SPI) tta&= OXO) nd of Read	RXTX1 < RXTXO; FFF; dGen_AI	// oc			R SFR Page 0	Bin	Dec	Hex	R Watch			Address	Value
//Rea adcda adcda adcda }//en]]]]]]]]]]]]]]]]]]]	ita= (SPI) ita+= SPII itas= 0x01 id of Read	RXTX1 < RXTXO; FFF; dGen_AI dGen_AI 0SFF	// DC 3 0x00		X	R SFR Page 0	Bin 1111 1111	Dec -1	Hex 0xFF	 Name +>	IRA	M	0x48	Value Q'
//Rear adcdar adcdar adcdar)//end	ita= (SPI) ita+= SPII itas= 0x01 id of Read	RXTX1 < RXTXO; FFF; dGen_AI	// oc	- 0	X	R SFR Page 0	Bin	Dec -1 28	Hex	 Name +> +>	IRA IRA	M M	0x48 0x49	Value 'Q'
//Rea adcda adcda adcda)//en)//en)) () () () () () () () () (tta= (SPI) tta+= SPI tta&= 0x01 d of Read fF 0x00 B 0x02	RXTX1 < RXTXO; FFF; dGen_AI dGen_AI 0SFF	// DC 3 0x00		X	R SFR Page 0	Bin 1111 1111	Dec -1	Hex 0xFF	 Name +>	IRA	M M M	0x48	Value Q' Y' 'S'
//Rea adcda adcda adcda)//en)//en)) () () () () () () () () (tta= (SPI) tta+= SPI tta&= 0x01 d of Read fF 0x00 B 0x02 0 0x00	RXTX1 < RXTXO; FFF; dGen_AI 0Gen_AI 0xFF 0x10	// DC 3 0x00 0x3D			R SFR Page 0 Name P0 SP	Bin 1111 1111 0001 1100	Dec -1 28	Hex 0xFF 0x1C	 Name +> +> +> +> +>	IBA IBA IBA IBA IBA	M M M M M	0x48 0x49 0x4A 0x4B 0x4B 0x4C	Value 'Q' 'F' 'C'
//Rea adcda adcda adcda }//en }//en i i i i i i i i i i i i i i i i i i i	tta= (SPI) tta+= SPI tta&= 0x01 d of Read fF 0x00 B 0x02 0 0x00	RXTX1 < RXTX0; FFF; dGen_AI 0%FF 0%10 0%00	3 0x00 0x3D 0x00	4 0x00 0x00 0x00	X	R SFR Page 0 Name P0 SP DPL0	Bin 1111 1111 0001 1100 1111 1011	Dec -1 28 -5	Hex 0xFF 0x1C 0xFB	 Name +> +> +> +>	IRA IRA IRA IRA	M M M M M	0x48 0x49 0x4A 0x4B	Value Q' Q' B' 'c'

Figure 26: 75:25 Vertical Arrangement



5 Watch List

The Watch List provides a quick way to view all relevant memory locations. Watch variables, "watches", can be customized to show the most relevant information. The commands to operate watches are:

Action Edit View Breakpoint Watch Window Help			- 6
■►Ⅲ ♥ ☑ <			
: Program 0x024F BP1 not set		100-004	60.0800 M
me	Memory	Address	Value
unsigned int adodata	IBAM	0x08	0
+>	IBAM	0x09	127
char fircoefh[]	IRAM	0x30	Т
+>	IRAM	0x31	Т
+>	IRAM	0x32	Т
+>	IRAM	0x33	'l'
+>	IBAM	0x34	'I'
+>	IBAM	0x35	'I'
+>	IRAM	0x36	Т
+>	IBAM	0x37	Т
⊷ >	IRAM	0x38	Ť
+>	IRAM	0x39	Ϋ́.
+->	IRAM	0x3A	Ť.
+>	IRAM	0x3B	Ŷ
+->	IBAM	0x3C	Ť
+->	IBAM	0x3D	Ϋ́
+->	IBAM	0x3E	Ϋ́
+>	IBAM	0x3E	
char fircoef[[]	IBAM	0x40	,T
+->	IBAM	0x40 0x41	Ī
+>	IBAM	0x41 0x42	
	IRAM	0x42 0x43	Ĵ
+>			- 'c'
+>	IRAM	0x44	
+>	IRAM	0x45	'B'
+>	IRAM	0×46	'0'
+>	IBAM	0x47	'Q'
+>	IBAM	0x48	'Q'
+>	IRAM	0x49	'0'
+>	IBAM	0x4A	'B'
+>	IBAM	0x4B	'c'
+>	IRAM	0x4C	- 9
+>	IRAM	0x4D	Ϋ́
+>	IRAM	0x4E	î T
+>	IRAM	0x4F	'='
char datastackh[]	IRAM	0x50	
+>	IRAM	0x51	
+>	IRAM	0x52	•
+>	IRAM	0x53	1
+->	IBAM	0x54	12
+>	IBAM	0x55	5
+->	IBAM	0x56	
+>	IBAM	0x57	
+->	IBAM	0x58	10

Figure 27: Watch List (Window Maximized)

The Watch List is refreshed each time the processor stops, a new watch is added, and the G refresh command is issued. Refreshing will stop the processor.



5.1 Add Watch

his command brings up a dialog to add a watch to the list. New watches are added to the end of the list.

Add Watch 🛛 🛛 🔀	Add Watch 🛛 🔀
Name: PO 💌	Name: Example 🗸
Location: SFR Pg 0	Location: XRAM
Address: 80	Address: 633
Value Type: Hexadecimal 💌	Value Type: Binary
OK <u>C</u> ancel	OK Cancel

Figure 28: Adding a Watch

When adding a watch, there are four elements to consider:

- Name: This should reflect location. Names of SFR's cannot be edited; these names must be selected from the Name Combo box. XRAM and IRAM names can be any text.
- Location: The memory location. This can be IRAM, XRAM or either SFR page. See Section 4.5 for more details.
- Address: The address of the watch.
- Value Type: The way the value will be displayed can be any one of the following:
 - ASCII: The ASCII character associated to the value
 - **Bin:** The value of the SFR in binary
 - **Hex:** The value of the SFR in hexadecimal
 - **Decimal:** There are two ways to display values in decimal
 - Unsigned: Values of bytes are displayed between 0 and 255
 - Signed: Values of bytes are displayed between -128 and 127

Watches added manually are not saved between software sessions, but are saved between debugging sessions.

The name will be added to memory views, and that memory location will be refreshed.

5.2 Removing a Watch

This command will remove a watch from the list. If there is a breakpoint associated with the watch, it will not be disabled.



5.3 Editing an Existing Watch

Edit Watch				
Name:	Example	~		
Location:	XRAM	~		
Address:		633		
Value Type	e: Binary	~		
<u></u> K	<u> </u>	icel		
Figure 2	9: Editing a	Watch		

Ship this command permits a watch to be changed. Any of the parameters of adding a watch can be changed, including its address. If there is a breakpoint associated with the watch, it will not be disabled. The name will be changed in the memory views if the name was changed, and that memory location will be refreshed if the location was changed.

5.4 VForcing a Value

This command allows a value to be changed. This value must be in the same format as the watch. If <Force> is clicked, the display will be refreshed. The displayed value is always guaranteed to be directly from the processor. For more information on display types, see Section 5.1.

Force	
Example = (Binary)	11010110
Eorce	<u>C</u> ancel

Figure 30: Forcing a Value



Warning:

- Changing content directly may have unintended consequences over program flow or peripheral operation.
- Some SFR addresses are partially or completely read-only and cannot be overwritten. No error message occurs if a read-only register is written to and no damage is done to the device.
- Certain peripherals must be enabled before their associated SFR can be changed.
- If the processor is stopped within a program segment that is executing from XRAM the debugger will not display correct XRAM values. This is due to the hardware disabling external memory. For more information on how code can be run from external RAM, please consult the device datasheet.
- Do not edit XRAM values if the processor is stopped within a program segment that is executing from the XRAM. For more information on how code can be run from external RAM, please consult the device datasheet.



6 Breakpoints

The debugger allows for six different breakpoints. By default, they are not enabled. Changing any breakpoint setting will halt the processor. Breakpoints can be set for the following conditions:

- Address in code space (the line of code being executed)
- Address of a memory location
- Value of a memory location

6.1 Setting and Removing Breakpoints from an Address Tree or Source View

Setting a breakpoint from an address tree or a source view is simple. Select the line that will become a breakpoint and choose "Toggle breakpoint x" from the Breakpoint menu or from the Context menu (right click). To disable a breakpoint, select Toggle again or set the same breakpoint elsewhere.

If the option is enabled, double clicking a line of code will toggle Breakpoint 0.

Address Trees will display a numbered arrow **D** next to where the breakpoint is set. Code views will highlight the line in yellow.

6.2 Setting and Removing Breakpoints from a Memory View

Setting a breakpoint from a memory view is also simple. Select the line that will become a breakpoint and choose "Toggle breakpoint x" from the Breakpoint menu or from the Context menu (right click). The relevant cell(s) will turn yellow. To disable a breakpoint, select Toggle again or set the same breakpoint elsewhere.

6.3 Setting and Removing Breakpoints from the Watch List

6.3.1 Standard Breakpoints

To set a breakpoint from a watch list, select the line that will become a breakpoint, and choose "Toggle breakpoint x" from the Breakpoint menu or from the Context menu (right click). The line will be marked with a numbered arrow. **D**. To disable a breakpoint, select Toggle again or set the same breakpoint elsewhere.

6.3.2 Value Breakpoints

We To set a value breakpoint in the watch list, select the line that will become a breakpoint, and choose "Break on value" from the Watch menu or from the Context menu (right click). The following dialog will appear:

Break on Value	
Break when P0 = (Hexadecimal)	35
<u>S</u> et	Cancel

Figure 31: Setting a Value Breakpoint from a Watch List

Enter the value at which to break in the format specified (the same format as the entry in the Watch List). When $\langle Set \rangle$ is clicked, a flag P will appear next to the entry.



6.4 Setting and Removing Breakpoints from the Breakpoint Settings Dialog

🖑 To view and adjust all the breakpoint settings at once, open the Breakpoint Settings dialog.

Breakpoint Settings	Breakpoint Settings
Breakpoint Settings Standard Value Breakpoint 0 0000 Program Skip: Breakpoint 1 0000 Program 0 🗘 Breakpoint 2 0000 Program All addresses in hexadecimal Breakpoint 3 0000 Program Intervalue	Breakpoint Settings Standard Value Value 1 When 0x 00 When 0x 00 Value 2 When 0x 00 When 0x 00 When 0x 00 Image: When 0x 00 When 0x 00 Image: When 0x 00
Breakpoint 5 0000 Program V Apply	

Figure 32: Breakpoint Settings Window

6.4.1 Standard Breakpoints

Breakpoint information is presented from left to right. To set a breakpoint, mark the checkbox. The address refers to the location of the breakpoint and the Combo box selects the memory space. Click <Apply> to accept the changes and apply all of them simultaneously. Changes to breakpoints only occur after the <Apply> button is clicked. All entries are in hexadecimal.

Click <Undo> to revert to the last applied settings. <Undo> does not disable breakpoints.

6.4.2 Value Breakpoints

Breakpoint information is presented from left to right. To set a breakpoint, select the checkbox. The address refers to the location of the breakpoint and the Combo box selects the memory space. Click <Apply> to accept the changes and apply all of them at once. Changes to breakpoints only occur after the <Apply> button is clicked. All entries are in hexadecimal.

To set a breakpoint, complete the settings in the Value tab of the Breakpoint Settings window (see above). For example, "When 0x123 in XRAM equals 0x45" will stop the processor when 0x45 is written to address 0x123 in XRAM.

Click <Undo> to revert to the last applied settings. <Undo> does not disable breakpoints.

6.4.3 Setting a Skip Count

Breakpoint 0 and Value Breakpoint 1 can be configured to stop the processor after a specific number of times. This is most useful for breakpoints set within a loop in code space, but it can be applied for any breakpoint type. Select a number between 0 and 254 in the Edit box and click <Apply> to set the skip counter.

Setting the skip counter will halt execution of the program in the target device, if it is running. Setting the skip counter to 0 will stop the processor each time the established condition is met.



6.5 Mutually Exclusive Breakpoints

Value breakpoints take the space of two standard breakpoints. Table 7 shows the relationship between standard and value breakpoints. When Value Breakpoint 1 is set, Breakpoint 0 and Breakpoint 1 will be disabled, and be unable to be set.

Standard	Value
0	1
1	
2	2
3	2
4	3
5	5

Table 7: Mutually Exclusive Breakpoints

When setting Breakpoint 0 or Breakpoint 1, Value Breakpoint 1 will be disabled, and be unable to be set. Figure 33 shows an example of this behavior.

Breakpoint Settings				Breakpoint Settings
Standard Value				Standard Value
Breakpoint 0	003B	Program 🔽	Skip:	
🔲 Breakpoint 1	0000	Program 💌	0 🗘	When 0x 00 in IRAM v is equal to 0x 00
Breakpoint 2	0000	Program 🗸		Value 2 When 0x 123 in XRAM v is equal to 0x 00
Breakpoint 3	0000	Program 💉	All addresses in hexadecimal	Value 3
Breakpoint 4	0000	Program 🔽	Undo	When 0x 00 in IRAM v is equal to 0x 00
Breakpoint 5	0000	Program 💌		Undo Apply

Figure 33: Mutually Exclusive Breakpoints

When setting value breakpoints in the Watch List, placement is automatic. If a value breakpoint cannot be set, the following warning message will be displayed:

Versa Ware JTAG					
1	Unable to set a value breakpoint because there are too many breakpoints in use. Each value breakpoint takes 2 breakpoint slots. Please free up BPO and BP1, BP2 and BP3, or BP4 and BP5, or any other value breakpoint if set before setting another value breakpoint.				
	ОК				

Figure 34: Too Many Breakpoints

6.6 Breakpoint Information Toolbars

These toolbars, grouped in pairs, provide quick access to which breakpoints have been enabled and where they are set to trigger. They can be docked to the top or bottom of the application window, or they can float.

These bars display data in black when breakpoints are set and gray when breakpoints are disabled.

BPO: unsigned int dacdata	BP1: Program 0x00E0	BP2: DP5	BP3 not set			
Figure 25. Decalment Information Tablean						

Figure 35:	Breakpoint	Information	Toolbars
------------	------------	-------------	----------

Variable names are displayed in the place of raw addresses where possible. These names are retrieved from the Watch List. See Section 5 for more details.

6.7 When a Breakpoint is Reached

When a breakpoint in code space is reached, the program stops **before the instruction is executed** and displays a message indicating which breakpoint was triggered. For breakpoints in memory and for value breakpoints, the program stops **after the instruction is executed**. At this point, any other action can be performed (e.g. view SFR content).

n <u>E</u> dit <u>V</u> iew <u>B</u> reakpoint Watc <u>h W</u> indow <u>H</u> elp								
🔳 🕨 🖉 💭 🚷 🔍 🄍 🄍 🔍 🔍 🔍 🔍	💊 💊 = 24 🖑 🛟 🖸 🗃 🗄	6888	3					
: unsigned int dacdata BP1: Program 0x00E0	BP2: DPS BP3 not set							
Your_Application.ihx			RAM					
C [213] PWMCFG = 0x17;	//Point to MSB MID	^	Name	Address	Bin	Dec	Hex	ASCII
a 00DD mov _PWMCFG,#0x1	.7			0x2D	0000 0000	0	0x00	0
C [214] PWMDATA = 0xA2;	11			0x2E	0000 0000	0	0x00	0
DOEO nov _PUMDATA,#0x	A2			0x2F	0000 0000	0	0x00	0
C [215]			char fircoefh[]	0x30	0000 0010	2	0x02	0
C [216] PWMCFG = 0x07;	//Point to LSB MID		+>	0x31	0000 0100	4	0x04	0
a OOE3 mov _PWMCFG,#0x0	17		+>	0x32	0000 1000	8	0x08	0
C [217] PWMDATA = 0xC2;	-20		+>	0x33	0000 1101	13	0x0D	0
- a OOE6 mov _PWMDATA,#0x	(UZ		+>	0x34	0001 0010	18	0x12	П
C [218] C [219]								
	W as timer Interrupt to monito	r PWM5 o	R SFR Page 0					
	/PWM7:4 Timer module Interrupt		Name	Address	Bin	Dec	Hex	ASCII
	PWM(:4 Ilmer module interrupt							
	n an		PO	0x80	1111 1111	-1	0xFF	
00E9 anlINTSRC2,#0x	n an	~	SP	0x81	0000 0111	7	0x07	0
	n an	× > .::	SP DPL0	0x81 0x82	0000 0111 0000 0000	7 0	0x07 0x00	0
00E9 anl _INTSRC2,#0x	n an		SP	0x81	0000 0111 0000 0000 0000 0000	7 0 0	0x07	ÿ 0 0
□ 00E9 en1INT\$RC2,#0x	n an		SP DPL0	0x81 0x82	0000 0111 0000 0000	7 0 0	0x07 0x00	0
00E9 anlINTSRC2,#0x	n an		SP DPL0 DPH0	0x81 0x82 0x83	0000 0111 0000 0000 0000 0000	7 0 0	0x07 0x00 0x00	0
Your_Application.c	DF //PWM Timer 7 Prescaler =	Sys Cl	SP DPL0 DPH0 DPL1	0x81 0x82 0x83 0x83	0000 0111 0000 0000 0000 0000 0000 0000	7 0 0	0x07 0x00 0x00 0x00	000000000000000000000000000000000000000
Your_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (wi	DF //PWM Timer 7 Prescaler = 11 be monitored by interrupt	Sys Cl	SP DPL0 DPH0 DPL1 DPH1	0x81 0x82 0x83 0x83 0x84 0x85	0000 0111 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000	7 0 0 0	0x07 0x00 0x00 0x00 0x00	000000000000000000000000000000000000000
Your_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (wi // PWM Timer 7 counts from 0000	DF //PUM Timer 7 Prescaler = 11 be monitored by interrupt to A2C2h	Sys Cl	SP DPL0 DPH0 DPL1 DPH1 DPH1 DPS Pr3N	0x81 0x82 0x83 0x84 0x85 0x85 0x86	0000 0111 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000	7 0 0 0 0	0x00 0x00 0x00 0x00 0x00 0x00	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Your_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (wi	DF //PWM Timer 7 Prescaler = 11 be monitored by interrupt	Sys Cl	SP DPL0 DPH0 DPL1 DPH1 DPS PCNN	0x81 0x82 0x83 0x84 0x85 0x85 0x86	0000 0111 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0110 0000	7 0 0 0 0 0 96	0x07 0x00 0x00 0x00 0x00 0x00 0x00 0x60	
<pre>> 00E9 anl _INTSRC2,#0x Your_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (wi // PWM Timer 7 counts from 0000 PWMCFG = 0x17;</pre>	DF //PWM Timer 7 Prescaler = 11 be monitored by interrupt to &2C2h //Point to MSB MID //	Sys Cl	SP DPL0 DPH0 DPL1 DPH1 DPS PCNN R Watch Name	0x81 0x82 0x83 0x84 0x85 0x85 0x86	0000 0111 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0110 0000 Memory	7 0 0 0 0 96 8	0x07 0x00 0x00 0x00 0x00 0x00 0x00 0x00	
<pre>> 00E9 anl _INTSRC2,#0x //our_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (wi // PWM Timer 7 counts from 0000 PWMCFG = 0x17; PWMDATA = 0xA2; PWMCFG = 0x07;</pre>	DF //PWM Timer 7 Prescaler = 11 be monitored by interrupt to &2C2h //Point to MSB MID	Sys Cl	SP DPL0 DPH0 DPL1 DPH1 DPS PCNN	0x81 0x82 0x83 0x84 0x85 0x85 0x86	0000 0111 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0110 0000	7 0 0 0 0 96 96	0x07 0x00 0x00 0x00 0x00 0x00 0x00 0x60	I I I I I Value
Your_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (wi // PWM Timer 7 counts from 0000 PWMCFG = 0x17; PWMDATA = 0xA2;	DF //PWM Timer 7 Prescaler = 11 be monitored by interrupt to &2C2h //Point to MSB MID //	Sys Cl	SP DPL0 DPH0 DPL1 DPH1 DPS Pf:DN R Watch Name +-> +-> +->	0x81 0x82 0x83 0x84 0x85 0x85 0x86	0000 0111 0000 0000 0000 0000 0000 0000 0000 0000 0110 0000 0110 0000 III AM IRAM IRAM IRAM	7 0 0 0 0 96 0 8 0 0 0 0 0 0 0 0 0 0 0	0x07 0x00 0x00 0x00 0x00 0x00 0x00 0x00	U U U U U Value
<pre>> 00E9 anl _INTSRC2,#0x //our_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (wi // PWM Timer 7 counts from 0000 PWMCFG = 0x17; PWMDATA = 0xA2; PWMCFG = 0x07;</pre>	DF //PWM Timer 7 Prescaler = 11 be monitored by interrupt to &2C2h //Point to MSB MID //	Sys Cl	SP DPL0 DPH0 DPL1 DPH1 PCNN R Watch Name +→> +→> +→>	0x81 0x82 0x83 0x84 0x85 0x85 0x86	0000 0111 0000 0000 0000 0000 0000 0000 0000 0000 0110 0000 0110 0000 IRAM IRAM IRAM IRAM	7 0 0 0 96 96 0 0 0 0 0 0 0 0 0 0	0x07 0x00 0x00 0x00 0x00 0x00 0x00 0x00	U U U U U Value
<pre>> 00E9 anl _INTSRC2,#0x //our_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (wi // PWM Timer 7 counts from 0000 PWMCFG = 0x17; PWMDATA = 0xA2; PWMCFG = 0x07;</pre>	DF //PWM Timer 7 Prescaler = 11 be monitored by interrupt to &2C2h //Point to MSB MID // //Point to LSB MID	= Sys C]	SP DPL0 DPH0 DPL1 DPH1 DPS Pf:DN R Watch Name +-> +-> +->	0x81 0x82 0x83 0x84 0x85 0x85 0x86	0000 0111 0000 0000 0000 0000 0000 0000 0000 0000 0110 0000 0110 0000 III AM IRAM IRAM IRAM	7 0 0 0 0 0 96 0 8 0 8 0 8 0 8 0 8 0 8 0 8 0 8 0 8 0	0x07 0x00 0x00 0x00 0x00 0x00 0x00 0x00	U U U U U U U U U U U U
<pre>> 00E9 anl _INTSRC2,#0x Your_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (wi // PWM Timer 7 counts from 0000 PWMCFG = 0x17; PWMDATA = 0xA2; PWMCFG = 0x07; PWMDATA = 0xC2;</pre>	DF //PWM Timer 7 Prescaler = 11 be monitored by interrupt to A2C2h //Point to MSB MID // //Point to LSB MID timer Interrupt to monitor	= Sys C]	SP DPL0 DPH0 DPL1 DPM PCDN Reconstruction ***> ***> ***> ***> ***> ***> ***> ***> ***> ***> ***> ***> ***>	0x81 0x82 0x83 0x84 0x85 0x85 0x86	0000 0111 0000 0000 0000 0000 0000 0000 0000 0000 0110 0000 1110 0000 IRAM IRAM IRAM IRAM IRAM IRAM IRAM IRAM	7 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0x07 0x00 0x00 0x00 0x00 0x00 0x00 0x00	
<pre>> 00E9 anl _INTSRC2,#0x Your_Application.c PWMCLKCFG = 0x10; //Configure PWM7 as Timer (wi // PWM Timer 7 counts from 0000 PWMCFG = 0x17; PWMDATA = 0xA2; PWMCFG = 0x07; PWMCFG = 0x07; PWMDATA = 0xC2; //Configure and Enable PWM as</pre>	DF //PWM Timer 7 Prescaler = 11 be monitored by interrupt to &2C2h //Point to MSB MID // //Point to LSB MID timer Interrupt to monitor 4 Timer module Interrupt ve on high Level(0)	Sys C)	SP DPL0 DPH0 DPL1 DPH1 PS PCDN R Watch Name +-> +-> +-> +-> +->	0x81 0x82 0x83 0x84 0x85 0x86 0x86	0000 0111 0000 0000 0000 0000 0000 0000 0000 0000 0110 0000 0110 0000 1110 0000 1110 0000 1110 0000 1110 0000 1110 0000 1110 0000 1110 0000	7 0 0 0 0 0 0 96 0 0 0 0 0 0 0 0 0 0 0 0	0x07 0x00 0x00 0x00 0x00 0x00 0x00 0x00	0 0 0 0 0

Figure 36: A Breakpoint is Reached

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Once the desired operations are complete, choose either run (\blacktriangleright) to resume the program or step (\blacksquare) to advance one instruction at a time. See sections 4.4.1 and 4.4.2 for more details.

7 Command Line Options

Versa Ware JTAG is distributed with a command line tool called VWJTAG that can be used in scripts or as a companion to this software. For more information, please consult VWJTAG ReadMe. This HTML file is located in the same directory as VWJTAG, or in the Start menu under "Programs\Ramtron\Versa Ware JTAG".

8 Connection Problem Troubleshooting

8.1 Connection Error at Startup

Once Versa Ware JTAG is launched, it will try to synchronize with the target device. If the communication fails, the following error message will appear:



Figure 37: Unable to Connect to Device

Possible causes for this error are:

- The programming interface is not connected to the PC
- The programming interface is not powered
- The target device is not correctly inserted into the socket
- The development environment does not have automatic power control (see Section 3.8.3)
- Parallel port settings are incorrect (see Section 9)

Rectify the above condition(s) and use the Synchronize command.

8.2 Connection Error during Session

If the power is cut, the JTAG cable unplugged or if the PC goes into standby, hibernate or shutdown, a connection error will occur during debugging or programming. An error message will appear and the window will be closed. Reconnect and try again.

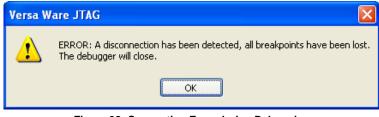


Figure 38: Connection Error during Debugging



8.3 Intermittent Connection Errors

If programming often fails or debugging sessions are frequently interrupted, check for the following situations:

8.3.1 Dongles



Software that requires a hardware key (dongle) can cause problems when concurrently run with Versa Ware JTAG. These programs tend to interrupt communication to the VersaKit development system, in search for hardware keys, even under the following circumstances:

- Program minimized
- USB dongle is installed
- Current license does not require a dongle but a different license package does

Do not connect the JTAG adaptor to a parallel port dongle, connect it directly to the port instead.

8.3.2 Too Many Applications Running

Applications that require a lot of system resources may cause connection problems.

9 Parallel Port Setup

Versa Ware JTAG software requires a dedicated PC parallel port. The port must either be built onto the motherboard, or an ISA card. **PCI cards or USB adapters are not supported.**

The port must be in ECP mode and use address 378h. These settings can be found in the system BIOS at boot-up for ports built onto the motherboard.

The Versa-JTAG must be connected to LPT1. Make sure all other devices have been uninstalled from both the JTAG and LPT1. Interrupts must be disabled. To do this, go to the Device Manager in System Properties, and click "ECP Printer Port (LPT1)". (ECP might not be listed, ensure the correct setting in the BIOS).



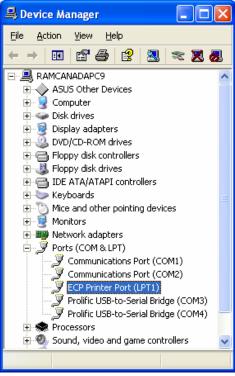


Figure 39: Device Manager Window

Right-click the port and then select "Properties" to bring up the settings window for LPT1, and then navigate to the tab. Ensure that "Never use an interrupt" is selected in the Filter resource box.

ECP Printer Port (LPT1) Properties						
General Port Settings Driver Details Resources						
Filter Resource Method						
◯ <u>I</u> ry not to use an interrupt						
⊙ Never use an interrupt						
◯ <u>U</u> se any interrupt assigned to the port						
✓ Enable legacy Plug and Play detection						
LPT Port Number:						
OK Cancel						

Figure 40: Required Port Settings to Use with Versa Ware JTAG



On the Resources tab, ensure that LPT1 uses ranges 0378h to 037Fh, as well as range 0778h to 077Bh. If these values do not appear in the window, try correcting them in the BIOS (for motherboard parallel ports), or the port's driver configuration page (for ISA parallel ports).

If the values still do not match, uncheck "Use automatic settings" and set the configuration manually. Multiple attempts may be necessary.

ECP Printer Port	(LPT1) Properties	? 🔀					
General Port Setti	ngs Driver Details Resources						
ECP Prin	ter Port (LPT1)						
Resource settings:							
Resource type	Setting						
	0778 - 077B						
DMA	03						
Setting <u>b</u> ased on:	Current configuration	~					
	✓ Use automatic settings	Change Setting					
Conflicting device list:							
No conflicts.		X					
		JK Cancel					

Figure 41: Resources Used for LPT1

Restart Windows once the LPT1 settings are set.

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