SEALEVEL
SYSTEMS INCORPORATED

ACB-V™
PART # 4012
USER MANUAL

SECTIONS:

FIGURES:

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SECTION 1.

Installation

The ***ACB-V*** can be installed in any of the PC expansion slots. Remove the PC case, remove the blank metal slot cover, and insert the board. Replace the screw, replace the cover, and the installation is complete.

Be sure to set the address and jumper options before installation.

SECTION 2.

Address Selection

The ***ACB-V*** occupies 8 consecutive I/O locations. A dip-switch (SW1) is used to set the base address for these locations. Be careful when selecting the base address as some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

Address	Binary	Switch Settings						
	A9----------A0	1	2	3	4	5	6	7
238-23F	1000111XXX	Off	On	On	On	Off	Off	Off
280-287	1010000XXX	Off	On	Off	On	On	On	On
2A0-2A7	1010100XXX	Off	On	Off	On	Off	On	On
2E8-2EF	1011101XXX	Off	On	Off	Off	Off	On	Off
300-307	1100000XXX	Off	Off	On	On	On	On	On
328-32F	1100101XXX	Off	Off	On	On	Off	On	Off
3E8-3EF	1111101XXX	Off	Off	Off	Off	Off	On	Off

Typically COM1:=3F8H; COM2:=2F8H; COM3:=3E8H; COM4:=2E8H.

Figure 1

The following illustration shows the correlation between the dip-switch setting and the address bits used to determine the base address. In the example below, the address 300 Hex through 307 Hex is selected. 300 Hex =11 0000 0XXX in binary representation.

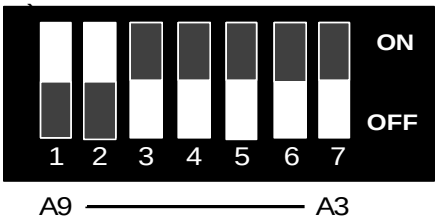


Figure 2

Note that setting the switch "On" or "Closed" corresponds to a "0" in the address, while leaving it "Off" or "Open" corresponds to a "1".

The relative I/O address of the 8530 SCC registers is as follows:

- Base+0 Channel A Data Port
- Base+1 Channel A Control Port
- Base+2 Channel B Data Port
- Base+3 Channel B Control Port
- Base+4 Board Control / Status Port

Where "Base" is the selected board base address.

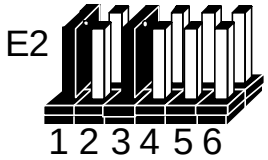
SECTION 3.

Option Selection

The ***ACB-V*** contains several jumper straps which must be set for proper operation.

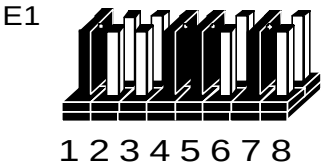
E2- This header selects DMA mode of operation. Channel A of the SCC can operate in either half-duplex or full duplex DMA mode. Full duplex DMA can transmit and receive data simultaneously. Half-duplex DMA can transmit or receive data, but not in both directions simultaneously. Both channels A and B can be used in half-duplex mode. The various options for E1 and E2 jumper settings are as follows:

NOTE: If DMA is not used, remove all of the jumpers on E1 and E2. Refer to Page 3 for the most common DMA settings.



1	DACK 1 Or 3 Acknowledge For Two Channel Mode
2	Two Channel A/B Mode A3B1
3	Two Channel A/B Mode A1B3
4	On = Ch. A Only / Off = Ch. B Only
5	DACK 3 DMA Acknowledge Channel 3
6	DACK 1 DMA Acknowledge Channel 1

Figure 3
Header E2 DMA Mode Options



1	A or B Ch 3
2	A only Ch 3
3	A or B Ch 1
4	A only Ch 1
5	B Enable
6	A Full Duplex
7	DMA Always Enabled
8	Control Port Bit 7 Enables DMA (See Below)

Figure 4
Header E1 DMA Mode Options

E1: Positions 7 and 8 enable or disable DMA operation. A jumper "ON" position 7 permanently enables the DMA tri-state drivers. A jumper "ON" position 8 places DMA under software control via the DMA enable control port bit (located at Base+4). Removing the jumper disables the drivers, and no DMA can be performed.

NOTE : The power on reset signal disables the DMA enable signal. A jumper placed in position 7 of E1 will override any software uses of the DMA enable / disable status port bit.

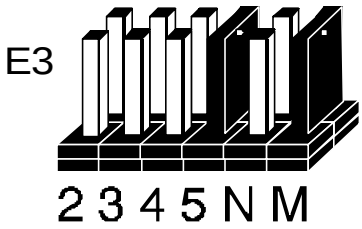
Commonly Used DMA Jumper Options

Option	E2	E1	Program 8530
No DMA Channel A or B.	None	None	N/A
Single Channel DMA (Half Duplex Only):			
Ch.A DMA Ch.1 Half Duplex Ch.B No DMA.	4,6	4	WAIT/REQ A
Ch.A DMA Ch.3 Half Duplex Ch.B No DMA.	4,5	2	WAIT/REQ A
Ch.B DMA Ch.1 Half Duplex Ch.A No DMA.	6 Only	3,5	WAIT/REQ B
Ch.B DMA Ch.3 Half Duplex Ch.A No DMA	5 Only	1,5	WAIT/REQ B
Both DMA Channels (1 and 3) Selected:			
Ch.A DMA Ch.1 Half Duplex Ch.B DMA Ch.3 Half Duplex	1,3	1,4,5	WAIT/REQ A WAIT/REQ B
Ch.A DMA Ch.3 Half Duplex Ch.B DMA Ch.1 Half Duplex	1,2	2,3,5	WAIT/REQ A WAIT/REQ B
Full Duplex Channel A with Both DMA Channels 1 and 3:			
Ch.A DMA Ch.1 Receive Data Ch.A DMA Ch.3 Transmit Data	1,4	1,4,6	WAIT/REQ A DTR/REQ A
Ch.A DMA Ch.3 Receive Data Ch.A DMA Ch.1 Transmit Data	1,4	2,3,6	WAIT/REQ A DTR/REQ A

Note: ***Channel B of the ACB-V does not support full duplex DMA.***

Figure 5

E3: This header selects the interrupt request line for the port. The diagram below shows IRQ 5 selected in a shared configuration. If no interrupt is desired, remove the jumper.



2	Selects IRQ2
3	Selects IRQ3
4	Selects IRQ4
5	Selects IRQ5
N	Selects Normal (1 IRQ Per Board) IRQ Mode
M	Selects "Multi-IRQ" (Shared) IRQ Mode

Figure 6

The factory default setting for E3 is: "5" and "M".

EPROM Usage

The EPROM socket on the ***ACB-V*** is provided for convenience only and does not affect the communication functions of the board in any way. If the EPROM is not used, the socket should be disabled (dip-switch SW2 position 5 off). The following table shows several EPROM base address examples.

The EPROM is a 27128 device occupying 16K bytes of memory at or above C800 Hex to be recognized by the PC on boot up. Address lines A19, and A18 are always a binary 1, forcing a selection of C000 Hex or greater.

Address	Address Lines				Switch position setting (SW1)			
	A17	A16	A15	A14	1	2	3	4
C000-C3FF	0	0	0	0	On	On	On	On
C400-C7FF	0	0	0	1	On	On	On	Off
C800-C9FF	0	0	1	0	On	On	Off	On
D000-D3FF	0	1	0	0	On	Off	On	On
D400-D7FF	0	1	0	1	On	Off	On	Off
D800-DBFF	0	1	1	0	On	Off	Off	On
E000-E3FF	1	0	0	0	Off	On	On	On
E400-E7FF	1	0	0	1	Off	On	On	Off

Figure 7
EPROM Address Examples

Note: Some "AT" class machines cannot use address E000 and above.

Figure 8 illustrates the correlation between the dip-switch setting and the address bits used to determine the base address.

Switch position 5 enables and disables the EPROM socket. The default setting is with the EPROM socket disabled. The ***ACB-V*** will be shipped with the dip-switch in the configuration illustrated in Figure 8.

Figure 8
Dip-Switch Illustration (SW2)

SECTION 4.

Technical Description

Advanced Communications Board IV Specifications

The Sealevel ***ACB-V*** advanced communications board provides the PC with two high speed sync/async ports. The ***ACB-V*** can be used in a variety of sophisticated communication applications such as SDLC, HDLC, X.25, and high speed async. Features included on the card are:

- Two channels of sync / async communications using 8530 chip
- DMA supports data rate greater than 1 million bps (bits per second)
- Selectable Port Address, IRQ level (2,3,4,5), and DMA channel (1 or 3)
- CCITT V.35 interface with full modem control supports TD, RD, RTS, CTS, DSR, DCD, DTR, TXC, RXC signals
- Jumper options for clock source
- Software programmable baud rate
- High Speed Enhanced Serial Communications Controller (85C30,85230) compatible

The ***ACB-V*** utilizes the ZILOG 8530 Serial Communications Controller (SCC). This chip features programmable baud rate, data format and interrupt control, as well as DMA control. Refer to the 8530 technical manual, the ZILOG SCC users manual, and the ACB Developers Toolkit Diskette for details on programming the SCC.

CCITT V.35

The Comite Consultatif Internationale de Telegraphie et Telephonie also known as the CCITT is the agency that set the V.35 standard. V.35 specifies an electrical, mechanical, and physical interface that is used extensively by high-speed digital carriers such as AT&T Dataphone Digital Service (DDS). CCITT V.35 is an international standard that is often referred to as "Data Transmission at 48 Kbps Using 60 - 108 KHz Group-Band Circuits." CCITT V.35 electrical characteristics are a combination of unbalanced voltage and balanced current mode signals. Data and clock signals are balanced current mode circuits. These circuits typically have voltage levels from 0.5 Volts to -0.5 Volts (1 Volt differential). The modem control signals are unbalanced signals and are compatible with RS-232. The physical connector is a 34 pin connector that supports 24 data, clock and control signals. The physical connector is defined in the ISO-2593 standard. CCITT V.35 is implemented with both DTE and DCE interfaces, the ***ACB-V*** is implemented using the DTE interface. The ***ACB-V*** will not generate a clock signal without a modification. because the CCITT V.35 specification does not specify a clock output signal for a V.35 DTE. If an output clock signal is required for the V.35 interface, please call Sealevel Systems Technical Support . The ***ACB-V*** is compatible with CCITT V.36 and V.37.

SECTION 5.

Programming the ACB-V

Control/Status Port

The ***ACB-V*** occupies eight **I**nput/**O**utput (I/O) addresses. The first four are used by the SCC chip, while the fifth address (Base+4) is the address of the on-board ***Control/Status Port.*** This port is used to set the **D**ata **T**erminal **R**eady (DTR) signal, to enable or disable DMA under software control, and to monitor the **D**ata **S**et **R**eady (DSR) input signals from the modem. The following table lists bit positions of the Control/ Status port.

Bit:	Output Port Bits		Input Port Bits	
0	DTR A	1=On, 0=Off	DSR A	1=On, 0=Off
1	DTR B	1=On, 0=Off	DSR B	1=On, 0=Off
2	Not Used		Not Used	1=On, 0=Off
3	Not Used		Not Used	1=On, 0=Off
4	Not Used		Not Used	1=On, 0=Off
5	Not Used		Not Used	1=On, 0=Off
6	Not Used		Not Used	1=On, 0=Off
7	DMA Enable	1=On, 0=Off	Not Used	1=On, 0=Off

Figure 11

Software Examples

Function	Program Bits
Turn On CH.A DTR	Write Out Base+4,XXXX XXX1
Turn On CH.B DTR	Write Out Base+4,XXXX XX1X
Turn Off CH.A DTR	Write Out Base+4,XXXX XXX0
Turn Off CH.B DTR	Write Out Base+4,XXXX XX0X
Enable DMA Drivers	Write Out Base+4,1XXX XXXX
Disable DMA Drivers	Write Out Base+4,0XXX XXXX
Test CH.A DSR	Read In Base+4, Mask=0000 0001
Test CH.B DSR	Read In Base+4, Mask=0000 0010

Figure 12

NOTE: Assembly language programs should not do two successive I/O accesses, which violates the 8530 SCC recovery time specification. Please refer to the 8530 technical reference for more details.

Correct:

```
MOV DX,3E0H
OUT DX,AL
JMP $+2
OUT DX,AL
```

Incorrect:

```
MOV DX,3E0H
OUT DX,AL
OUT DX,AL
```

Direct Memory Access

Direct **M**emory **A**ccess (DMA) can be used to transfer data at very high rates. DMA allows the ***ACB-V*** to transfer data directly to or from system memory bypassing the CPU. The software examples provided on the ACB Developer Toolkit diskette demonstrate the setup and use of DMA.

Internal Baud Rate Generator

The baud rate of the SCC is programmed under software control. The standard oscillator supplied with the board is 4.9152 MHz. However, other oscillator values can be substituted to achieve different baud rates.

P1 and P2 Connector

The connector on the ***ACB-V*** is a DB-15. This connector is matched with a V.35 cable to provide the proper mechanical connection as required by the ISO-2593 standard.

Note: The connector for the SCC Channel A is labeled as P2 and is the bottom connector when the card is installed in a socket. The connector for SCC Channel B is labeled P1 and is the top connector when the card is installed in a socket.

Signal		Name	DB-15 Pin #	V.35 Pin #	Mode
GND		Ground	8	B	
TDB	TX+	Transmit Data Positive	2	S	Output V.35
TDA	TX-	Transmit Data Negative	9	P	Output V.35
RDB	RX+	Receive Data Positive	4	T	Input V.35
RDA	RX-	Receive Data Negative	11	R	Input V.35
TXCB	TXC+	Transmit Clock	12	AA	Input V.35
TXCA	TXC-	Transmit Clock	10	Y	Input V.35
RXCB	RXC+	Receive Clock	13	X	Input V.35
RXCA	RXC-	Receive Clock	14	V	Input V.35
CTS	CTS	Clear To Send	5	D	Input RS-232
DSR	DSR	Data Set Ready	6	E	Input RS-232
DCD	DCD	Data Carrier Detect	7	F	Input RS-232
RTS	RTS	Request To Send	3	C	Output RS-232
DTR	DTR	Data Terminal Ready	15	H	Output RS-232

ACB Developer Toolkit Diskette and the ACB Resource Kit for DOS

The ACB Developer Toolkit software provides sample software for DOS and technical insight to aid in the development of reliable applications and device drivers for the ACB family of communication cards. The goal in publishing this collection of source code and technical information is two fold. First is to provide the developer with ample information to develop ACB based applications. Second is to provide a channel for suggestions into the technical support efforts. The ACB Resource Kit provides a brief overview of the ACB product line. Topics concerning applications and integration are covered to provide a complete overview of the versatile ACB family. During ACB development, any questions, comments, suggestions, or to receive the ACB Resource Kit, please contact Technical Support at the numbers listed at the end of this manual.

Software Installation

Windows Users

Choose **Install Software** at the beginning of the CD and select **Synchronous/Asynchronous Software** and install the **SeaMAC** software.

SECTION 6.

Specifications

Environmental Specifications

Specification	Operating	Storage
Temperature range	0 - 50 Degrees C 32 - 122 Degrees F	-20 - 70 Degrees C -40 - 100 Degrees F
Humidity Range	0- 90% R.H. Non-Condensing	0- 90% R.H. Non-Condensing

Performance Specifications

MTBF > 150,000 Hours
MTTR < .25 Hours
Turnaround for repair - 5 working days

Manufacturing Specifications

- Adherence to IPC 610-A Class-III standards with a 0.1 visual A.Q.L. and 100% functional testing.
- Boards are built to U.L. 94V0 rating and are 100% electrically tested. Most boards are solder mask over bare copper.

Power Specifications

Supply Line	+5	-5	±12
Rating (mA)	450 mA	75 mA	50 mA

SECTION 7.

Warranty

Sealevel Systems, Inc. provides a lifetime warranty for this product. Should this product fail to be in good working order at any time during this period, Sealevel Systems will, at it's option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Sealevel Systems assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Sealevel Systems will not be liable for any claim made by any other related party.

Return authorization must be obtained from Sealevel Systems before returned merchandise will be accepted. Authorization can be obtained by calling Sealevel Systems and requesting a Return Merchandise Authorization (RMA) Number.

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