SEALEVEL
SYSTEMS INCORPORATED

ACB-VI
USER MANUAL
PART # 4015

SECTIONS:

FIGURES:

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SECTION 1.

INSTALLATION

The ACB-VI can be installed in any of the "PC", "XT", or "AT" expansion slots, except J8 on the original IBM "XT" and Portable. Be sure to set the address and jumper options before installation. To install, remove the PC case, remove the blank metal slot cover, and insert the board. Replace the screw, replace the case, and installation is complete.

SECTION 2.

ADDRESS SELECTION

The ACB-VI board occupies 8 consecutive I/O locations. A dip switch (SW1) is used to set the base address for these locations. Be careful when selecting the base address as some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

ADDRESS	BINARY REP	SWITCH POSITION SETTING:						
	A9--------A0	1	2	3	4	5	6	7
238-23F	1000110XXX	OFF	ON	ON	ON	OFF	OFF	OFF
2A0-2A8	1010100XXX	OFF	ON	OFF	ON	OFF	ON	ON
2E8-2EF	1011101XXX	OFF	ON	OFF	OFF	OFF	ON	OFF
2F8-2FF	1011111XXX	OFF	ON	OFF	OFF	OFF	OFF	OFF
300-308	1100000XXX	OFF	OFF	ON	ON	ON	ON	ON
328-32F	1100101XXX	OFF	OFF	ON	ON	OFF	ON	OFF
3E8-3EF	1111101XXX	OFF	OFF	OFF	OFF	OFF	ON	OFF

TYPICALLY COM1: = 3F8h; COM2: = 2F8h; COM3: = 3E8h; COM4: = 2E8h.

Figure 1
Address Selection Table

The following illustration shows the correlation between the dip switch setting and the address bits used to determine the base address. In the example below, the address 300 Hex through 307 Hex is selected. 300 Hex =11 0000 0XXX in binary representation.

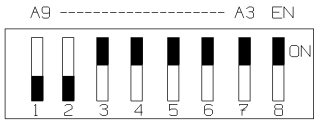

Figure 2
Dip Switch Illustration

Note that setting the switch "On" or "Closed" corresponds to a "0" in the address, while leaving it "Off" or "Open" corresponds to a "1".

PORT ENABLE / DISABLE

The ACB VI can be enabled or disabled with switch position 8 on the dip switch. The port is enabled with the switch "On" or "Closed" and disabled when "Off" or "Open".

I/O ADDRESSES

The relative I/O address of the 8530 SCC registers are as follows:

- Base+0 Channel A Data Port
- Base+1 Channel A Control Port
- Base+2 Channel B Data Port
- Base+3 Channel B Control Port
- Base+4,5,6 Board Control / Status Registers

Where "Base" is the selected board base address.

SECTION 3.

TECHNICAL DESCRIPTION

The ACB-VI **A**dvanced **C**ommunications **B**oard provides the PC/XT/AT with one high speed sync/async port and one RS-232 port suitable for use as a CSU command port.

Features Include:

- One channel of synchronous / asychronous communications using 8530 **S**erial **C**ommunications **C**ontroller (SCC) channel A
- SCC channel B asynchronous port for CSU/DSU Command Port
- Selectable Port Address and IRQ level (2-5,7,10-12,15)
- Selectable DMA Channels (0,1,2,3)
- Selectable RS-232, CCITT V.35, RS-422 / RS-485 / 530, MIL 188-C AND MIL 188-114 for Channel A of the SCC on a DB-25P
- Channel A interface supports TD, RD, RTS, CTS, DSR, DCD, TXC, RXC, DTR, RI, and TSET signals on all interfaces and includes SQD on the RS-232 interface.
- RS-232C Interface for Channel B of the SCC supports TD, RD, RTS, CTS, DSR, DCD, DTR, RI, signals on a DB-9P Male Connector

The board occupies eight Input/Output (I/O) addresses. The first four are used by the SCC , while the fifth, sixth, and seventh addresses (Base+4, Base+5, And Base+6) are the addresses of the on-board Control / Status registers. The address at Base+7 is not used. The ports at Base + 4, 5, and 6 are used to set the **D**ata **T**erminal **R**eady (DTR) signals "On" or "Off", to enable or disable DMA and Interrupts under program control, and to monitor the **D**ata **S**et **R**eady (DSR), **D**ata **C**arrier **D**etect (DCD), **R**ing **I**ndicator (RI), and **S**ignal **Q**uality **D**etect (SQD) signals from the modem, as well as determining the source of interrupt.

	BASE +4	BASE +4	BASE+5	BASE+6
BIT	**OUTPUT BIT**	**INPUT BIT**	**INPUT BIT**	**INPUT BIT**
D0	DTRA - 1 = ON	DSRA - 0 = ON	DTRA 1=ON	RS-232 = 0
D1	DTRB - 1 = ON	DSRB - 0 = ON	DTRB 1=ON	V.35 = 0
D2	X	SQD - 0 = ON	DCDA 0=ON	RS-530 = 0
D3	X	SCCIRQ - 0 = ON	RIA 0=ON	MIL188 = 0
D4	X	DCDB - 0 = ON	RIB 0=ON	X
D5	X	TCIRQ - 0 = ON	X	X
D6	IRQ ENABLE - 1 = ON	IRQEN - 1= ON	X	X
D7	DMA ENABLE -1 = ON	DMAEN - 1= ON	X	X

Figure 3
Status and Control Port Bit Definitions
"X" represents unused bits

SQD: **S**ignal **Q**uality **D**etect an input signal provided by some modems on pin 21 of the DB-25 connector. This signal is provided only when the RS-232 interface is selected

TCIRQ: **T**erminal **C**ount **IRQ** is generated when the DMA controller has transferred all of the programmed number of data bytes, and the DMA transfer is completed.

SCCIRQ: SCC generated interrupt indicating that the 8530 is requesting a data transfer or indicating a status change.

For both Channels A and B, the DCD and RI signals are "Or'ed" together to form the DCD input to the SCC. This is to allow the status change interrupt to generate an IRQ when "Ring" occurs. The assumption is that "Ring" is pulsing active low, and goes back to a high after the "Ring". This will not interfere with DCD, as RI returns high, allowing DCD to also generate status change interrupts. both of these signals are available as status inputs, allowing the program to determine which signal caused the IRQ.

Programming Note:
The ACB-VI can be setup to operate using a polling method, interrupts, or utilize system DMA. The most efficient method is a combination of DMA and interrupts. The ACB-VI has been optimized to generate an interrupt at the end of a DMA transfer. This will allow for DMA initialization and buffer management to take place at interrupt time and provide a virtually seamless communication channel. If the "**T**" option on header E9 is selected, an onboard latch will be set when Terminal Count for the selected DMA channel(s) is reached. This latch will cause an interrupt to be generated and program execution will be transferred to the application Interrupt Service Routine (ISR). The DMA Terminal Count Interrupt condition should be reset from the ISR by writing to BASE+5. The value that is written to this I/O location is irrelevant. If your application or driver is interrupting on mulitple conditions, reading the Status Register located at Base+4 will determine the source of the interrupt (SCC or DMA Terminal Count generated). Bit D3 in the Status Port corresponds to a SCC generated interrupt and bit D5 corresponds to an interrupt generated by the end of a DMA transfer. Bit D3 can only be reset by polling the SCC to determine the interrupt source and required action necessary to reset the interrupt. Please refer to the Software Toolkit and the 8530 Technical Manual for details and examples on interrupt driven and DMA programming examples.

SOFTWARE CONSIDERATIONS

Although interrupts are disabled when the ACB-VI is powered on and TCIRQ is preset by a system reset it is recommended to reset the TCIRQ latch ***Before*** enabling interrupts.

The 8530 SCC requires that successive I/O accesses ***Not Be Made*** to the SCC as this violates the SCC "Recovery Time". All programs written in Assembly Language and some C compilers should insert a short jump to meet this timing requirement. See below for example:

CORRECT:

```
MOV DX,3E0H
OUT DX,AL
JMP $+2
OUT DX,AL
```

INCORRECT:

```
MOV DX,3E0H
OUT DX,AL
OUT DX,AL
```

SECTION 4.

OPTION SELECTION

The ACB-VI contains several jumper straps which must be set for proper operation.

E11: Selects the interrupt request line for the port. If no interrupt is desired, remove the jumper.

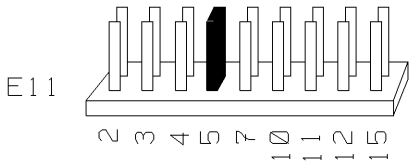

Figure 4
Header E11 (IRQ 5 Selected)

SECTION 4 (CONTINUED)

HEADER E9 SELECTIONS

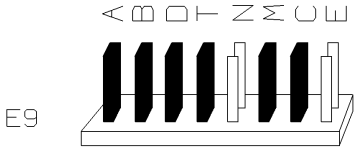

Figure 5
Shown in Factory Default

Set jumper to "**A**" to enable the DMA channel selected on E16. Jumper "**B**" enables the DMA channel selected on E15. Note that E15 corresponds to the 8530 signal WAIT/REQ and can be used for transmit or receive DMA transfer. Jumper E16 corresponds to the 8530 signal DTR/WAIT and can be used for transmit DMA transfers only. If you are using the ACB-VI in a full duplex DMA situation, set the transmit DMA channel on jumper E16 and the receive DMA channel on jumper E15. Removing the "**A**" and the "**B**" jumper will disable both DMA channels.

If the "**D**" jumper is installed, the DMA enable is controlled through software. If the jumper is installed, the DMA is enabled by setting (1) bit D7 in the Control Register at I/O location Base + 4. To disable DMA, reset (0) bit D7 at Base +4. If the jumper is removed DMA is always enabled.

Set jumper to "**T**" to enable the Terminal Count interrupt. When a DMA transfer is complete, the DMA count register rolls over to 65,535 (FFFF Hex). Once the Count Register reaches this number, the DMA transfer is complete, i.e. the Terminal Count has been reached. The ACB-VI card will generate an interrupt at the end of a DMA transfer if this option is selected. The status of the interrupt can be obtained by checking bit D5 in the status register at Base + 4. To clear the pending Terminal Count IRQ, read the I/O location at Base + 5 and reinitialize the DMA controller.

Set jumper to "**N**" for single interrupt mode. This setting is the normal setting for most applications.

Set jumper to "**M**" to include a 1K Ohm resistor needed in "Shared" interrupt mode. Be sure that only one port has the "**M**" jumper set or that only one resistor is in the circuit.

Note: ***If two or more ACB-VI cards are used in a bus set one jumper to "M" and set no jumpers at positions "N" or "M" on the other ACB-VI cards.***

In most instances the ACB-VI will receive both the RXC and TXC clocks from the modem or channel bank. For this reason both the RXC and TXC pins on P1 are always inputs and the SCC RTXC and TRXC pins (WR11) should be programmed as inputs unless TSET is used as an output. If the ACB-VI is to receive the TXC input clock on the TXC pin(s) install a jumper at "**C**".
If "C" is installed, the WR11 must be programmed for pin TRXC be an input. This signal received on TXC pin(s) of P1 will be eched the TSET pin(s) of P1.

If the board is to source a transmit clock, as in modem-less operation, remove jumper at "**C**" and program the SCC to generate a bit clock on the SCC TRXC pin (WR11), which will then be sent out on the TSET pin(s) of P1. The baud rate for the SCC can be set internally in the chip, using a programmed divisor and the oscillator frequency of 4.9152 Megahertz (Mhz).

Set jumper to "**E**" if the EIA-530 (and RS-485) transmit driver is to be enabled by the SCC signal **R**equest **T**o **S**end (RTS) With the jumper installed RTS enables the driver. Removing the jumper enables the driver regardless of RTS. This jumper should only be installed if you are running the board in a multi-drop polled environment such as RS-485, and you have software that knows how to "Talk" on the RS-485 bus. For normal point-to-point EIA-530 and RS-422, remove the jumper.

SECTION 4 (CONTINUED)

HEADER E15 & E16 SELECTIONS

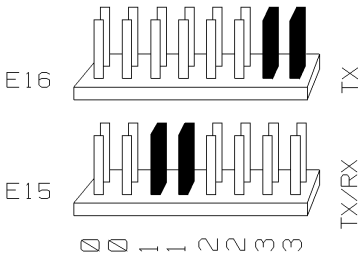

Figure 6
Header E15 & E16

E15 & E16 select DMA mode of operation. Channel A of the SCC will function in half duplex or full duplex DMA modes. Full duplex means that DMA can be used for simultaneous transmit and receive. Half duplex DMA means that you can either transmit, or receive with DMA. The 8530 has two signals that correspond to DMA request signals, WAIT/REQ and DTR/REQ. E15 corresponds to WAIT/REQ and E16 corresponds to DTR/REQ. WAIT/REQ and DTR/REQ can be programmed to serve a DMA request lines by setting the appropriate bits in Write Register 1 and Write Register 14 in the 8530. WAIT/REQ (E15) can be programmed for transmit or receive DMA transfers and DTR/REQ can be programmed for transmit only. For additional information on the programming of the 8530 please refer to the Zilog 8530 Technical Manual. Please note that each DMA channel is selected by two jumpers. Only one DMA channel may be selected for each header block.

SECTION 5.

INTERFACE SELECTION

Interface selection is as easy as installing five dip jumpers (shunts) in the correct sockets. The following table lists the sockets for each of the available interfaces. Please note that all 5 must be set correctly. Also note that each socket is labeled to indicate the interface selection it corresponds to. Please refer to the Silk-screen drawing provided as an aid in locating these positions.

INTERFACE	JUMPERS INSTALLED
RS-232	E1, E5, E8, E10, E17
EIA-530	E1, E4, E7, E12, E13
CCITT V.35	E1, E3, E6, E8, E17
MIL-188-114	E1, E2, E14, E18, E19
MIL-188-C	E2, E14, E17, E18, E19

SECTION 6.

CHANNEL A PIN DEFINITIONS

RS-232 SIGNALS

Signal	Name	Pin #	Mode
GND	Ground	7	
RD	Receive Data	3	Input RS-232
CTS	Clear To Send	5	Input RS-232
DSR	Data Set Ready	6	Input RS-232
DCD	Data Carr. Detect	8	Input RS-232
TD	Transmit Data	2	Output RS-232
RTS	Req. To Send	4	Output RS-232
TXC	Transmit Clock	15	Input RS-232
RXC	Receive Clock	17	Input RS-232
TSET	Tx. Sig. Element Tim	24	Output RS-232
DTR	Data Terminal Ready	20	Output RS-232
RI	Ring Indicator	22	Input RS-232
SQD	Signal Quality Detect	21	Input RS-232

V.35 SIGNALS

SIGNAL	NAME	DB-25 PIN #	V.35 PIN #	MODE
GND	Ground	7	B	
RDB RX+	Receive Positive	10	T	Input V.35
RDA RX-	Receive Negative	11	R	Input V.35
CTS	Clear To Send	5	D	Input RS-232
DSR	Data Set Ready	6	E	Input RS-232
DCD	Data Carr.Detect	8	F	Input RS-232
TDB TX+	Transmit Positive	12	S	Output V.35
TDA TX-	Transmit Negative	13	P	Output V.35
RTS	Request To Send	4	C	Output RS-232
TXCB TXC+	Transmit Clock Pos.	21	AA	Input V.35
TXCA TXC-	Transmit Clock Neg.	23	Y	Input V.35
RXCB RXC+	Receive Clock Pos.	24	X	Input V.35
RXCA RXC-	Receive Clock Neg.	25	V	Input V.35
TSETB TSET+	Tx. Signal Timing Pos.	19	W	Output V.35
TSETA TSET-	Tx. Signal Timing Neg.	18	U	Output V.35
DTR	Data Terminal Ready	20	H	Output RS-232
RI	Ring Indicator	22	J	Input RS-232

SECTION 6. **(CONTINUED)**

EIA- 530, RS-422 AND MIL 188 SIGNALS:

SIGNAL	NAME	PIN #	MODE
GND	Ground	7	
RDB RX+	Receive Positive	16	Input
RDA RX-	Receive Negative	3	Input
CTSB CTS+	Clear To Send Pos.	13	Input
CTSA CTS-	Clear To Send Neg.	5	Input
DSRB DSR+	Data Set Ready Pos.	22	Input
DSRA DSR	Data Set Ready Neg.	6	Input
DCDB DCD+	Data Carr. Detect Pos.	10	Input
DCDA DCD-	Data Carr. Detect Neg.	8	Input
TDB TX+	Transmit Positive	14	Output
TDA TX-	Transmit Negative	2	Output
RTSB RTS+	Req. To Send Pos.	19	Output
RTSA RTS-	Req. To Send Neg.	4	Output
DTRB DTR+	Data Term. Ready Pos.	23	Output
DTRA DTR-	Data Term. Ready Neg.	20	Output
TXCB TXC+	Transmit Clock Pos.	12	Input
TXCA TXC-	Transmit Clock Neg.	15	Input
RXCB RXC+	Receive Clock Pos.	9	Input
RXCA RXC-	Receive Clock Neg.	17	Input
TSETB TSET+	Terminal Timing Pos.	11	Output
TSETA TSET-	Terminal Timing Neg.	24	Output
RIA RI-	Ring Indicator Neg.	18	Input
RIB RI+	Ring Indicator Pos.	25	Input

NOTE: The EIA-530 pinout is adhered to except for the signal ***Ring Indicator*** which is not specified by EIA-530.

RS-422 / 530 LINE TERMINATION

Each receiver of the RS-422 / 530 line has a 100 ohm resistor across the input and a 1k ohm pull-up/pull-down combination bias the receiver inputs.

MIL 188-C / MIL 188-114 SELECTION

Installing jumper E17 will select MIL 188-C single ended signaling. Removing this jumper enables MIL 188-114 differential operation. Optional slew rate limiting capacitors can be installed at locations C28-C35. Please contact Sealevel Systems Technical Support for details.

NOTE: If the MIL 188-C interface is selected, only the signals marked Positive or + should be connected in your connector hood.

SECTION 6. (CONTINUED)

CHANNEL B PIN DEFINITIONS

RS-232 SCC CHANNEL B SIGNALS

SIGNAL	NAME	PIN #	MODE
GND	Ground	5	
RD	Receive Data	2	Input RS-232
CTS	Clear To Send	8	Input RS-232
DSR	Data Set Ready	6	Input RS-232
DCD	Data Carr. Detect	1	Input RS-232
RI	Ring Indicator	9	Input RS-232
TD	Transmit Data	3	Output RS-232
RTS	Request To Send	7	Output RS-232
DTR	Data Terminal Ready	4	Output RS-232

CABLE OPTIONS

Several cabling options are available from Sealevel Systems, including RS-449 adapters and V.35 cables. Please contact Sealevel Systems Technical Support for more information on cabling options.

SECTION 7.

SPECIFICATIONS

ENVIRONMENTAL SPECIFICATIONS

Specification	Operating	Storage
Temperature range	0 - 50 Degrees C 32 - 122 Degrees F	-20 - 70 Degrees C -40 - 100 Degrees F
Humidity Range	0- 90% R.H. Non-Condensing	0- 90% R.H. Non-Condensing

PERFORMANCE SPECIFICATIONS

MTBF > 150,000 Hours
MTTR < .25 Hours
Turnaround For Repair - 5 Working Days

MANUFACTURING SPECIFICATIONS

- IPC 610-A Class-III standards adhered to with a 0.1 visual A.Q.L. and 100% Functional Testing.
- Boards are built to U.L. 94V0 rating and are 100% Electrically tested. Boards are Solder Mask over bare Copper or Solder Mask over Tin Nickel.

POWER SPECIFICATIONS

SUPPLY LINE	+5Vdc	-5Vdc	-12Vdc	+12Vdc
RS-232	830mA	85mA	25mA	25mA
RS-530	900mA	85mA	25mA	25mA
V.35	800mA	85mA	25mA	25mA
MIL 188-114	960mA	200mA	25mA	25mA

BOARD SIZE

The maximum length of the board as measured from the rear board bracket is 13.330" . The height of the board as measured from the motherboard edge connector is 4.2". These measurements are held to +/- .010 inches in manufacturing.

SECTION 8.

WARRANTY

Sealevel Systems, Inc. provides a lifetime warranty for this product. Should this product fail to be in good working order at any time during this period, Sealevel Systems will, at it's option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Sealevel Systems assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Sealevel Systems will not be liable for any claim made by any other related party.

Return authorization must be obtained from Sealevel Systems before returned merchandise will be accepted. Authorization can be obtained by calling Sealevel Systems and requesting a Return Merchandise Authorization (RMA) Number.

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Please Refer To Your Included Diskette For Any Post Production Manual Updates And Application Specific Information.