SEALEVEL
SYSTEMS INCORPORATED

PIO-48™
PART # 4030
USER MANUAL

Sections:

Figures:

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SECTION 1.

Installation

The PIO-48 can be installed in any of the PC expansion slots, except J8 on the original IBM "XT" and Portable. Remove the PC case, remove the blank metal slot cover, and insert the board. Replace the screw, replace the case, and the installation is complete.

Be sure to set the address and jumper options before installation.

SECTION 2.

Address Selection

The PIO-48 occupies 8 consecutive I/O locations. Dip-switch SW1 sets the base address for the PIO-48. Be careful when selecting the base address as some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict. 9 8 7 6 5 4 3

ADDRESS	BINARY	SWITCH POSITION SETTING:						
Hex	A9 A0	1	2	3	4	5	6	7
280-287	1010000XXX	OFF	ON	OFF	ON	ON	ON	ON
2A0-2A7	1010100XXX	OFF	ON	OFF	ON	OFF	ON	ON
2E8-2EF	1011101XXX	OFF	ON	OFF	OFF	OFF	ON	OFF
2F8-2FF	1011111XXX	OFF	ON	OFF	OFF	OFF	OFF	OFF
3E8-3EF	1111101XXX	OFF	OFF	OFF	OFF	OFF	ON	OFF
300-307	1100000XXX	OFF	OFF	ON	ON	ON	ON	ON
328-32F	1100101XXX	OFF	OFF	ON	ON	OFF	ON	OFF
3F8-3FF	1111111XXX	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Typically COM1: = 3F8h; COM2: = 2F8h; COM3: = 3E8h; COM4: = 2E8h.

Figure 1
Address Selection Table

The following illustration shows the correlation between the dip-switch setting and the address bits used to determine the base address. In the example below, the address 300 hex through 307 hex is selected. 300 HEX =11 0000 0XXX In binary representation.

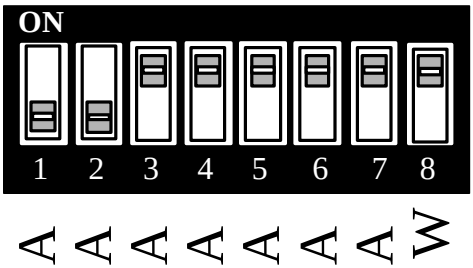

Figure 2
Dip-Switch Illustration

NOTE: Setting the switch "On" or "Closed" corresponds to a "0" in the address, while leaving it "Off" or "Open" corresponds to a "1".

SECTION 3.

Options

Wait States

The PIO-48 has the option of inserting one 500 nS wait state for each access. This may be required on certain machines with bus clocks in excess of 8 MHz. With the wide variety of machines available, no concrete rules exist concerning wait states. If the PIO-48 doesn't seem to be responding properly, try inserting a wait state.

To enable wait state insertion, set position 8 of the dip-switch to "ON". To disable wait states, set position 8 "OFF".

Interrupts

The headers marked J5 and J6 allow the use of interrupts with the parallel ports. J5 selects IRQ2 through IRQ7 for Port 1 (U9 and J1), while J6 selects the IRQ for Port 2 (U16 and J3).

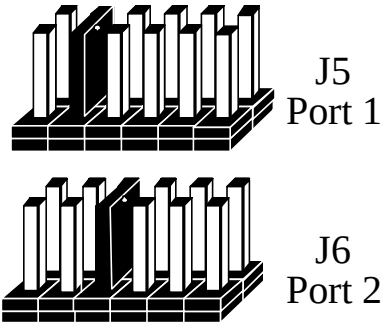

Figure 3
J5 & J6 Interrupt Header (Shown in Factory Default)

The interrupt input is available on the optional DB-37 cable connector at pin 1. This input is active high, logic level 1, and must be enabled by pin 2, interrupt enable, which is active low, or logic level 0. The enable line can be tied to ground if desired to always keep the interrupt enabled. This implementation allows either positive or negative logic input to cause an IRQ to be generated. Please contact Sealevel Systems Technical Support for further information.

The use of interrupts also requires special software to initialize the 8259 interrupt controller and set the appropriate interrupt service routine vector, etc. Please refer to the ***IBM Technical Reference Manual*** for more details.

SECTION 4.

TECHNICAL DESCRIPTION

The PIO-48 utilizes two 8255 Parallel input/output (I/O) chips. Each chip provides three eight-bit parallel I/O ports for a total of 48 I/O Lines. The ports within each 8255 are organized as ports A, B, C, and D. For further information on the functionality of the 8255 refer to the 8255 data sheets at the end of this manual.

Ports A, B and C, can be input or output, meaning that they can be read (or input from), and written (output) to. Port D is the ***Control Register***, which determines whether ports A, B and C are input or output. The Control Register sets the mode and direction for each port A, B, and C. On power-on reset, the 8255 is reset and initialized with all 24 I/O lines as inputs. The Control Register is normally written to at the beginning of a program, even if all ports are to be input ports.

I/O port offset addresses from Base Address (ex. 300 Hex)

8255 #1 (U9)	PORT A	300 HEX	768 DECIMAL	I/O PORT
	PORT B	301 HEX	769 DECIMAL	I/O PORT
	PORT C	302 HEX	770 DECIMAL	I/O PORT
	PORT D	303 HEX	771 DECIMAL	CONTROL REGISTER
8255 #2 (U16)	PORT A	304 HEX	772 DECIMAL	I/O PORT
	PORT B	305 HEX	772 DECIMAL	I/O PORT
	PORT C	306 HEX	774 DECIMAL	I/O PORT
	PORT D	307 HEX	775 DECIMAL	CONTROL REGISTER

Software Installation

For proper operation install software first. To install the software place the CD in your CD-ROM tray and the auto-run program will start. If auto-run is not available, browse the CD and choose “index.htm”. Choose **Install Software** at the beginning of the CD. Select the **Digital I/O** software drivers and install **SeaIO** prior to installing hardware.

Connectors

The PIO-48 provides two connectors for each port. The first connector (J1 and J3) is a 50 pin header designed to mate with an optional ribbon cable to a solid state relay I/O module rack. The second connector, (J2 and J4) is a 40 pin header that connects through an optional ribbon cable to a DB-37 (male) connector that matches the pin-out of the Metrabyte™ PIO-12 board. These cables are available from Sealevel Systems.

Connector Pin-Out

PORT BIT	J1, J3 50 PIN	J2, J4 40 PIN	DB-37 CABLE
PORT A			
0	47	36	37
1	45	34	36
2	43	32	35
3	41	30	34
4	39	28	33
5	37	26	32
6	35	24	31
7	33	22	30
PORT B			
0	31	19	10
1	29	17	9
2	27	15	8
3	25	13	7
4	23	11	6
5	21	9	5
6	19	7	4
7	17	5	3
PORT C			
0	15	20	29
1	13	18	28
2	11	16	27
3	9	14	26
4	7	12	25
5	5	10	24
6	3	8	23
7	1	6	22
Power, Ground and Interrupt Connections			
Ground	2-50	4,21,25,29,33,37	11,13,15,17,19,21
Interrupt Input	N/C	1	1
Interrupt Enable/	N/C	3	2
+5 Volts	49	2,35	20
-5 Volts	N/C	23	12
+12 Volts	N/C	31	16
-12 Volts	N/C	27	14

Programming With The API

Application Programmers Interface (API)

Most modern operating systems do not allow direct hardware access. The SeaIO driver and API have been included to provide control over the hardware in Windows and Linux environments.

The purpose of this section of the manual is to help the customer with the mapping of the API to the actual inputs for the 4030 specifically. Complete documentation of the API can be found in its accompanying help file.

Reading the Inputs:

The API presents the inputs as active low. If an input is driven high (2V to 5.25 V) it will read as a logical zero (0), if driven low (0V to 0.8V) it will read as a logical one (1).

Reading the Outputs:

The API returns the complement of value that is currently being used to drive the outputs. The outputs cannot be read with relative addressing, absolute addressing must be used. Refer to **Relative Addressing vs. Absolute Addressing** for more information.

Writing the Outputs:

The outputs are active high. Writing a one (1) corresponds to 5V while writing a zero (0) corresponds to 0V, at the output.

Interrupts:

Interrupt sampling can be set up in the API. Refer to the API section in the SeaI/O help file for more detailed information.

Port C

Port C of each bank has the ability to be configured as two four bit ports. If both lower and upper nibbles are configured the same then no special considerations need to be made. But if they are configured differently, one nibble as input, and one as output then the user will have to keep this in mind.

Port C absolute addressing (when port C is split)

When reading, the input nibble will be returned on the corresponding upper or lower nibble while the outputs will be returned on their corresponding upper or lower nibble. When writing, the corresponding nibble will be written to the output nibble, while the input nibble will have its output register written to. The output register can be written to without affecting the inputs. These will be eight bit operations and it will up to the programmer to keep track of the two four bit nibbles.

Port C relative addressing (when port C is split)

The input and output nibbles will each be treated as individual four bit ports.

Port Configuration:

Each eight-bit port can be configured as inputs or outputs. The API provides a set adapter state call to access the control words. For this device, two control word is used. Refer to the following table.

Note: The control panel also allows you to configure the device. Your program can over ride the control panel configuration when executed, but the control panel configuration will be the default on power up. The default settings are based on the settings in the control panel application when last changed and saved after re-booting.

8255 Control Word 0: Bank 1 (A1, B1, C1)
8255 Control Word 1: Bank 2 (A2, B2, C2)

Relative Addressing vs. Absolute Addressing

The SeaIO API makes a distinction between "absolute" and "relative" addressing modes. In absolute addressing mode, the Port argument to the API function acts as a simple byte offset from the base I/O address of the device. For instance, Port #0 refers to the I/O address base + 0; Port #1 refers to the I/O address base + 1.

Relative addressing mode, on the other hand, refers to input and output ports in a logical fashion. With a Port argument of 0 and an API function meant to output data, the first (0^{th}) output port on the device will be utilized. Likewise, with a Port argument of 0 and an API function designed to input data, the first (0^{th}) input port of the device will be utilized.

In all addressing modes, port numbers are zero-indexed; that is, the first port is port #0, the second port is #1, the third #2, and so on.

Tables : API Port/bit reference numbers for Absolute and Relative Addressing
R = Read
W = Write
R/W = Read or Write

Port	API Port # Absolute Address (function)
A1	0 (R/W)
B1	1 (R/W)
C1	2 (R/W)
A2	4 (R/W)
B2	5 (R/W)
C2	6 (R/W)

Absolute byte Address (any configuration)

Port	API Port # Relative Address (function)	Port Type
A1	0 (R)	Input
B1	1 (R)	Input
C1	2 (R)	Input
A2	0 (W)	Output
B2	1 (W)	Output
C2	2 (W)	Output

Relative byte Address Given: Inputs A1, B1, C1,
Outputs A2, B2, C

SECTION 5.

SPECIFICATIONS

Environmental Specifications

SPECIFICATION	OPERATING	STORAGE
Temperature Range	0 - 50 Degrees C 32 - 122 Degrees F	-20 - 70 Degrees C -4 - 158 Degrees F
Humidity Range	10 - 90% R.H. Non Condensing	10 - 90% Non Condensing

Manufacturing Specifications

- IPC 610-A CLASS-III standards adhered to with a 0.1 visual A.Q.L. and 100% Functional Testing.
- Boards are built to U.L. 94V0 rating and are 100% Electrically tested. Most boards are solder mask over bare copper.

Power Specifications

Supply Line	+5	+12	-12
Rating (mA)	200 mA	25 mA	25 mA

SECTION 6.

Warranty

Sealevel Systems, Inc. provides a lifetime warranty for this product. Should this product fail to be in good working order at any time during this period, Sealevel Systems will, at it's option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Sealevel Systems assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Sealevel Systems will not be liable for any claim made by any other related party.

Return authorization must be obtained from Sealevel Systems before returned merchandise will be accepted. Authorization can be obtained by calling Sealevel Systems and requesting a Return Merchandise Authorization (RMA) Number.

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