Differential Nonlinearity in Analog Measurements

Q: In a previous answer you noted, "… most applications require linearity but not absolute precision…" What does that mean?

A: Typically it means differential nonlinearity, or DNL. The DNL information indicates the difference between the measured difference between a perfect change of one LSB voltage weight between two adjacent codes in the ADC. I'll use a few diagrams (Figures 4, 5 and 6.) to show what that means for the digital output vs. analog-voltage input for a 3-bit ADC.

As the ADC's input signal increases from 0 to 7 volts, the ADC 3-bit output code changes from 0002 to 1112. Note the ADC output code changes at voltages of 0.5V, 1.5V, 2.5V, and so on up through 6.5 volts. An ADC output code doesn't represent one voltage; it represents a range of voltages. We express this range in terms of the voltage weight of the ADC's LSB. For the 3-bit ADC results shown in Figure 4, the LSB has a weight of 1volt, so each ADC voltage step varies by ±1 LSB, or ±1 volt. Thus an output code of 1012 indicates an input voltage between 4.5 and 5.5 volts.

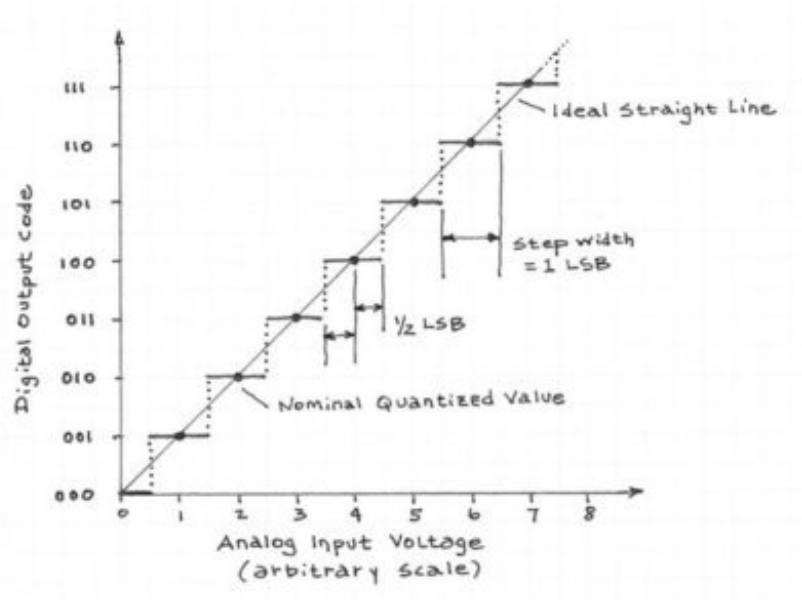

Figure 4. A perfect 3-bit output (000_2 to 111_2) for an input signal between 0 and 7 volts. The ideal straight line represents the increasing voltage applied to the ADC.

The diagram in **Figure 5** shows results from a 4-bit ADC, with the ideal ADC operation shown in the right. The plot on the left includes examples of differential nonlinearity (DNL) in which individual steps do not follow the ideal-ADC performance. The figure exaggerates the DNL. This diagram also illustrates integral nonlinearity (INL) which describes the variation between perfect linear response and for an ideal ADC.

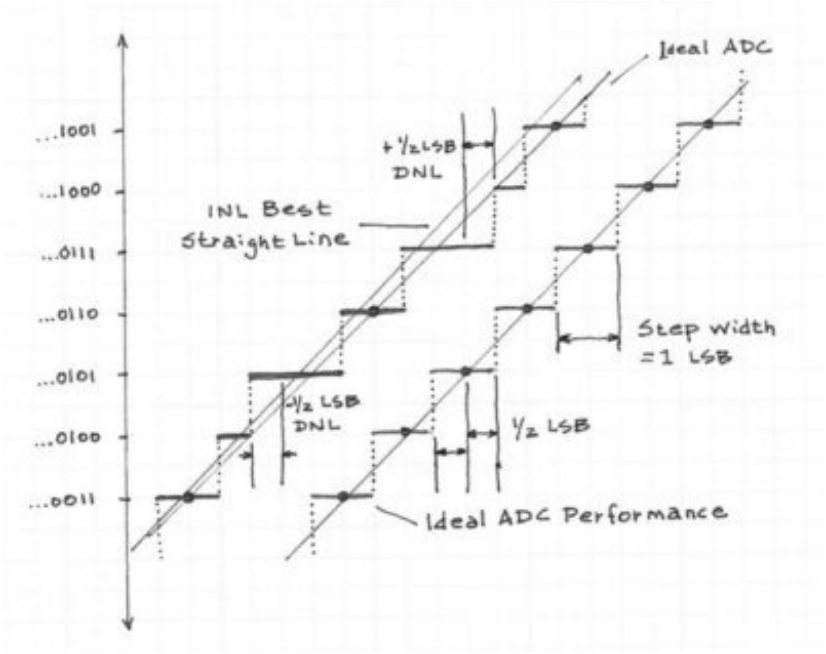

Figure 5. Plots for an ideal ADC (right) and for an ADC that shows differential and integral nonlinearity errors.

I have included **Figure 6** so you can see the effect of an offset and a gain error in ADC performance. An offset error “moves” the ADC results to a higher or lower voltage across the entire measurement range. Thus you still have good resolution, but the actual and measured voltages have a constant voltage offset, or error. The gain error shows an error that increases as the input voltage increases.

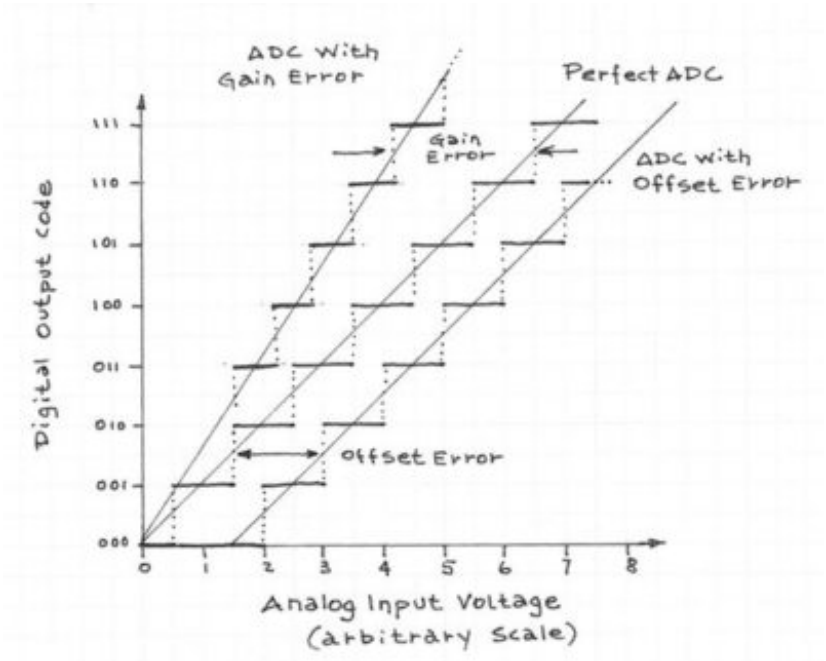

Figure 6. Plots of ADC behavior that show a gain error and an offset error in the digital outputs. These plots exaggerate the errors for the sake of clarity.