OpenSPARC™ T1 Processor Datasheet

8 Cores, 1.2 GHz, 3 Mbyte L2-cache, DDR2 SDRAM and J-Bus Interface

Sun Microsystems, Inc.
www.sun.com

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Preface

This document describes the OpenSPARC™ T1 processor, which is the first chip multiprocessor that fully implements the Sun™ Throughput Computing Initiative.

How This Document Is Organized

This document is organized as described in the following paragraph.

Chapter 1 is a datasheet that describes the OpenSPARC T1 processor from Sun Microsystems, Inc.™

Using UNIX Commands

This document might not contain information about basic UNIX® commands and procedures such as shutting down the system, booting the system, and configuring devices. Refer to the following for this information:

- Software documentation that you received with your system
- Solaris™ Operating System documentation, which is at:

  `http://docs.sun.com`

Shell Prompts

Shell	Prompt
C shell	*machine-name*%
C shell superuser	*machine-name*#
Bourne shell and Korn shell	$
Bourne shell and Korn shell superuser	#

Typographic Conventions

Typeface*	Meaning	Examples
AaBbCc123	The names of commands, files, and directories; on-screen computer output	Edit your .login file. Use ls -a to list all files. % You have mail.
AaBbCc123	What you type, when contrasted with on-screen computer output	% **su** Password:
AaBbCc123	Book titles, new words or terms, words to be emphasized. Replace command-line variables with real names or values.	Read Chapter 6 in the *User's Guide*. These are called *class* options. You *must* be superuser to do this. To delete a file, type rm *filename*.

* The settings on your browser might differ from these settings.

Related Documentation

The documents listed as online are available at:

`http://www.opensparc.net`

Application	Title	Part Number	Format	Location
OpenSPARC T1 instruction set	*UltraSPARC Architecture 2005 Specification*	950-4895-03	PDF	Online
OpenSPARC T1 processor internal registers	*UltraSPARC T1 Supplement to the UltraSPARC Architecture 2005*	819-3404-02	PDF	Online
OpenSPARC T1 processor J-Bus and SSI interfaces	*OpenSPARC T1 Processor External Interface Specification*	818-5014-10	PDF	Download
OpenSPARC T1 megacells	*OpenSPARC T1 Processor Megacell Specification*	819-5016-10	PDF	Download
Running simulations and synthesis on the OpenSPARC T1 processor	*OpenSPARC T1 Processor Design and Verification User's Guide*	819-5019-10	PDF	Download

Documentation, Support, and Training

Sun Function	URL
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OpenSPARC T1 Processor Datasheet, part number 819-5015-10

CHAPTER 1

OpenSPARC T1 Processor

This chapter gives details on the following topics:

1.1 Description

The OpenSPARC T1 processor is the first chip multiprocessor that fully implements the Sun Throughput Computing Initiative. Each of the eight SPARC® processor cores has full hardware support for four threads. Each SPARC core has an instruction cache and data cache and fully associative instruction and data translation lookaside buffers (TLB). The eight SPARC cores are connected through a crossbar to an on-chip unified Level 2 cache (L2-cache). The four on-chip dynamic random access memory (DRAM) controllers directly interface to double data rate-synchronous DRAM (DDR2 SDRAM). In addition, there is an on-chip J-Bus controller. The OpenSPARC T1 processor is a highly integrated processor that implements the 64-bit SPARC V9 architecture. This processor targets commercial applications such as application servers and database servers.

1.2 Features

The OpenSPARC T1 processor features include the following:

CPU

- SPARC V9 Architecture

- On-chip L2-cache
- 48-bit virtual, 40-bit physical address space

Caches

- 16 Kbyte primary instruction cache per core
  - Parity
- 8 Kbyte primary data cache per core
  - Parity
- 3 Mbyte unified L2-cache
  - Error correction code (ECC)
  - 12-way set-associative, 4 banks

Integration

- 8 cores, 4 threads per core
- Four 144-bit DDR2-533 SDRAM interfaces
  - Quad error correction, octal error detection, chipkill ECC
  - Optional 2-channel operation mode
- J-Bus Interface
  - 2.56 Gbyte/sec peak effective bandwidth
  - 128-bit address or data bus
  - 150–200 MHz operation

1.3 Functional Overview

The section provides more detailed functional information.

1.3.1 OpenSPARC T1 Description

FIGURE 1-1 shows a block diagram of the OpenSPARC T1 processor illustrating the various interfaces and integrated components of the chip. The OpenSPARC T1 processor functions and capabilities include the following:

- Eight SPARC single-issue processor cores
- Support for four threads on each core
- 64-bit data paths
- 48-bit virtual address and 40-bit physical address space
- J-Bus controller

- 16 Kbyte primary instruction cache memory per core
- 8 Kbyte primary data cache memory per core
- 64-entry fully associative instruction TLB per core
- 64-entry fully associative data TLB per core
- 3 Mbyte unified L2-cache
- Four DRAM controllers interfacing to DDR2 SDRAM

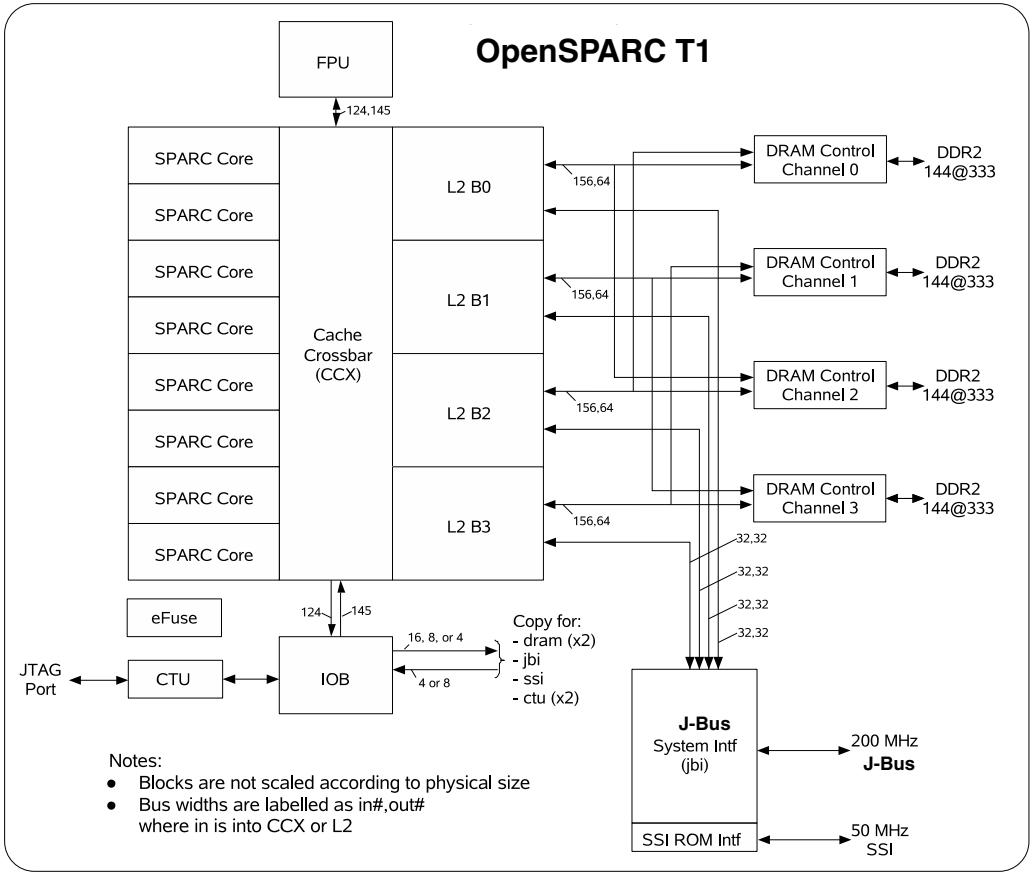

FIGURE 1-1 OpenSPARC T1 Processor Block Diagram

1.3.2 OpenSPARC T1 Processor Components

This section provides further detail regarding the OpenSPARC T1 components.

1.3.2.1 SPARC Core

Each SPARC core has hardware support for four threads. This support consists of a full register file (with eight register windows) per thread, with most of the address space identifiers (ASI), ancillary state registers (ASR), and privileged registers replicated per thread. The four threads share the instruction and data caches and TLBs. Each instruction cache is 16 Kbytes with a 32-byte line size. The data caches are write through, 8 Kbytes, and have a 16-byte line size. An autodemap feature is included with the TLBs to enable the multiple threads to update the TLB without locking.

1.3.2.2 Floating-Point Unit

A single floating-point unit (FPU) is shared by all eight SPARC cores. The shared floating-point unit is sufficient for most commercial applications in which typically less than 1% of the instructions are floating-point operations.

1.3.2.3 L2-cache

The L2-cache is banked four ways, with the bank selection based on physical address bits 7:6. The cache is 3 Mbyte, 12-way set-associative with pseudo-least recently used (LRU) replacement (replacement is based on a used bit scheme). The line size is 64 bytes. Unloaded access time is 23 cycles for an L1 data cache miss and 22 cycles for an L1 instruction cache miss.

1.3.2.4 DRAM Controller

The OpenSPARC T1 processor's DRAM controller is banked four ways (a two-bank option is available for cost-constrained minimal memory configurations), with each L2 bank interacting with exactly one DRAM controller bank. The DRAM controller is interleaved based on physical address bits 7:6, so each DRAM controller bank must have identical dual in-line memory modules (DIMM) installed and enabled.

The OpenSPARC T1 processor uses DDR2 DIMMs and can support one or two ranks of stacked or unstacked DIMMs. Each DRAM bank/port is two-DIMMs wide (128 bit + 16 bit ECC). All installed DIMMs must be identical, and the same number of DIMMs (that is, ranks) must be installed on each DRAM controller port. The DRAM controller frequency is an exact ratio of the core frequency, where the core frequency must be at least three times the DRAM controller frequency. The double data rate (DDR) data buses transfer data at twice the frequency of the DRAM controller frequency.

1.3.2.5 I/O Bridge

The I/O bridge (IOB) performs an address decode on I/O-addressable transactions and directs them to the appropriate internal block or to the appropriate external interface (J-Bus or serial system interface). In addition, the IOB maintains the register status for external interrupts.

1.3.2.6 J-Bus Interface

The J-Bus interface (JBI) is the interconnect between the OpenSPARC T1 processor and the I/O subsystem. J-Bus is a 200 MHz, 128-bit wide, multiplexed address or data bus, used predominantly for direct memory access (DMA) traffic, plus the programmable input/output (PIO) traffic to control it.

The J-Bus interface is the block that interfaces to J-Bus, receiving and responding to DMA requests, routing them to the appropriate L2 banks, and also issuing PIO transactions on behalf of the processor threads and forwarding responses back.

1.3.2.7 Serial System Interface

The OpenSPARC T1 processor has a 50 Mbyte/sec serial system interface (SSI) that connects to an external application specific integrated circuit (ASIC), which in turn interfaces to the boot read-only memory (ROM). In addition, the SSI supports PIO accesses across the SSI, thus supporting optional control status registers (CSR) or other interfaces within the ASIC.

1.3.2.8 Electronic Fuse

The electronic fuse (e-Fuse) block contains configuration information that is electronically burned in as part of manufacturing, including part serial number and core available information.

1.3.3 OpenSPARC T1 Memory System

The OpenSPARC T1 chip supports four memory channels. For low-cost system configurations, a two-channel mode can be selected by means of software-programmable control registers. Each channel supports DDR2 JEDEC standard DIMMs. The type of DRAM components supported are 256 Mbit, 512 Mbit, 1 Gbit and 2 Gbit. The maximum speed of the DIMMs supported is 200 MHz clock (400 MHz data rate). The controller works on single-ended DQS only and has the capability to detect any double-nibble error or correct any single-nibble error

contained in one 144-bit chunk. The controller always assumes that additive latency (AL) is zero. The maximum physical address space supported by the controller is 128 Gbytes (37 bits of physical address).

The OpenSPARC T1 chip contains an on-die termination (ODT) feature that is selectable in the DRAM Read Enable Clock Invert, ODT enable mask, and VREF control register. The purpose of this feature is to improve read timing by reducing the intersymbol interference (ISI) effects on the network. This feature terminates the DQ and DQS pins with the equivalent of 150 ohms (Ω) to VDD18/2 under all conditions except when the DQ and DQS pins are enabled during write transactions.

Further information on memory initialization and DRAM control and status registers can be found in the memory controller section of the *UltraSPARC T1 Processor Supplement*.

1.3.4 OpenSPARC T1 Clock Architecture

Three synchronous clock domains are on the OpenSPARC T1 processor – CMP (for SPARC and caches), J-Bus (for IOB and JBI), and DRAM (for the DRAM controller and external DIMMs). All of these are sourced from the same phase-locked loop (PLL). Synchronization pulses are generated to control transmission of signals and data across clock domain boundaries.

The clock and test unit (CTU) is responsible for resetting the PLL and counting the lock period. Once sufficient time has passed to enable the PLL to have locked, the clock control logic is responsible for enabling distribution below the cluster levels by turning on cluster enables.

Further information on the OpenSPARC T1 clock architecture, including sequences for changing input clock frequency or clock ratios, clock control registers, PLL bypass, stop and scan support, and clock stretch, can be found in the *UltraSPARC T1 Processor Supplement*.

1.3.5 OpenSPARC T1 Reset Architecture

The processor has two flavors of reset – power-on reset (POR) and warm reset. POR is defined as the reset event arising from turning power on to the chip and is triggered by assertion of power-on reset. Warm reset encompasses all resets when the chip has been in operation prior to the event triggering the reset.

The reset state of software-visible registers is specified in the *UltraSPARC T1 Processor Supplement*.

1.3.6 JTAG and Boundary Scan

The CTU contains the JTAG block, which enables access to the shadow scan chains. The unit also has a control register (CREG) interface that enables the JTAG to issue reads of any I/O-addressable register, some ASI locations, and any memory location while the processor is in operation.

The OpenSPARC T1 processor contains an IEEE 1149.1-compliant test access port (TAP) controller with the standard five-pin JTAG interface. In addition to the standard IEEE 1149.1 instructions, roughly 20 private instructions provide access to the processor's design for testability (DFT) features.

1.3.7 OpenSPARC T1 Special RAS Features

The OpenSPARC T1 processor includes many special features for reliability, availability, serviceability (RAS), and related areas. Several of these are described in the following sections.

1.3.7.1 Memory Chipkill Error Correction

The processor supports chipkill error correction for main memory. Any error contained within a single-aligned memory nibble (4b) can be corrected, and any error that is contained within any two nibbles can be detected as uncorrectable.

1.3.7.2 Memory Hardware Scrubber

Each OpenSPARC T1 DRAM controller has a background hardware error scanner and scrubber to reduce the incidence of multinibble errors. If a correctable error is found, the error is logged, corrected, and written back (scrubbed in hardware) to memory. The L2-cache also has a background scanner and scrubber.

1.3.7.3 Thermal Diode and Throttle Control

The processor has an on-chip thermal diode connected to I/O pins, enabling system hardware to obtain a rough measure of the chip temperature. If an overtemperature condition is detected, the CPU can be shut down, or CPU utilization can be throttled to reduce power consumption.

1.3.7.4 Performance Counters

Each OpenSPARC T1 SPARC thread has two performance counters that count instructions plus occurrences of one other event. The possible other events include cache misses of various types, TLB traps, and store buffer full occurrences. Counts can be qualified to count events in User mode, Supervisor mode, or both.

Two counters in each DRAM controller can be used to count transactions and latency for different operations, which can be used to compute average latency.

The J-Bus unit also has two performance counters. Like the DRAM counters, these counters can be used to count events and latencies and to compute average latency.

1.3.7.5 Shadow Scan

In addition to the usual scan chains, the processor has shadow scan capability. This enables scan extraction of some of the processor state while execution continues. Shadow scan is provided on a per-thread basis for the SPARC cores. The rest of the chip has a separate shadow scan chain.

1.3.7.6 Debug Ports

The OpenSPARC T1 processor contains both a dedicated debug port (Debug Port A) and a J-Bus debug port (Debug Port B). The debug port target bandwidth for logic analysis is 40 bits at J-Bus frequency, which is matched to the width of a single internal debug port selection. This bandwidth is sufficient for an address header every J-Bus cycle.

1.4 Signal Description

This section provides a detailed description of OpenSPARC T1 signals. The signals are arranged in functional groups according to their associated interface.

1.4.1 Signal Overview

The processor primarily consists of DDR2 400 SDRAM signals and J-Bus signals. FIGURE 1-2 shows the main interfaces and the number of signals.

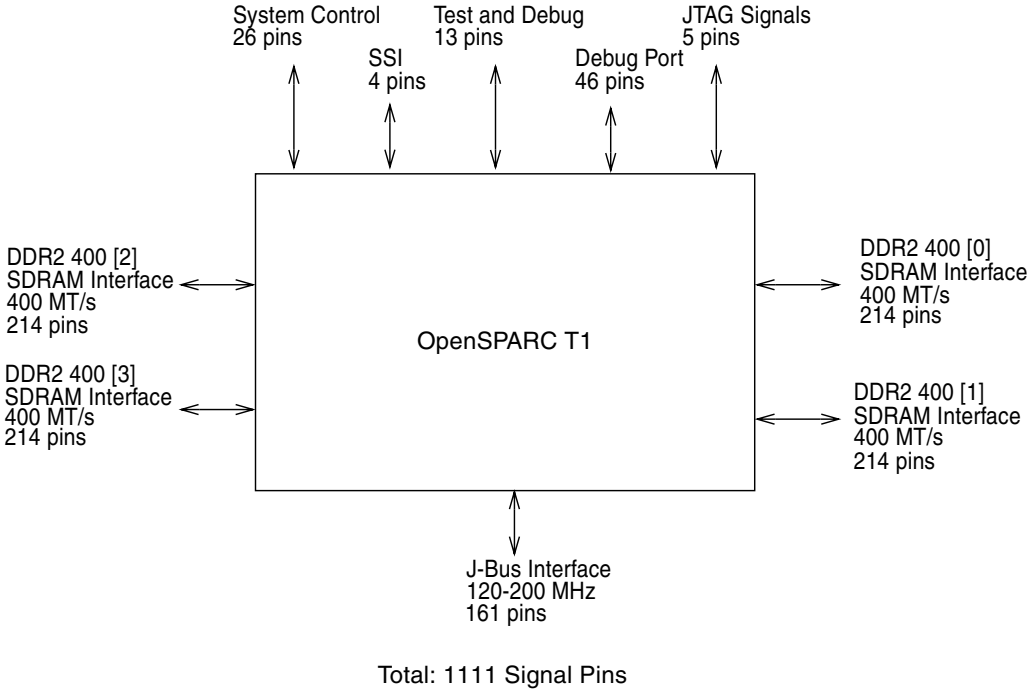

FIGURE 1-2 OpenSPARC T1 Signals

The following table lists the OpenSPARC T1 Processor signal pins including the I/O pins on each group. Spare pins are excluded from this description.

TABLE 1-1 OpenSPARC T1 Processor Signal Description

Group	Pins
DDR2 400 SDRAM interface signals (4 channels)	856
J-Bus interface signals	161
Serial system interface	4
Debug port signals	46
System control signals	26

TABLE 1-1 OpenSPARC T1 Processor Signal Description *(Continued)*

Group	Pins
Test and debug signals	13
JTAG – IEEE 1149.1 test access port signals	5
Total number of OpenSPARC T1 signal pins	**1111**

1.4.2 DDR2 400 SDRAM Interface Signals

The OpenSPARC T1 processor has four DDR2 SDRAM interface channels with 214 signals per channel for a total of 856 signals.

TABLE 1-2 DDR2 400 SDRAM Memory Interface Signal Description

SIGNAL NAME	I/O	TYPE	Vref	FUNCTION
DQ[127:0]*	I/O	SSTL-18 †	0.9‡	DIMM memory bus (128 bits).
DQS[35:0]	I/O			SDRAM data strobes (one strobe every four data bits).
CB[15:0]	I/O			DIMM ECC check bits.
ADDR[14:0]	O			SDRAM address bus.
CK_P[3:0]	O			SDRAM clock outputs (positive lines of four differential signal pairs).
CK_N[3:0]	O			SDRAM clock outputs (negative lines of four differential signal pairs).
CKE	O			SDRAM clock enable.
CS_L[3:0]	O			SDRAM chip select lines (active low).
RAS_L	O			SDRAM row address command (active low).
CAS_L	O			SDRAM column address command (active low).
WE_L	O			SDRAM write enable command (active low).
BA[2:0]	O			SDRAM bank address.

* The signal names shown are repeated for each of the four DDR2 channels. The actual pin names are the signal names as shown in the table preceded by the channel to which they belong. For example, the DQ pins on DDR2 channel 3 are named DRAM3_DQ[127:0].

† SSTL-18 is 1.8 V I/O power, with 0.9 V pull-up reference

‡ Vref is generated internally to the OpenSPARC T1 Processor processor. No external Vref pin is provided.

1.4.3 J-Bus Signals

The OpenSPARC T1 processor has 161 J-Bus interface signals.

TABLE 1-3 J-Bus Signal Description

SIGNAL NAME	I/O	TYPE	Vref	FUNCTION
J_REQ4_IN_L	I	DTL *	1.125 V	Incoming arbitration requests from other masters on J-Bus. Point-to-point topology.
J_REQ5_IN_L	I			Incoming arbitration requests from other masters on J-Bus. Point-to-point topology.
J_REQ0_OUT_L	O			Outgoing arbitration requests for J_AD. Point-to-point topology.
J_REQ1_OUT_L	O			Outgoing arbitration requests for J_AD. Point-to-point topology. (Functionally equivalent to J_REQ0_OUT_L).
J_AD[127:0]	I/O			J-Bus Address and Data multiplexed bus.
J_ADP[3:0]	I/O			Word parity for all J_AD transfer, and J_ADTYPE.
J_ADTYPE[7:0]	I/O			Identifies packet type on J_AD/J_ADP, and signal destination for returning read data. Read transaction ID for out of order data return.
J_PACK0[2:0]	I/O			Encoded snoop info and flow control, plus read data flow control, enabled by J_ID for port 0.
J_PACK1[2:0]	I/O			Encoded snoop info and flow control, plus read data flow control, enabled by J_ID for port 1.
J_PACK4[2:0]	I/O			Encoded snoop info and flow control, plus read data flow control, enabled by J_ID for port 4.
J_PACK5[2:0]	I/O			Encoded snoop info and flow control, plus read data flow control, enabled by J_ID for port 5.
J_PAR	I			Control parity check for J_REQ and J_PACK, driven by JIO every cycle.
J_ERR	O			Not used functionally but driven by any agent that detects an error condition in the J-Bus logic.
J_RST_L	I			System reset.
J_CLK[1:0]	I	Reduced PECL †		Differential PECL clock reference for PLL (120–200 MHz). J_CLK[0] is the positive sense clock and J_CLK[1] is the negative sense clock.

* DTL is 1.5 V I/O power, with 1.125 V pull-up reference.

† 1.1 V supply rail.

1.4.4 SSI Interface Signals

The OpenSPARC T1 processor has a four-signal serial system interface.

TABLE 1-4 SSI Signal Description

SIGNAL NAME	I/O	TYPE	Vref	FUNCTION
SSI_MOSI	O	HSTL*	0.75 V	SSI master out, slave in
SSI_MISO	I			SSI master in, slave out
SSI_SCK	O			SSI clock
EXT_INT_L	I			External interrupt

* HSTL is 1.5 V I/O power, with 0.75 V reference.

1.4.5 Debug Port Signals

The OpenSPARC T1 processor has 46 signals for a dedicated debug port.

TABLE 1-5 Debug Port Signal Description

SIGNAL NAME	I/O	TYPE	Vref	FUNCTION
DBG_DQ[39:0]		DTL *	1.125 V	Debug output
DBG_CK_P[2:0]				Debug output clock, positive true
DBG_CK_N[2:0]				Debug output clock, negative true

* DTL is 1.5 V I/O power, with 1.125 V pull-up reference.

1.4.6 System Control Signals

The OpenSPARC T1 processor has 26 system control signals.

TABLE 1-6 System Control Signal Description

SIGNAL NAME	I/O	TYPE	Vref	FUNCTION
DRAM01_P_REF_RES	I	Analog		PFET PVT impedance reference resistor.
DRAM01_N_REF_RES	I	Analog		NFET PVT impedance reference resistor.
DRAM23_P_REF_RES	I	Analog		PFET PVT impedance reference resistor.
DRAM23_N_REF_RES	I	Analog		NFET PVT impedance reference resistor.

TABLE 1-6 System Control Signal Description *(Continued)*

SIGNAL NAME	I/O	TYPE	Vref	FUNCTION
DTL_R_VREF	I	Analog		DTL voltage reference (1.125 V).
DTL_L_VREF	I	Analog		DTL voltage reference (1.125 V).
JBUS_P_REF_RES	I	Analog		PFET PVT impedance reference reference.
JBUS_N_REF_RES	I	Analog		NFET PVT impedance reference resistor.
DBG_VREF	I	Analog		Debug port voltage reference (DTL signaling type, 1.125 V).
DIODE_TOP[2:0]	O	Analog		Thermal diode – DIODE_TOP[2] is the emitter; DIODE_TOP[1] is the collector (P-substrate); DIODE_TOP[0] is the base.
DIODE_BOT[2:0]	O	Analog		Thermal diode – DIODE_BOT[2] is the emitter; DIODE_BOT[1] is the collector (P-substrate); DIODE_BOT[0] is the base.
TEMP_TRIG	I	HSTL	0.75 V	Interrupt input from temperature sensor.
PWRON_RST_L	I	CMOS		Power-on reset.
PLL_CHAR_IN	I	CMOS		Enables core clocks to be viewed through external differential pins. Also used to put PCM into “2-pin” mode. If high at reset, “Tester Warm Reset” is performed.
HSTL_VREF	I	Analog		HSTL Voltage reference (0.75 V).
VDD_SENSE	O	Analog		Core vdd sense pins (+). Three pins total.
VSS_SENSE	O	Analog		Core vss sense pins (-). Three pins total.
VREG_SELBG_L	I	CMOS		PLL voltage regulator bandgap select – selects which voltage reference to use for the on-chip analog voltage regulator. 0 = select bandgap, 1= 0.611*Vdda.

1.4.7 Test and Debug Signals

The OpenSPARC T1 processor has 13 test and debug signals.

TABLE 1-7 Test and Debug Signal Description

SIGNAL NAME	I/O	TYPE	Vref	FUNCTION
CLKOBS[1:0]	O	SSTL		Enables core clock parameters to be observed. Controlled through PLL_CHAR_IN pin.
TSR_TESTIO[1:0]	O	Analog		Temperature sensor analog out. Experimental temperature sensor. Not for use in system designs.
DO_BIST	I	DTL	1.125 V	Activate built-in self test.
TRIGIN	I	HSTL	0.75 V	Stop clock based on external event. When DO_BIST is asserted during reset, TRIGIN controls BISI/BIST selection.
TEST_MODE	I	CMOS		Mux pins into tester mode.
PGRM_EN	I	CMOS		e-Fuse program enable.
PMI	I	CMOS		Process control module input pin.
PMO	O	CMOS		Process control module output pin.
BURNIN	I	CMOS		Sets burnin mode for PCM modules.
CLK_STRETCH	I	HSTL	0.75 V	Clock stretch pin for tester.
TCK2	I	CMOS		Test clock input (for parallel scan use only).

1.4.8 JTAG – IEEE 1149.1 Test Access Port Controller Interface

The OpenSPARC T1 processor has five JTAG test access port (TAP) controller interface signals.

TABLE 1-8 JTAG- IEEE 1149.1 Test Access Port Interface Signal Descriptions

SIGNAL NAME	I/O	TYPE	Vref	FUNCTION
TRST_L	I	CMOS		IEEE 1149 test reset input (active low). Includes an on-chip pull-up resistor with a value between 1.2k ohms and 4.5k ohms.
TMS	I			IEEE 1149 test mode select input. Includes an on-chip pull-up resistor with a value between 1.2k ohms and 4.5k ohms.
TDI	I			IEEE 1149 test data input. Includes an on-chip pull-up resistor with a value between 1.2k ohms and 4.5k ohms.
TCK	I			IEEE 1149 test clock input.
TDO	O			IEEE 1149 test data output.

1.4.9 Power, Ground, Spares, and Unconnected Pins

Required power, ground, spares, and unconnected pins are physical-implementation dependent.