microSPARC™-IIep Design Application Note

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microSPARC™-IIep Design Application Note

This document explains how to set up and run a simulation of the microSPARC-IIep design. It contains the following sections:

Directory Structure

TABLE 1 details the directory structure for the microSPARC-IIep design database.

TABLE 1 Database Directory Structure

Directory	Contents
`diag`	Diagnostic routines and executables for Cadence Verilog-XL and Synopsys VCS
`docs`	Documentation and Verilog design code in HTML format
`env`	Executables and scripts for running the simulation and compilation of the results
`lib`	Generic components for design and RTL simulation
`log`	Simulation results. You can change this path according to the path for the environment variable `RESULTSDIR` in the `.cshrc` file.

TABLE 1 Database Directory Structure *(Continued)*

Directory	Contents
`ssparc`	Design code
`system`	Files related to the test bench
`tools`	`ssparc` tools, such as Verilog PLI routines and PCI interface models

Tool Requirements

To simulate the source distribution for the microSPARC-IIep design, you must use the following tools:

- Sun™ C compiler
- Perl (version 4.0) — Use Perl to run some of the simulation scripts, which may refer to the absolute path location of Perl. In that case, edit those scripts and point to the location in your environment, where you have installed Perl.
- A Verilog simulator — Use a simulator such as Cadence Verilog-XL (version 2.7.x) or Synopsys VCS (version 4.0.1) on the Solaris 2.5.x operating environment or a compatible version.

Note – The microSPARC-IIep design kit supports the Sun C compiler only. Though the design may function correctly with other Verilog simulators, Sun has tested the microSPARC-IIep RTL core with Cadence Verilog-XL and Synopsys VCS only. In addition, that design kit uses the Sun `make` utility and does not support GNU `make`.

Setup of the Simulation Environment

To set up the simulation environment, do the following:

1. **Assuming you use the `csh` shell, edit the `user.cshrc` file in the `env` directory to reflect the correct paths and define the appropriate environment variables and paths for the Verilog simulator and C compiler.**

   A template of the `user.cshrc` file, as shown in CODE EXAMPLE 1, is in: `$SPARCV8HOME/$PROJECT/user.cshrc`. Comments are preceded by the # symbol.

CODE EXAMPLE 1 Contents of the `user.cshrc` Template File In the `env` Directory

```
### Set the environment variable SPARCV8HOME, as follows.

setenv SPARCV8HOME directory-where-you-untarred-the-distribution
setenv PROJECT sparc_v8

### Set the environment variables for the Sun C compiler, as follows.

setenv CC_PATH path-for-the-Sun-C-compiler
setenv CC_NAME cc

### Set the environment variable RESULTSDIR, which points to the directory
### where to store regression results, as follows. Create one if that directory
### does not exist. By default, it points to:
### $SPARCV8HOME/$PROJECT/log/results.
### You must create the directories SPARCV8HOME/$PROJECT/log and
### SPARCV8HOME/$PROJECT/log/results.

setenv RESULTSDIR $SPARCV8HOME/$PROJECT/log/results

### Set the paths for the Verilog executables, as follows.

# Define the location of simv, the Synopsys VCS executable compiled with the RTL
# code.

setenv SIMV_PATH $SPARCV8HOME/$PROJECT/diag/vcs

# If you plan to run RTL simulations with Cadence Verilog-XL, set the following
# environment variables.

setenv VERITOOLS_PATH path-to-the-Verilog-tools-directory
setenv VLOG_PATH path-to-the-Verilog-directory
# Example: setenv VLOG_PATH $VERITOOLS_PATH/verilog
setenv VLOG_NAME generated-executable-of-Verilog-XL-
# Example: setenv VLOG_NAME my_verilog

# Define the location of vlist, the configuration file that lists the Verilog
# files that are required to run simulations.

setenv VLIST_PATH $SPARCV8HOME/$PROJECT/diag

# Set the Library path for the tools.

setenv LD_LIBRARY_PATH ${LD_LIBRARY_PATH}:$VERITOOLS_PATH/lib
```

CODE EXAMPLE 1 Contents of the `user.cshrc` Template File In the `env` Directory

```
# Set the path for the additional library for compilation of the Verilog-XL
# executable.

setenv LD_LIBRARY_PATH ${LD_LIBRARY_PATH}:${VERITOOLS_PATH}/tools/lib

# If you plan to run RTL simulations with Synopsys VCS, ensure that VCS is on
# your path. Also, define the environment variables for running VCS and their
# paths.

# Define the environment variables and paths for the EDA tools.

# Source the project-specific environment variables.

source $SPARCV8HOME/$PROJECT/env/project.cshrc
rehash
```

2. **Source the** `user.cshrc` **file by typing:**

   ```
   % source user.cshrc
   ```

Creation of the RTL Model

Next, you must create the RTL model by generating the Verilog executables for the Cadence Verilog-XL or Synopsys VCS compiler. Then take the following step:

- **If you use the Synopsys VCS simulator, type:**

  ```
  % makevcs
  ```

  If you use the Cadence Verilog-XL simulator, type:

  ```
  % makeverilog
  ```

  For Verilog-XL, you can change the name of the executable by modifying the `VLOG_NAME` environment variable in the `user.cshrc` file, as described in the previous section.

  For information on the warnings displayed during compilation, see *Appendix A: Warning Messages During Compilation* on page 9.

Simulation

Before running the simulation, do the following:

1. **Create a directory to store the results from the simulations.**

   The default is: `$SPARCV8HOME/$PROJECT/log/results`. You must create the directories `SPARCV8HOME/$PROJECT/log` and `SPARCV8HOME/$PROJECT/log/results`.

Note – If you create a different directory, be sure to use that path name for the `RESULTSDIR` environment variable in the `user.cshrc` file.

---

2. **Verify that you have read, write, and execute permissions for the following directories:**
   `$RESULTSDIR`
   `$SPARCV8HOME/$PROJECT/diag/bin`

3. **Run the diagnostics, as follows.**

   The complete set of diagnostics (`all.eagle.vcs` and `all.eagle.xl` for Synopsys VCS and Cadence Verilog-XL, respectively) are in the directory `$SPARCV8HOME/$PROJECT/env/regress/script/rtl/edo`. Run the scripts that contain the diagnostic run commands.

   For starters, we recommend that you run the scripts `rtl_mini_regression` and `rtl_mini_regression.verilog_xl`, which are two scripts for running a subset of the diagnostics, `rtl_mini_regression` (for Synopsys VCS) and `rtl_mini_regression.verilog_xl` (for Cadence Verilog-XL). These scripts are located at `$SPARCV8HOME/$PROJECT/env/regress/script`.

   For example:

   - To run a diagnostic with Synopsys VCS, type:

```
% run -simm32 -vcsmodel $SIMV_PATH/simv -S -asm2ver datapath_virt \
tlb32_rst
```

   - To run a diagnostic with Cadence Verilog-XL, type:

```
% run -simm32 -S -asm2ver datapath_virt tlb32_rst
```

4. **Execute the command:**

   `% compile_summary` *summary-filename*

   For example:

```
% compile_summary verilog_xl_summary
```

summary-filename is the file that stores the summary of the simulation runs and resides in the $RESULTSDIR directory. It provides a synopsis of the vectors that have passed or failed. TABLE 2 lists the notations used in summary files.

TABLE 2 Notations In Summary Files

Notation	Description
S	Simulation errors from Verilog
M	Memory miscompares
R	Register miscompares
F	Floating point miscompares
V	Sparse memory miscompares
RDW	N = Not used + = Warning messages present * = Differences in the sas_verilog.dif file
PASF	Diagnostics complete, but with expected error messages, memory miscompares, or register miscompares

Appendix A: Warning Messages During Compilation

Following is a list of some of the warning messages generated by the Synopsys VCS and Cadence Verilog-XL compilers. You can ignore them because the compilation proceeds despite these warnings.

From the Synopsys VCS Compiler

The Synopsys VCS compiler generates the following warning messages.

```
Warning: system function $dist_normal is not implemented (../
../../sparc_v8/env/rtl/task.v line 1164)

Warning: system function $dist_normal is not implemented (../
../../sparc_v8/env/rtl/task.v line 1177)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/mmu/rtl/mmu.v line 1011)
recompiling module fpufpc
recompiling module fpusas_sig

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/rtl/fpusas_sig.v line 107)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/rtl/fpusas_sig.v line 110)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/rtl/fpusas_sig.v line 127)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/rtl/fpusas_sig.v line 132)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/rtl/fpusas_sig.v line 135)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/rtl/fpusas_sig.v line 207)
```

```
Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_ctl/rtl/microcoderom.v line 49)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 185)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 191)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 207)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 232)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 237)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 244)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 247)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 252)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 270)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 294)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 297)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 300)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 303)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 316)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 491)
```

```
Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 536)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 544)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fhold_ctl.v line 548)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/fp_qst.v line 198)
recompiling module qcore_ctl

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 147)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 150)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 268)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 271)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 274)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 327)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 330)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 333)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 344)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 385)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 388)
```

```
Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 391)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 427)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 430)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 433)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 472)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 475)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 478)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 547)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 550)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 553)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 808)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 834)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 842)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 844)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 846)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 848)
```

```
Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/qcore_ctl.v line 858)
recompiling module rfrw_ctl

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/rfrw_ctl.v line 99)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/rfrw_ctl.v line 192)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/rfrw_ctl.v line 197)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/rfrw_ctl.v line 205)
recompiling module stat_ctl

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/stat_ctl.v line 113)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/stat_ctl.v line 116)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/stat_ctl.v line 176)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/stat_ctl.v line 178)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/stat_ctl.v line 180)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/stat_ctl.v line 183)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/stat_ctl.v line 184)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/stat_ctl.v line 206)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpc/rtl/stat_ctl.v line 229)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/carry51.v line 64)
```

```
Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/carry51.v line 77)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/fpm_exp.v line 117)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/fpm_exp.v line 122)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/fpm_exp.v line 127)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/fpm_exp.v line 225)
recompiling module fpm_frac

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/fpm_frac.v line 134)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/fpm_frac.v line 140)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/fpm_frac.v line 146)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/fpm_frac.v line 222)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/fpm_frac.v line 343)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/sign.v line 59)
recompiling module special
recompiling module sticky

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/sticky.v line 64)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/fpu/fp_fpm/rtl/sticky.v line 69)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/mmu/m_mmu_cntl/rtl/m_mmu_cntl.v line
1448)
```

```
Warning: Too few module port connections
(../../../sparc_v8/ssparc/mmu/m_mmu_cntl/rtl/rl_mmu_lgc.v line
1443)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/clkbuf/rtl/clkbuf_c.v line 121)
recompiling module ssparc_chip

Warning: Too few module port connections
(../../../sparc_v8/ssparc/rtl/ssparc.v line 591)
recompiling module ssparc_core

Warning: Too few module port connections
(../../../sparc_v8/ssparc/rtl/ssparc_core.v line 523)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/rtl/ssparc_core.v line 1019)
recompiling module misc

Warning: Too few module port connections
(../../../sparc_v8/ssparc/clk_misc/misc/rtl/misc.v line 251)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/clk_misc/misc/rtl/misc.v line 259)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/clk_misc/rl_jtag_cntl/rtl/
jtag_subblocks.v line 899)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/afxmaster/rtl/afxmaster.v line
1206)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/pci_core/rtl/pci_core.v line 751)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/pci_core/rtl/pci_core.v line 826)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/pci_core/rtl/pci_core.v line
1118)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/pci_core/rtl/pci_core.v line
1272)
```

```
Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/pci_core/rtl/pci_core.v line
1290)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/pci_core/rtl/pci_core.v line
1369)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/pci_core/rtl/pci_core.v line
1394)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/pci_core/rtl/pci_core.v line
1421)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/rtl/pcic.v line 684)

Warning: Too few module port connections
(../../../sparc_v8/ssparc/pcic/rtl/pcic.v line 1003)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/cells.v line 305)
recompiling module MflipflopR

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/cells.v line 322)
recompiling module Mflipflop_noop

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/cells.v line 481)
recompiling module Mflipflop_r

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/cells.v line 450)
recompiling module Mflipflop_rh

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/cells.v line 394)
recompiling module Mflipflop_s

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/cells.v line 433)
recompiling module Mflipflop_sh
```

```
Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/cells.v line 376)
recompiling module Mflipflop_sr

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/cells.v line 413)
recompiling module Mflipflop_srh

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/cells.v line 345)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/cells.v line 467)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 1852)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 1864)
recompiling module con1
recompiling module dual_adder13

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 1766)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 1774)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2179)
recompiling module FDREG_1Byte

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2186)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2187)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2188)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2189)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2190)
```

```
Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2191)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2192)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2193)
recompiling module FREG_1Bit

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2199)
recompiling module FREG_1Byte

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2206)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2207)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2208)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2209)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2210)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2211)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2212)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2213)
recompiling module ME_BUF_C
recompiling module ME_NOR2_D
recompiling module FREG_2bit

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/me_cells.v line 2554)
```

```
Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/BSCN.v line 584)
816 of 853 modules done
recompiling module MEM_BI

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/BSCN.v line 320)
recompiling module MEM_BI_NS

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/BSCN.v line 604)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/BSCN.v line 474)

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/BSCN.v line 483)
recompiling module MEM_OUT_NS

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/BSCN.v line 664)
recompiling module PCI_BI

Warning: Too few module port connections
(../../../sparc_v8/lib/rtl/BSCN.v line 203)
```

From the Cadence Verilog-XL Compiler

The Cadence Verilog-XL compiler generates the following warning message:

```
"/import/seagle-rgrA/cadence/project/soleil/sparc_v8/tools/
verilog/scanlink/pli/ipp.c", line 50: warning: assignment type
mismatch:
pointer to struct ipp_struct {pointer to function() returning
int accept, pointer to function() returning int close,
pointer... "=" pointer to char
```

Appendix B: Error and Warning Messages During Simulation

Following is a list of some of the error and warning messages generated by the Synopsys VCS and Cadence Verilog-XL simulators. You can ignore them because the simulation proceeds despite these errors and warnings.

From the Synopsys VCS Simulator

The Synopsys VCS simulator generates the following warning messages:

```
Error: DRAM at 0 rasb_l violates tRP(ras precharge time

Error: DRAM at 0 tCSR(cas setup time(w.r.t rasb_l), CBR
refresh) violated
(rasb_low_cycle - cas_low_cycle) == 0

Error: DRAM at 0 rasb_l violates tRP(ras precharge time

Error: DRAM at 0 tCSR(cas setup time(w.r.t rasb_l), CBR
refresh) violated
(rasb_low_cycle - cas_low_cycle) == 0

Error: DRAM at 0 rasb_l violates tRP(ras precharge time

Error: DRAM at 0 tCSR(cas setup time(w.r.t rasb_l), CBR
refresh) violated
(rasb_low_cycle - cas_low_cycle) == 0

Error: DRAM at 0 rast_l violates tRP(ras precharge time

Error: DRAM at 0 tCSR(cas setup time(w.r.t rast_l), CBR
refresh) violated

Error: DRAM at 0 tCSR(cas setup time(w.r.t rast_l), CBR
refresh) violated

Error: DRAM at 0 tCSR(cas setup time(w.r.t rast_l), CBR
refresh) violated
```

```
Error: DRAM at 0 tCSR(cas setup time(w.r.t rast_l), CBR
refresh) violated

"Cannot open COMMAND file pcislave_tst.cmd. No commands are
preloaded!"

WARNING at 0 from
Msystem.lmc_slave1.fm.get_addr_tbl_elmnt.loop_get
"GET_ADDR_TBL_ELMNT: main not found in table"
"Illegal function call, function main not declared"
"Cannot open data file pcislave_tst.io. No data is preloaded!"
"Cannot open data file pcislave_tst.cfg. No data is preloaded!"

Note at time 0 from Msystem.lmc_slave1.fm.report_slave
"SYNOPSYS PCISLAVE MODEL 5.3

WARNING at time 0 from Msystem.lmc_master1.fm.exe_call
"Cannot open COMMAND file lmc_master1.cmd. No commands are
preloaded!"

WARNING at 0 from
Msystem.lmc_master1.fm.get_addr_tbl_elmnt.loop_get
"GET_ADDR_TBL_ELMNT: main not found in table"

WARNING at 0 from Msystem.lmc_master1.fm.exe_call
"Illegal function call, function main not declared"

Setup sparse mem model for ravi slave memory

Setup sparse mem model for ravi slave io

afx_slave: setting read/write latencies to 0

 INFO: standby mode == 0

WARNING at time 3100 from Msystem.lmc_master1.fm.pclk_check
"Unknown value on pin pclk will be ignored"

WARNING at time 3100 from Msystem.u1.fm.clk_check
"Unknown value on pin clk will be ignored"
```

From the Cadence Verilog-XL Simulator

The Cadence Verilog-XL simulator generates the following warning messages:

```
Compiling source file "/import/seagle-rgrA/cadence/project/
soleil/sparc_v8/system/rtl/memif_defs.h"

Warning! Text macro (RD) redefined -
replaced with new definition [Verilog-TMREN]
"/import/seagle-rgrA/cadence/project/soleil/sparc
_v8/system/rtl/memif_defs.h", 300:

Warning! Text macro (lmv_timescale) redefined -
replaced with new definition [Verilog-TMREN]
"/import/seagle-rgrA/cadence/project/soleil/sparc_v8/system/lmc/
rtl/lmc_8.v", 83:

Warning! Text macro (time_scale_multiplier) redefined -
replaced with new definition [Verilog-TMREN]
"/import/seagle-rgrA/cadence/project/soleil/sparc_v8/system/lmc/
rtl/lmc_8.v", 84:

Warning! Text macro (TRUE) redefined -
replaced with new definition [Verilog-TMREN]
"/import/seagle-rgrA/cadence/project/soleil/sparc_v8/system/lmc/
rtl/lmc_8.v", 92:

Warning! Text macro (FALSE) redefined -
replaced with new definition [Verilog-TMREN]
"/import/seagle-rgrA/cadence/project/soleil/sparc_v8/system/lmc/
rtl/lmc_8.v", 94:
"Cannot open data file pcislave_tst.io. No data is preloaded!"
"Cannot open data file pcislave_tst.cfg. No data is preloaded!"
"Cannot open COMMAND file pcislave_tst.cmd. No commands are
preloaded!"

WARNING at 0 from
Msystem.lmc_slave1.fm.get_addr_tbl_elmnt.loop_get
"GET_ADDR_TBL_ELMNT: main not found in table"
"Illegal function call, function main not declared"
Note at time 0 from Msystem.lmc_slave1.fm.report_slave

WARNING at time 0 from Msystem.lmc_master1.fm.exe_call
"Cannot open COMMAND file lmc_master1.cmd. No commands are
preloaded!"
```

```
WARNING at 0 from
Msystem.lmc_master1.fm.get_addr_tbl_elmnt.loop_get
"GET_ADDR_TBL_ELMNT: main not found in table"

WARNING at 0 from Msystem.lmc_master1.fm.exe_call
"Illegal function call, function main not declared"

WARNING at time 3100 from Msystem.u1.fm.clk_check
"Unknown value on pin clk will be ignored"

WARNING at time 3100 from Msystem.lmc_master1.fm.pclk_check
"Unknown value on pin pclk will be ignored"

Warning! Text macro (ssparc_chip_file) redefined -
replaced with new definition [Verilog-TMREN]
"sparc_v8/system/rtl/ssparc_chiplsidump.v", 35:
```