

Challenges and Design Solutions to Upgrade Existing Systems for Higher Bandwidth (Part 1)

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Upgrading vs Replacing

Reuse Existing Infrastructure
Shorter Schedule
Lower Development Cost
Higher Performance
Feature Enhancements



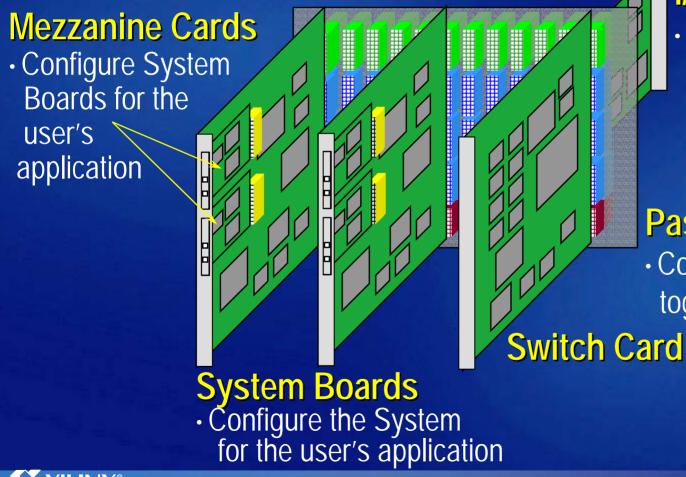


Upgrading A System

 Many Aspects to Consider for System Upgrade -Power budget -Thermal environment -Other functional upgrades Focus on the System I/O to Improve Data Bandwidth Serial Backplane Case Study Example



A Typical Backplane System



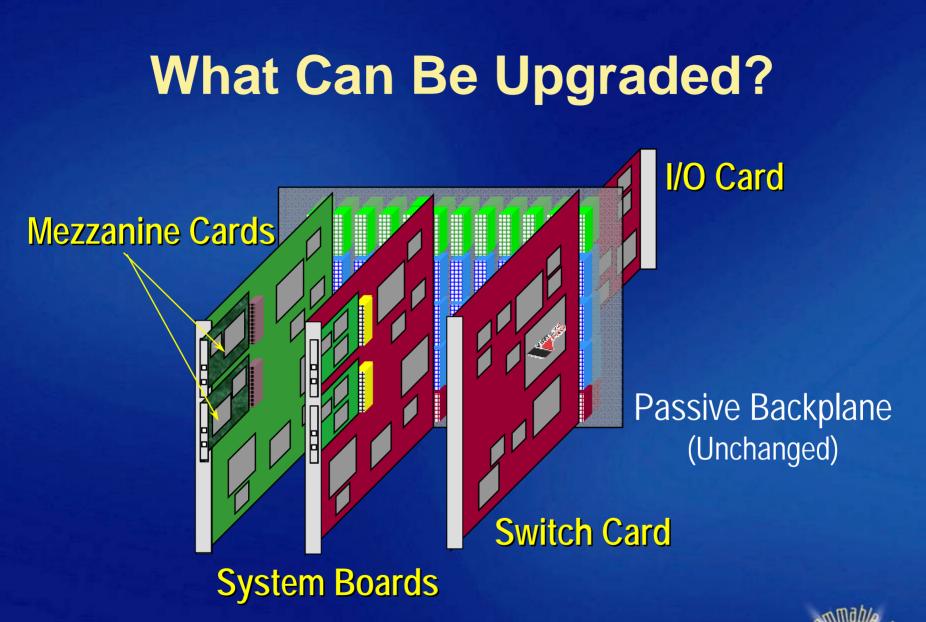
I/O Cards

 Configure system connections to the rest of the world

 Passive Backplane
 Connect everything together



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Challenges

- New Silicon Technology with Existing Connectors and Backplanes
- Signal Integrity and Attenuation Issues
 - Jitter, skin effect, dielectric losses
- Diagnostic Testing and Characterization
 - Interoperability testing
 - Bit-error rate measurements
- Serial Protocol Selection





Solving the Challenges Characterization and Prototyping - Determine overall system signal integrity and margin System Design Aspects -I/O performance tuning -Serial Protocol Selection Simulation is Recommended -HSPICE, S-parameter simulation



Characterization & Prototyping

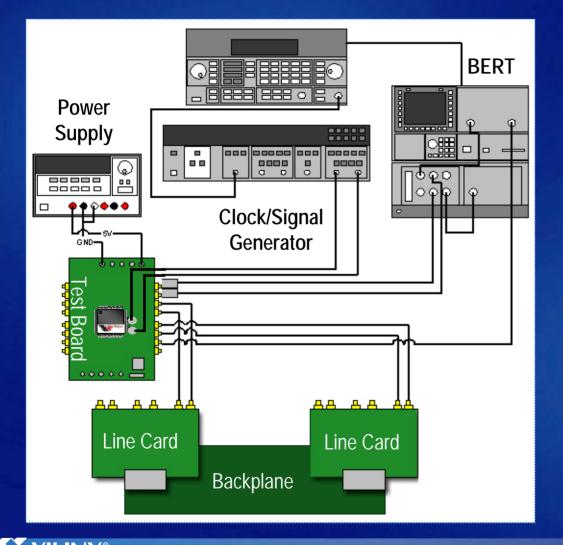
- Backplane Characterization Techniques
 - Eye diagrams height and width
 - Deterministic and random jitter
 - Channel Bit Error Rate (BER)
 - Channel loss with S-parameters using a Vector Network Analyzer (VNA)
 - Channel discontinuities using a Time Domain Reflectometer (TDR)

Validate Simulation with Hardware





Backplane Test Setup



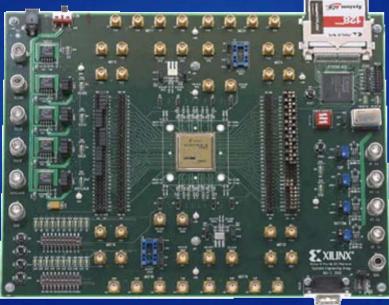
 Test Board Transmits and Receives Across Backplane

 Loopback within the Characterization Board





Example HW Characterization Platforms

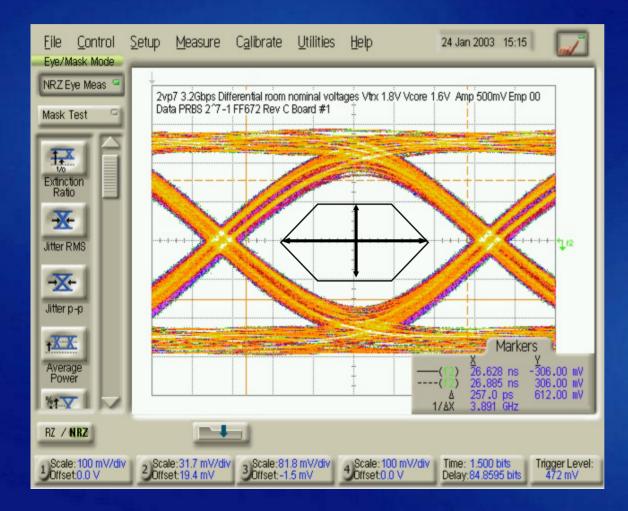


- Microstrip Board
- Allows Additional FR4 Trace Length to Be Added to RocketIO Signals
- 10", 15", 20", 30", or 40" FR4 Microstrip Lines

- ML321 Characterization Board
- Target device = XC2VP7 with 8 RocketIO[™] Serial Transceivers
- On-board Oscillator or External Clock Source Options
- 8 mil Width / 10 mil Spacing Microstrip (Buried Trace) Lines
- 100 Ohms Differential Termination



Eye Diagram with Mask

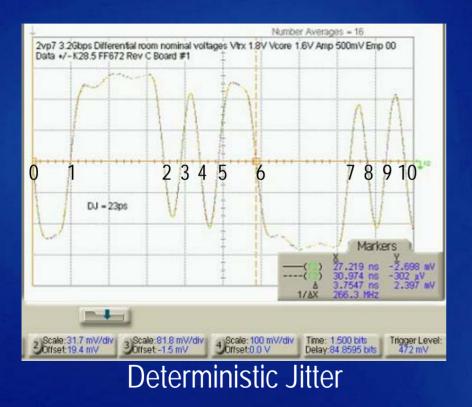


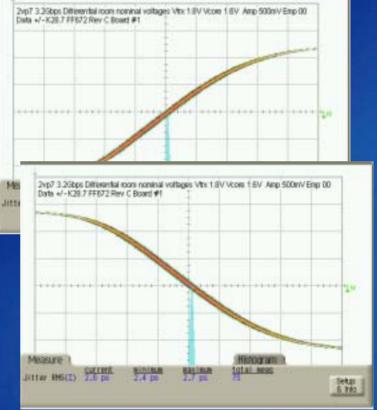
• Eye Width Data valid time Eye Height - Differential voltage • Eye Mask Defined by specific standard





System Jitter





Characteristics of Your Physical System

XILINX[®]

K28.5 & K28.7 are common test patterns

Random Jitter

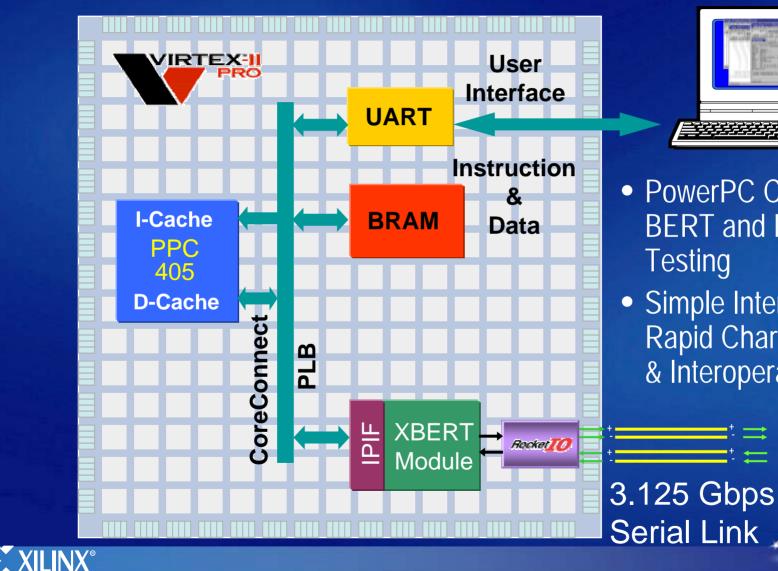


Bit Error Rate Test (BERT)

 Used to Verify Serial Links Integrity and **Compliance to Standard Specifications** In Its Most Simplistic Form - BER = Dropped frames/ Total frames In the Real World, BER is Calculated as a Statistical Estimate of the True Bit Error Rate Pseudo Random Binary Sequence (PRBS) - Typically used as a test signal when making BER measurements



Xilinx On-Chip BERT Design





- PowerPC Controls **BERT and PRBS** Testing
- Simple Interface for **Rapid Characterization** & Interoperability Tests

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System Distance Dilemma

Example A: Short Trace

Example B: Long Trace

Signal Attenuation & Jitter are Functions of Trace Length

Transmitter Settings Can be Adjusted for Slot Location Within **Backplane for Optimal Performance**

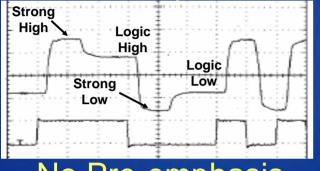




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Pre-emphasis for Signal Integrity

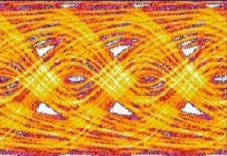
Pre-emphasis



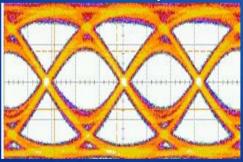
No Pre-emphasis

- Pre-emphasis Increases Drive of Transmitter Briefly
- Compensates for Frequency Dependent Loss in the Transmission Media
- Decreases Deterministic Jitter (DJ) at Receiver

10% Pre-emphasis



33% Pre-emphasis



After 44" of FR4 Backplane (3.125 Gbps)



Xilinx Adaptive I/O Solution

• Enhanced Diagnostic Testing

- Integrated with XBERT reference design
- Rapid Prototyping
 - Terminal interface for command line control of diagnostic testing and MGT transmitter settings without requiring FPGA reconfiguration
- In System RocketIO[™] Attribute Setting
 - MGT attributes can be automatically set depending on backplane slot location, accommodating differences in transmission length





Serial Protocols Supported

LAN/MAN/WAN

10/100 Ethernet (MII) 1Gb Ethernet(GMII) 10Gb Ethernet(XGMII) PCI-X 100 1Gb Ethernet (1000 Base-X) 10Gb Ethernet (XAUI) OC48* OC192* OC768*

Board-to-Board/Backplane

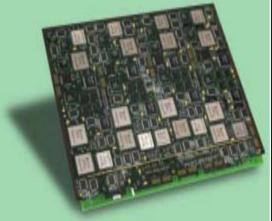
PCI 32/33 RapidIO[™] PCI 64/66 \bigcirc CSIX HyperTransport ■ RapidIO Ser. InfiniBand™ Fibre chan. ○ PCI Express™ 10GE(XAUI) 🥥 Aurora SONET*





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Serial Standards – enabled by RocketIO[™] technology Parallel Standards – enabled by SelectIOTM-Ultra technology

* SONET compatible, supports data rate

http://www.xilinx.com/connectivity



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Simulation to H/W Correlation

- MGT SPICE Models are Provided by IC Vendors
- SPICE Connector Models Can be Difficult to Use
- Lossy Coupled Transmission Lines
 - Modeling requires the use of matrices generated by a field solver and a frequency-dependent simulation methodology
 - "W element" modeling is commonly used to simulate coupled transmission lines with loss
 - S-parameter modeling can be more accurate

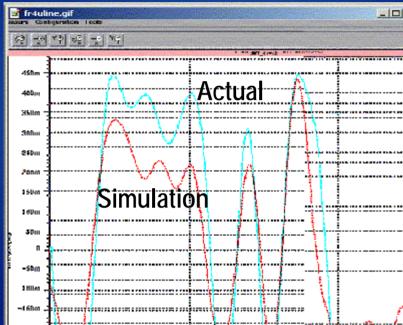


W-Element vs S-Parameters Simulation

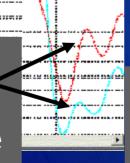
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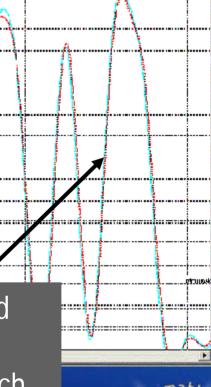
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Significant Difference Between the Simulation Data and Actual Hardware Measurements



Simulation Data and Actual Hardware Measurements Match



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Serial Design Resources

Dedicated Web Portal - http://www.xilinx.com/serialsolution

🐺 Xilinx Home : Products & Services - Netscape			
Elle Edit Yew Go Communicator Help 🛷 and			
Back Prove Real Coupons WebLINK SPW P Vacation map Groups MyVahood Trademar			
E XILINX"	Products		
HOME PRODUCTS & SERVICES END MARKETS SUPPORT EDUCATION ONLINE STORE CONTACT) I Silicon Solutions Design Resources System Resources Literature Home : Products & Services			
Entire Site	Products and Services Weekly Highlight		
Search Advanced Products Guide Product Datasheets	Visit our dedicated Serial Tsunami web portal for a one-stop shop on the latest design resources to enable your next serial design with serial technology.		
Application Notes	-		
Partnerships	○ Rockett0 [™] Serial I/O Technology	Intellectual Property Cores	
Reference Design Alliance Program	The RockettO multi-gigabit transceivers offer very high performance and complete functionality to enable multi-gigabit serial connectivity between boards,	Xilinchas IP cores for serial UO standards such as PCI Express, <u>Oisabit Ethernel</u> and <u>10 Oigabit</u> Ethernet ISE Design Tools include logic design	
AllianceEDA			
AllianceCORE	 Rocketto Demonstration Video Rocketto Flash Movie 	POExpress x1 Core Opened Efformet	
XPERTS Silicon Products	 10 Gbps Technology 	 10.0ioolult Ethernet XAU 	
Silicon Products	Learn More	Learn More	
	Signal Ingegrity/PC Board Design	Reference Designs	
	Signal integrity reduces the chance of data or signal comption and prevents enoneous data processing.	Xilmx offers a number of reference designs in the form of application notes with supporting design files. These designs represent good starting points for implementing simple to complex functions in Xilmx programmable logic.	
	SELCE Suite POB Decion Guidelines Usinge Models for MGTs	Solutions for BONET Backplanes Autora Protocol and Reference Designs Adaptive I/O Solution for befler signal integrity	
all 🕪 Document: Done			

• IP/ Ref. Designs RocketlO Data - Characterization – User Guide - SPICE suite PCB Design/Signal Integrity Tools HW Evaluation **Platforms** Partner Solutions Technical Training Design Services

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Conclusion

- Upgrading is Challenging but Achievable
- Upgrading Achieves Higher System Performance at Lower Cost in a Shorter Time
- FPGAs Offer Flexible and Cost Effective Solutions
- Xilinx Has Design Resources to Ensure Your Success





References

- Adaptive I/O Solution Three Reference Designs
 - http://www.xilinx.com/xapps/xapp660.pdf
 - http://www.xilinx.com/xapps/xapp661.pdf
 - http://www.xilinx.com/xapps/xapp662.pdf
- Aurora Open Protocol
 - http://www.xilinx.com/aurora
- Serial Design Resources (http://www.xilinx.com/serialsolution)
 - RocketIO User Guide
 - RocketIO Characterization Report
 - RocketIO ML321 characterization board
 - Serial IP & reference designs
 - RocketIO training class





Thank You!

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TEXAS INSTRUMENTS

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WIND RIVER

CMP