

Challenges and Design Solutions to Upgrade Existing Systems for Higher Bandwidth (Part 2)

Agenda

- Major design-in challenges
- Why simulate?
- Enabling design collaboration

Design-in of Complex IC's is Tougher than Ever

Silicon



Package



onto

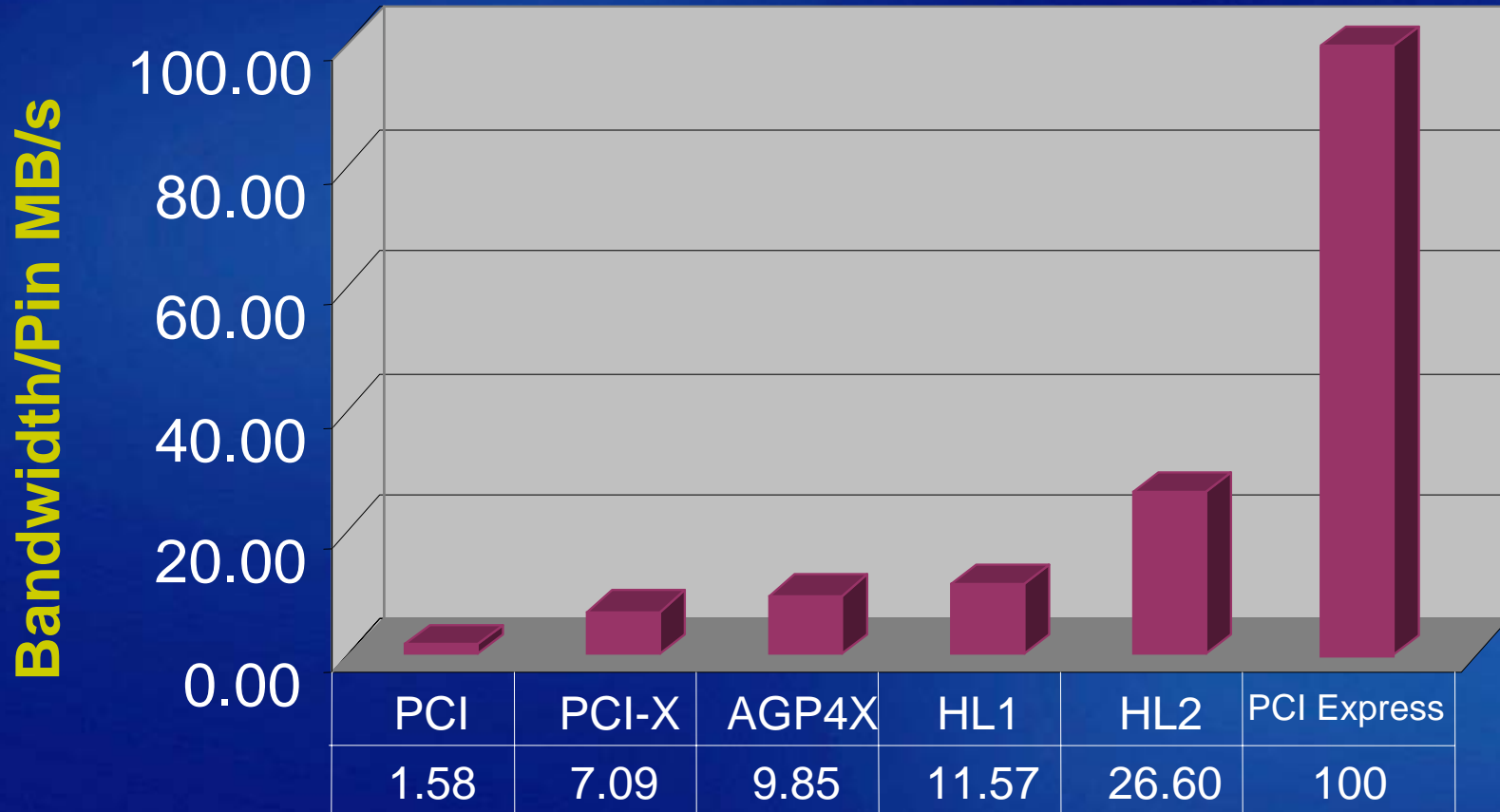
Board



into

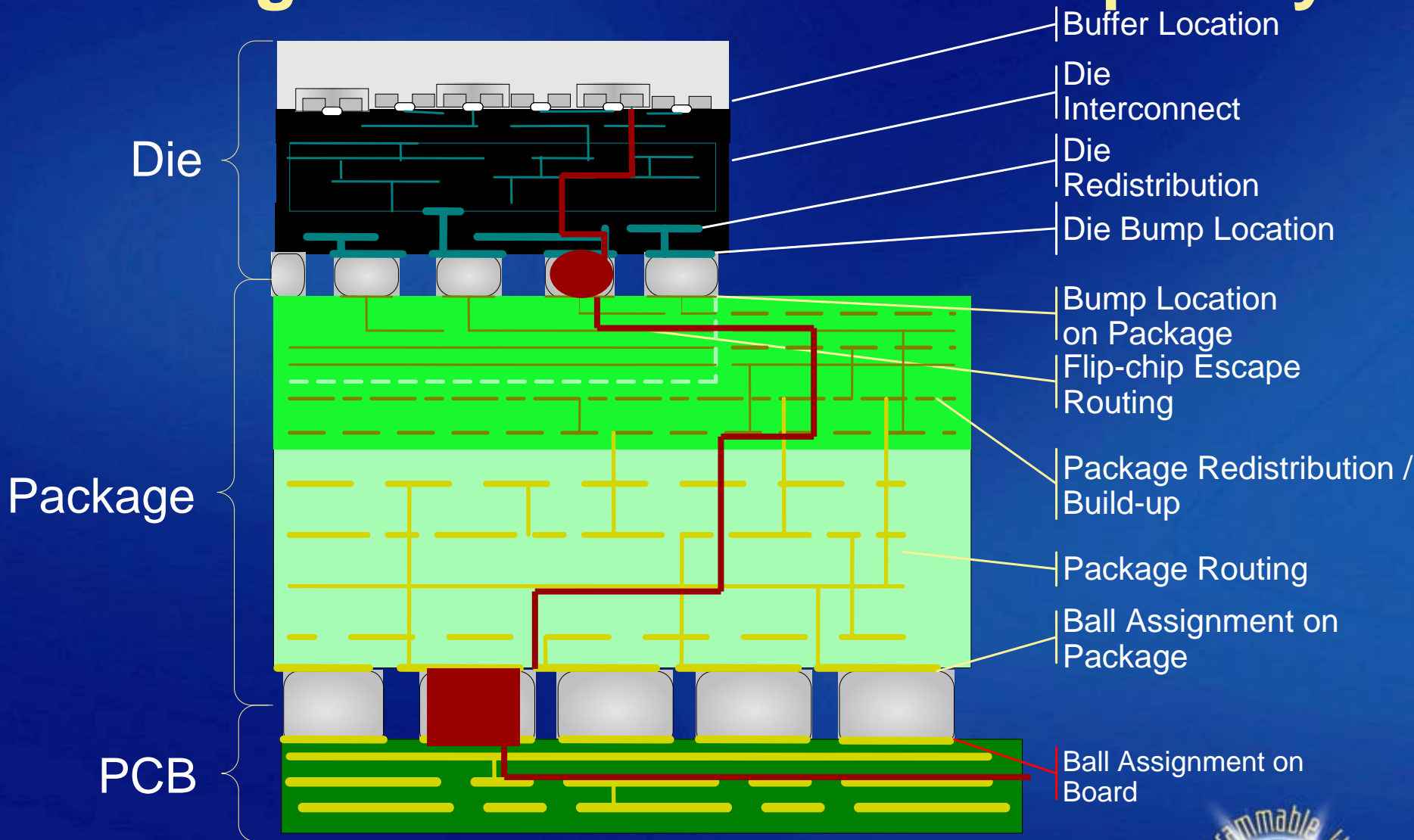
To
Volume

Increasing Bandwidth/pin Efficiency

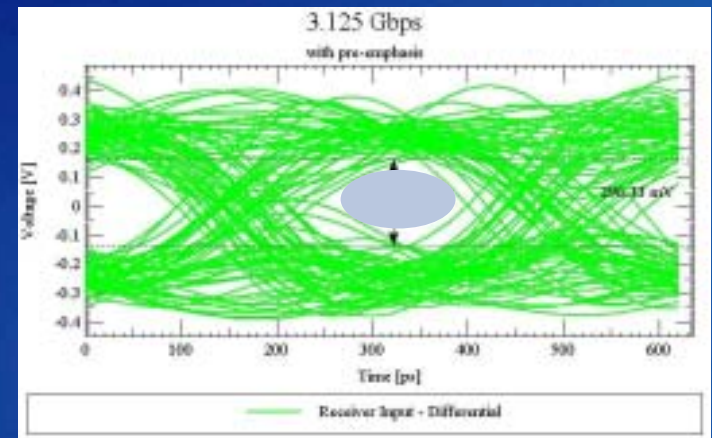
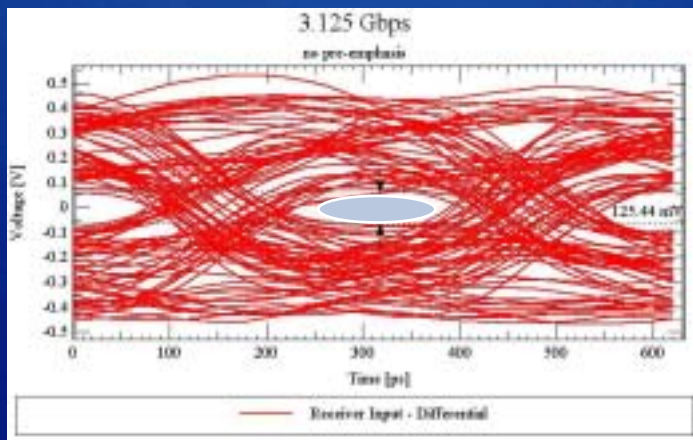
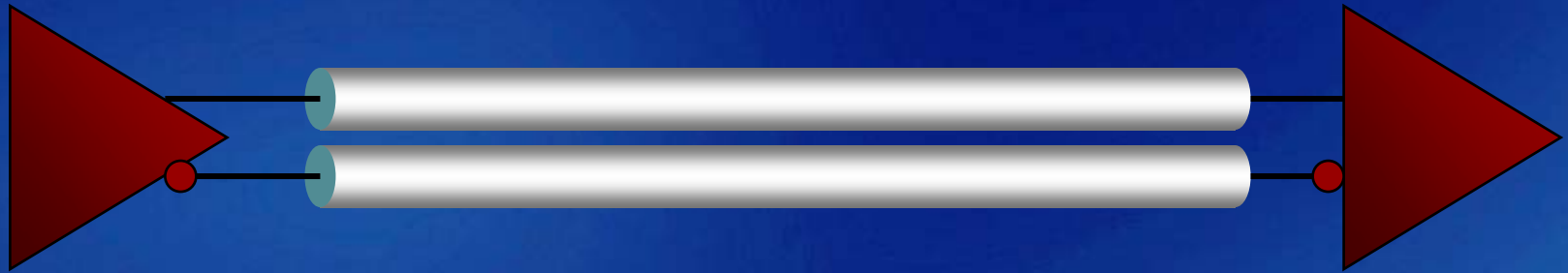


Source: Intel PCI Express Overview
Pins include all signals + VCC/GND

Dealing with Interconnect Complexity

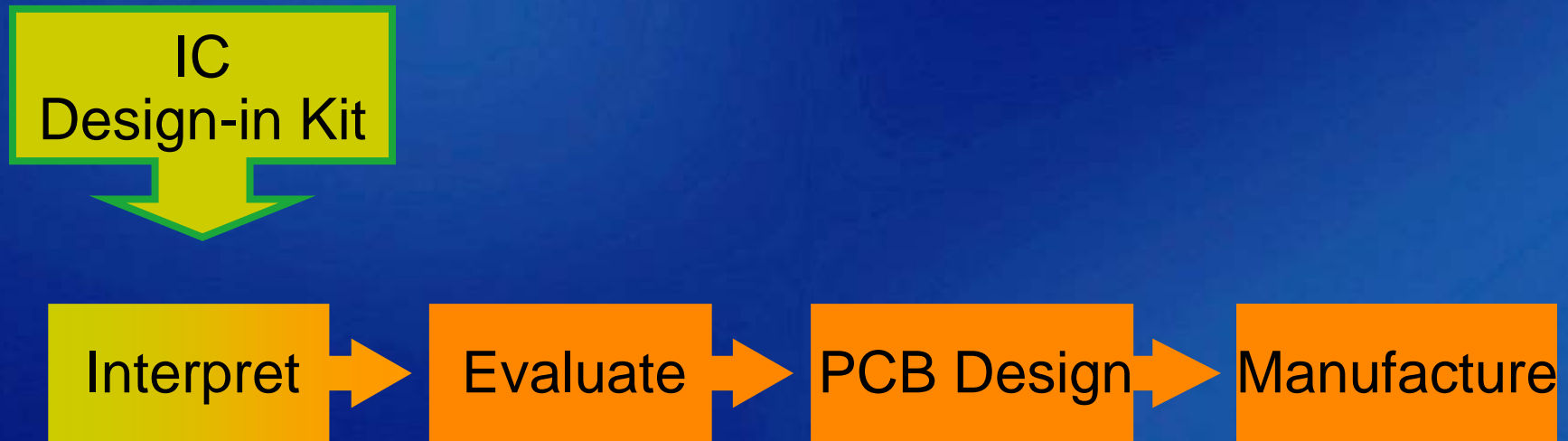


Simulation is Critical for High-Speed Design



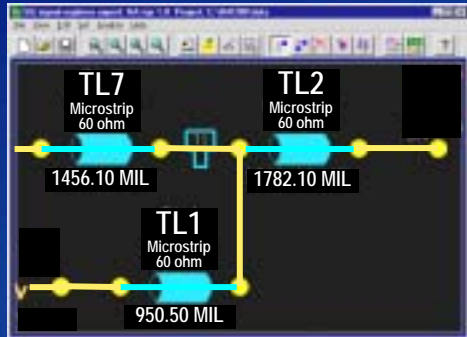
But setting up for simulation can be time consuming...

Design-in Kits Accelerate Design Start Time

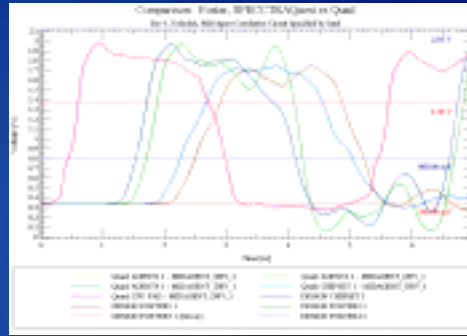


Save weeks or months off your design cycle

Design Kit Contents



**Simulation
Setup**



**Correlation
Data**



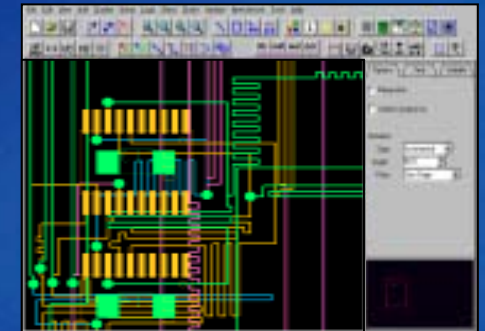
Schematics

Constraint	Value	Unit	Status
TL1 Length	950.50	MIL	OK
TL2 Length	1782.10	MIL	OK
TL7 Length	1456.10	MIL	OK
TL1 Impedance	60	ohm	OK
TL2 Impedance	60	ohm	OK
TL7 Impedance	60	ohm	OK

Constraints



**Tutorials
Utilities
Web page**



PCB Layout

Ready to simulate in minutes

High-speed PCB Systems Design

Design-in
Kit

EXPLORATION

CONSTRAIN &
FLOORPLAN

CONSTRAINT
DRIVEN LAYOUT

VERIFICATION



High-speed PCB Systems Design

Design-in
Kit

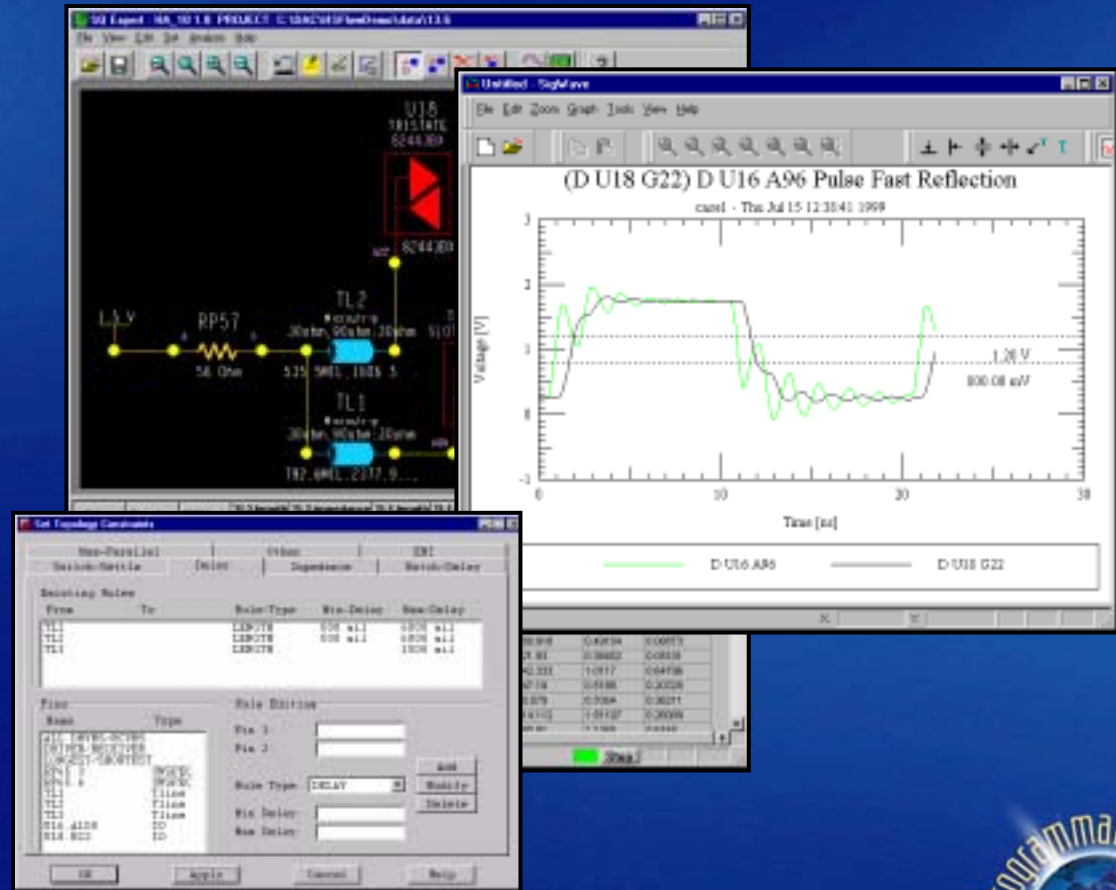
Models, topologies, stimulus,
Custom measurements

EXPLORATION

CONSTRAIN &
FLOORPLAN

CONSTRAINT
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VERIFICATION



High-speed PCB Systems Design

Design-in
Kit



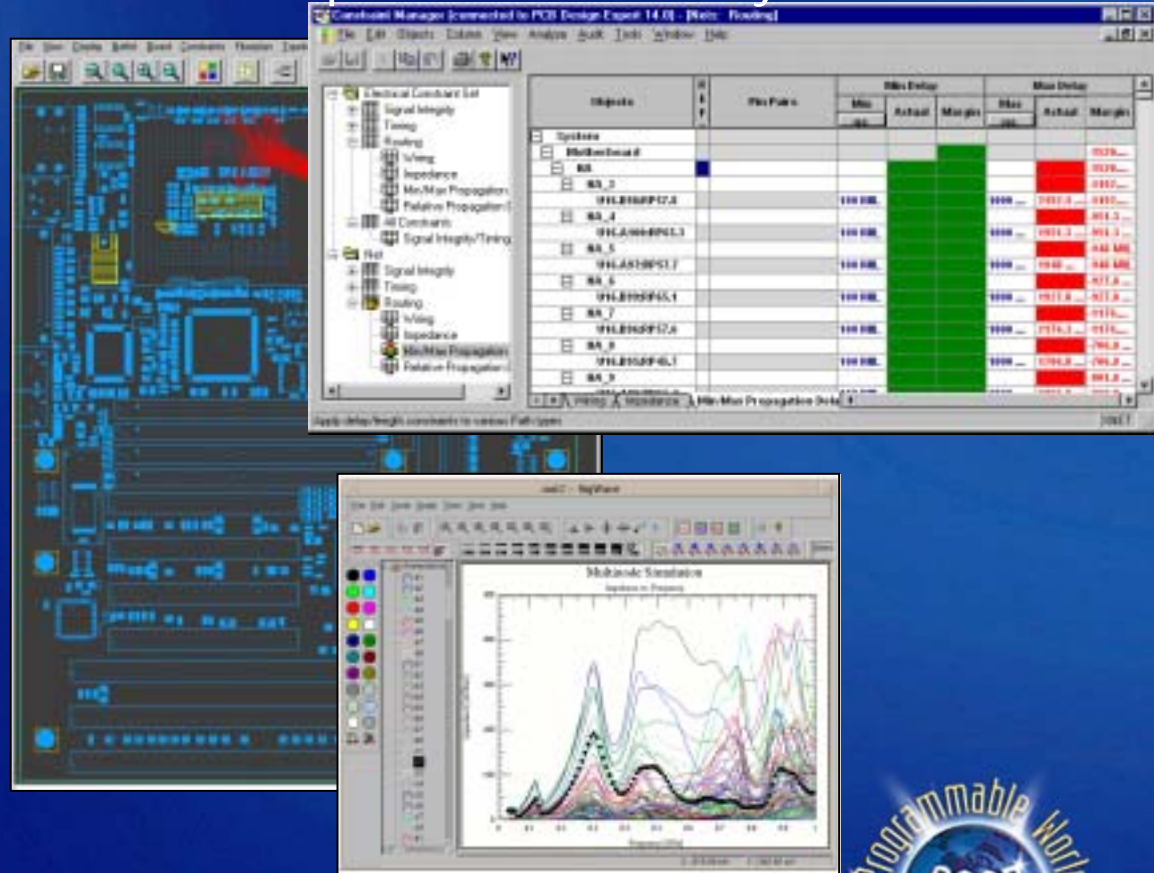
Pre-defined rules
Example schematic & layout

EXPLORATION

CONSTRAIN &
FLOORPLAN

CONSTRAINT
DRIVEN LAYOUT

VERIFICATION



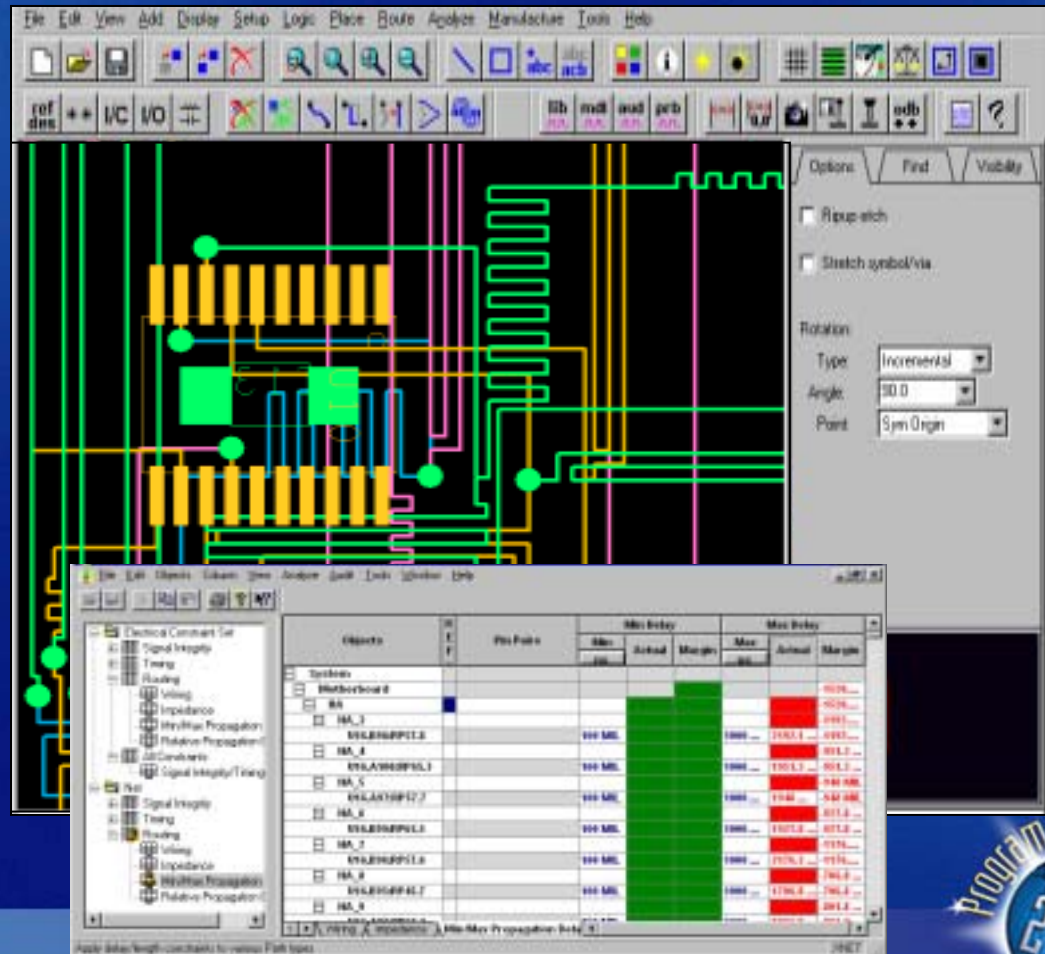
A diagram illustrating the flow from a Design-in Kit to a Design-out Kit. On the left, a teal cylinder labeled "Design-in Kit" is connected by a thick red arrow pointing to a teal cylinder on the right labeled "Design-out Kit".

EXPLORATION

CONSTRAIN & FLOORPLAN

CONSTRAINT DRIVEN LAYOUT

VERIFICATION



High-speed PCB Systems Design

Design-in
Kit

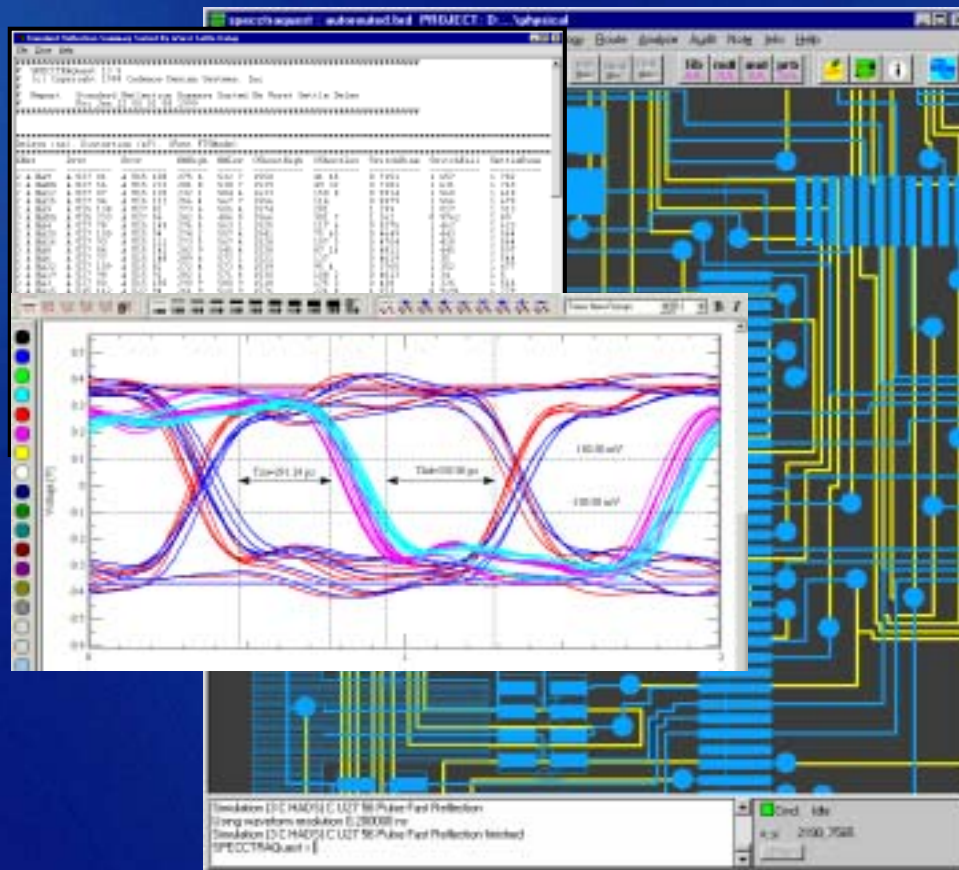
Component models
Post-processing utilities

EXPLORATION

CONSTRAIN &
FLOORPLAN

CONSTRAINT
DRIVEN LAYOUT

VERIFICATION



Design-in Kits Available Now



The screenshot shows the Xilinx website's 'Products' section. The Xilinx logo is in the top left. A navigation bar contains links: HOME, PRODUCTS, END MARKETS, SUPPORT, EDUCATION, ONLINE STORE, CONTACT, and SEARCH. Below this is a secondary navigation bar with links: Silicon Solutions, Design Resources, System Resources, and Literature. The main content area is titled 'RocketIO Design Kit with Cadence SPECCTRAQuest'. It includes a 'What's New Success Stories' sidebar, a 'Related Features' sidebar with links to 'Cadence and Xilinx Alliance Overview', 'SPECCTRAQuest Overview', 'Download the Kit from the SPICE Suite', and 'Xcell Journal Article'. The main text describes the kit as an electronic blueprint for simulating and implementing Virtex-II Pro™ Rocket IO transceivers. It lists the following features:

- Ready-to-simulate system level topologies for typical use of the device on the board/system;
- Verified IO buffer models;
- Large Package Model;
- Test bench data, Correlation data;
- Connector models for backplane applications;
- Device specific scripts/tools to evaluate simulation results;
- A video that describes how to get started with the design kit in the end users environment.

The URL http://www.xilinx.com/ise/alliance/rocketio_kit.htm is displayed at the bottom of the screenshot.



Summary

- Interconnect complexity and increasing speed
- Signal integrity is a mainstream design problem
- Simulation is the only way to first time design success
- Design-in kits get you designing product faster
- What are your IC suppliers doing to enable your product design?

References

- SPECCTRAQuest high-speed design community
 - <http://www.specctraquest.com>
- Cadence Design Chain Optimization Initiative
 - http://www.cadence.com/feature/design_chain.html
- Articles & papers
 - <http://www.specctraquest.com/Contribute/Solutions.asp>
 - http://www.specctraquest.com/downloads/xc_speckit42.pdf
 - http://www.xilinx.com/publications/xcellonline/xcell_45/xc_cadence45.htm
- Webinars & movies
 - <http://www.cadencepcb.com/promotions/designchain/jump.asp>
 - <http://www.specctraquest.com/Optimize/DesignKits.asp>
 - http://www3.vcall.com/digitallava/cadence_alex_rm/audio_rm/main.htm



Programmable World

2003

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Thank You!

Cadence across silicon-package-board

Market Leader

2001 Total Revenue: \$1.43B
2001 Product Revenue: \$830M

Global Business

North America 59%
Europe 21%
Japan/Asia 20%
>58 offices worldwide

Unmatched Resources

Total Employees: 5,600
Engineers: >3,600
2001 R&D investment: ~\$300M



*IEEE Corporate
Innovation Award
Recipient for 2002*



Rank	Company	Rev. # Mil.
1	Microsoft	25,296
2	Oracle	10,860
3	Computer Assoc.	4,198
4	Peoplesoft	2,073
5	Siebel Systems	2,048
6	Compuware	2,010
7	BMC Software	1,504
8	Veritas Software	1,492
9	Cadence Design	1,430
10	Electronic Arts	1,322

