XILINX®

Spartan and Spartan-XL Families of Serial Configuration PROMs

Introduction

The Spartan™ family of Serial Configuration PROMs (SPROM) provides and easy-to-use, cost-effective method for storing Spartan device configuration bitstreams.

When the Spartan device is in Master Serial mode, it generates a configuration clock that drives the Spartan SPROM. A short access time after the rising clock edge, data appears on the SPROM DATA output pin that is connected to the Spartan device DIN pin. The Spartan device generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SPROM. When a Spartan device is in Slave Serial mode, the SPROM and the Spartan device must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all SPROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance or the Foundation series development systems compiles the Spartan device design file into a standard HEX format which is then transferred to most commercial PROM programmers.

Spartan SPROM Features

- Serial Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Spartan FPGA devices
- Simple interface to the Spartan device requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low)
- Low-power CMOS floating gate process
- Available in 5 V and 3.3 V versions
- Available in compact plastic 8-pin DIP, 8-pin VOIC, or 20-pin SOIC (XC17S40 only) packages.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

Spartan FPGA	Compatible Spartan SPROM	Configuration Bits
XCS05	XC17S05	65,536
XCS05XL	XC17S05XL	131,072
XCS10	XC17S10	131,072
XCS10XL	XC17S10XL	131,072
XCS20	XC17S20	262,144
XCS20XL	XC17S20XL	262,144
XCS30	XC17S30	262,144
XCS30XL	XC17S30XL	262,144
XCS40	XC17S40	524,288
XCS40XL	XC17S40XL	524,288

Pin Description

Table 1: Serial PROM Pinouts

Pin Name	8-Pin PDIP & VOIC	20-Pin SOIC	Pin Description
DATA	1	1	Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.
CLK	2	3	Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3	8	When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is 3-stated. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGA's $\overline{INIT}$ pin. The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.
$\overline{CE}$	4	10	When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low-I_{CC} standby mode.
GND	5	11	GND is the ground connection.
$\overline{CEO}$	6	13	Chip Enable output, to be connected to the $\overline{CE}$ input of the next SPROM in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.
V_{CC}	7, 8	18, 20	The V_{CC} pins are to be connected to the positive voltage supply.

Controlling Serial PROMs

Connecting the Spartan device with the SPROM:

- The DATA output of the SPROM drives the DIN input of the lead Spartan device.
- The Master Spartan device CCLK output drives the CLK input of the SPROM.
- The $\overline{\text{RESET}}$/OE input of the SPROM is driven by the $\overline{\text{INIT}}$ output of the Spartan device. This connection assures that the SPROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods – such as driving $\overline{\text{RESET}}$/OE from $\overline{\text{LDC}}$ or system reset – assume that the SPROM internal power-on-reset is always in step with the FPGA's internal power-on-reset, which may not be a safe assumption.
- The $\overline{\text{CE}}$ input of the SPROM is driven by the DONE output of the Spartan device, provided that DONE is not permanently grounded. Otherwise, $\overline{\text{LDC}}$ can be used to drive $\overline{\text{CE}}$, but must then be unconditionally High during user operation. $\overline{\text{CE}}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Look-up table and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the Spartan device MODE pin. In Master Serial mode, the Spartan device automatically loads the configuration program from an external memory. The Spartan SPROM has been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, the Spartan device enters the Master Serial mode when the MODE pin is Low. Data is read from the Serial Configuration PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure the Spartan device. Data from the Serial Configuration PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the Spartan device is used only for configuration, it must still be held at a defined level during normal operation. The Spartan family takes care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple-configurations for a single Spartan device are stored in a Serial Configuration PROM, the $\overline{\text{OE}}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{\text{OE}}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies $\overline{\text{RESET}}$ during the Spartan device configuration process. The Spartan device aborts the configuration and then restarts a new configuration, as intended, but the SPROM does not reset its address counter, since it never saw a High level on its $\overline{\text{OE}}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the Spartan device is the Master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the Spartan device configuration will be completely wrong, with potential contentions inside the Spartan device and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Cascading Serial Configuration PROMs

For multiple Spartan devices configured as a daisy-chain, cascaded SPROMs provide additional memory. After the last bit from the first SPROM is read, the next clock signal to the SPROM asserts its $\overline{\text{CEO}}$ output Low and disables its DATA line. The second SPROM recognizes the Low level on its $\overline{\text{CE}}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded SPROMs are reset if the Spartan device $\overline{\text{RESET}}$ pin goes Low, assuming the SPROM reset polarity option has been inverted.

To reprogram the Spartan device with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.
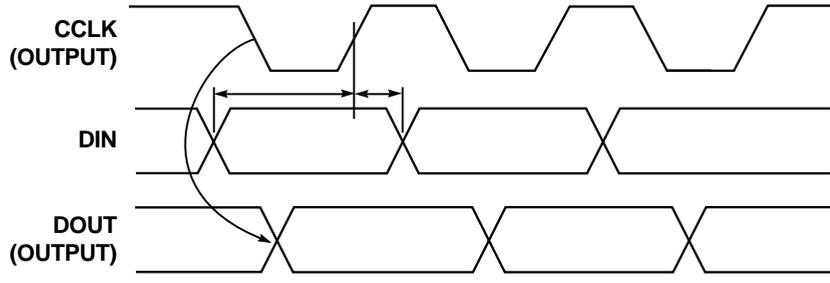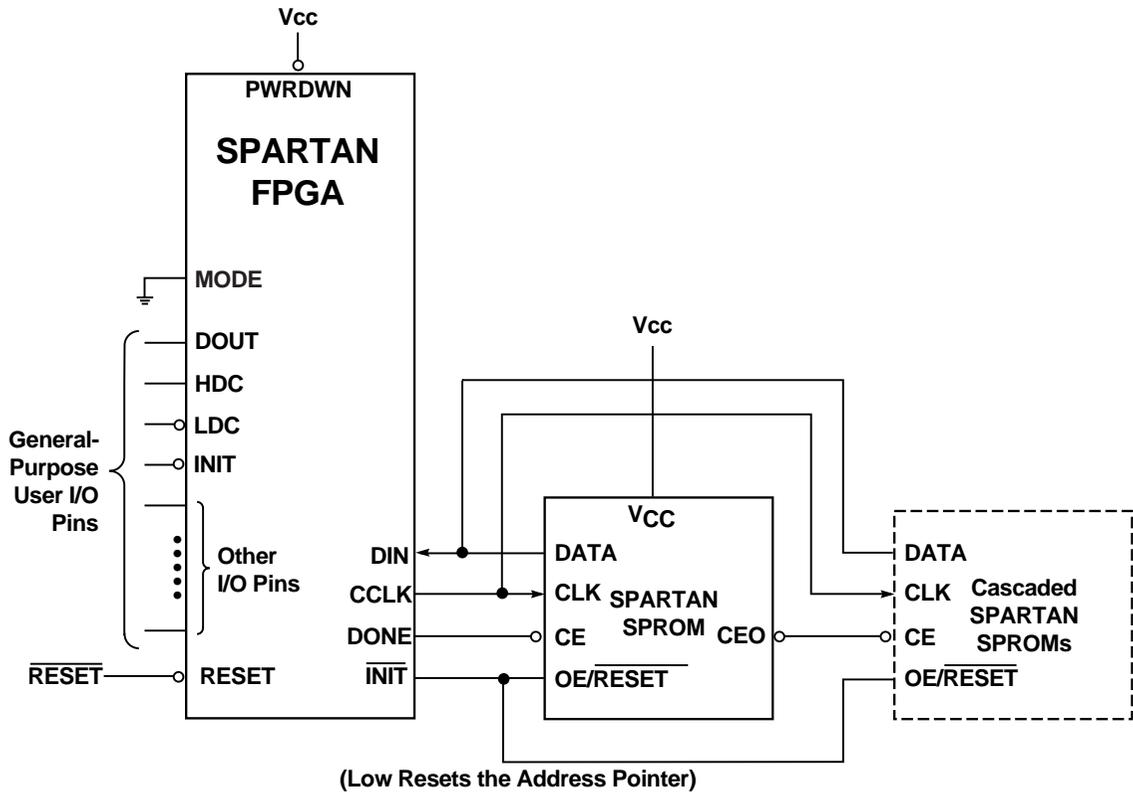
Figure 1: Master Serial Mode. The one-time-programmable Spartan SPROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional Spartan FPGAs. An early DONE inhibits the PROM data output one CCLK cycle before the Spartan FPGA I/Os become active.

Standby Mode

The SPROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Programming the Spartan Family Serial PROMs

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.
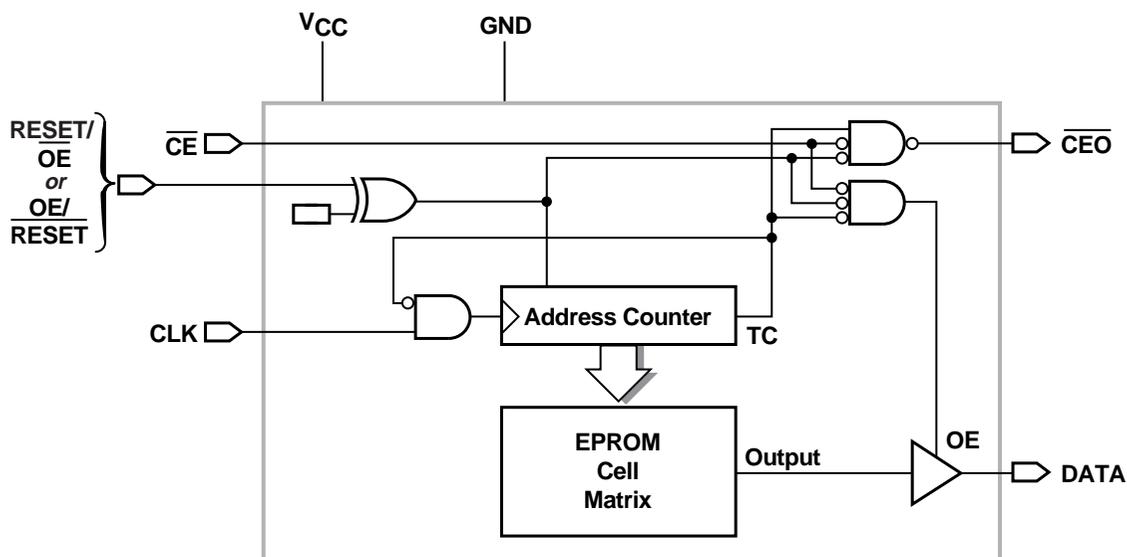
X8473

Figure 2: Simplified Block Diagram (does not show programming circuit)

Important: Always tie the two V_{CC} pins together in your application.

Table 2: Truth Table for XC17S00 Control Inputs

Control Inputs		Internal Address	Outputs		
RESET	**CE**		**DATA**	**CEO**	**I$_{cc}$**
Inactive	Low	if address $\leq$ TC: increment if address > TC: don't change	active 3-state	High Low	active reduced
Active	Low	Held reset	3-state	High	active
Inactive	High	Not changing	3-state	High	standby
Active	High	Held reset	3-state	High	standby

Notes: 1. The XC17S00 RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC+1 = address 0.

XC17S05, XC17S10, XC17S20, XC17S30, XC17S40

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	**V**
V_{IN}	Input voltage relative to GND	-0.5 to V_{CC} +0.5	**V**
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	**V**
T_{STG}	Storage temperature (ambient)	-65 to +150	**°C**
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	**°C**
ESD	Human Body Model Mil-std-883D Method 3015	4000	**V**

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND (T_A = 0°C to +70°C)	4.75	5.25	V
	Industrial	Supply voltage relative to GND (T_A = -40°C to +85°C)	4.50	5.50	V

Note: During normal read operation both V_{CC} pins must be connected together.

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
I_{CCA}	Supply current, active mode (at maximum frequency)			10.0	mA
I_{CCS}	Supply current, standby mode			50.0	µA
I_L	Input or output leakage current		-10.0	10.0	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0MHz)			10.0	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0MHz)			10.0	pF

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XC17S05XL, XC17S10XL, XC17S20XL, XC17S30XL, XC17S40XL

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to +5.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to +5.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
ESD	Human Body Model Mil-std-883D Method 3015	4000	V

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND (T_A = 0°C to +70°C)	3.0	3.6	V
	Industrial	Supply voltage relative to GND (T_A = -40°C to +85°C)	3.0	3.6	V

Note: During normal read operation both V_{CC} pins must be connected together.

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -3 mA)	Commercial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = -3 mA)	Industrial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)			5.0	mA
I_{CCS}	Supply current, standby mode			50.0	µA
I_L	Input or output leakage current		-10.0	10.0	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0MHz)			10.0	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0MHz)			10.0	pF

AC Characteristics Over Operating Condition
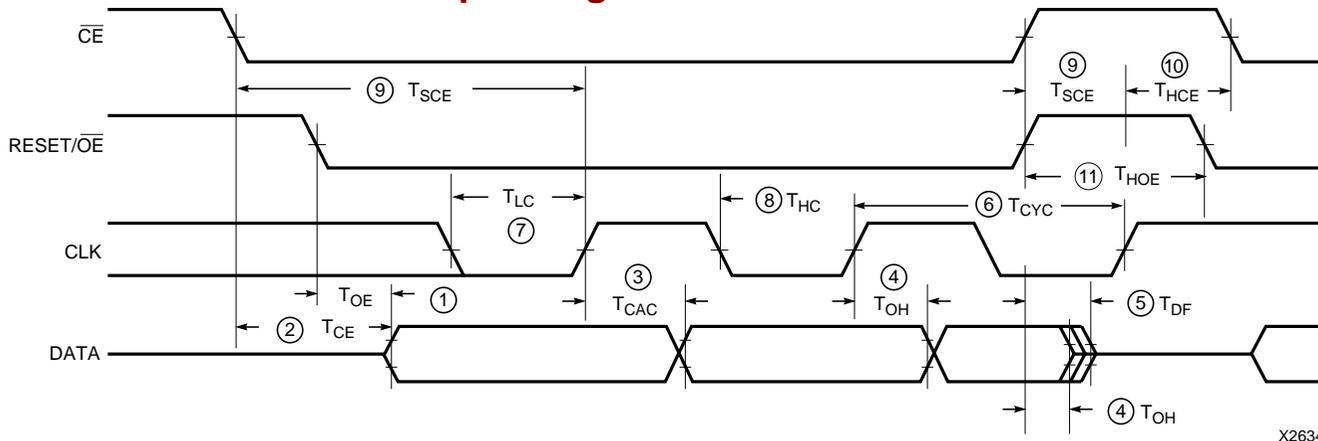
	Symbol	Description	Min	Max	Units
1	T_{OE}	$\overline{OE}$ to Data Delay		45	ns
2	T_{CE}	$\overline{CE}$ to Data Delay		60	ns
3	T_{CAC}	CLK to Data Delay		80	ns
4	T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK[3]	0		ns
5	T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay[2 & 3]		50	ns
6	T_{CYC}	Clock Periods (T_{CCLK} on FPGA)	100		ns
7	T_{LC}	CLK Low Time[3]	50		ns
8	T_{HC}	CLK High Time[3]	50		ns
9	T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25		ns
10	T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		ns
11	T_{HOE}	$\overline{OE}$ Hold Time (guarantees counters are reset)	25		ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at +200mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

AC Characteristics Over Operating Condition When Cascading
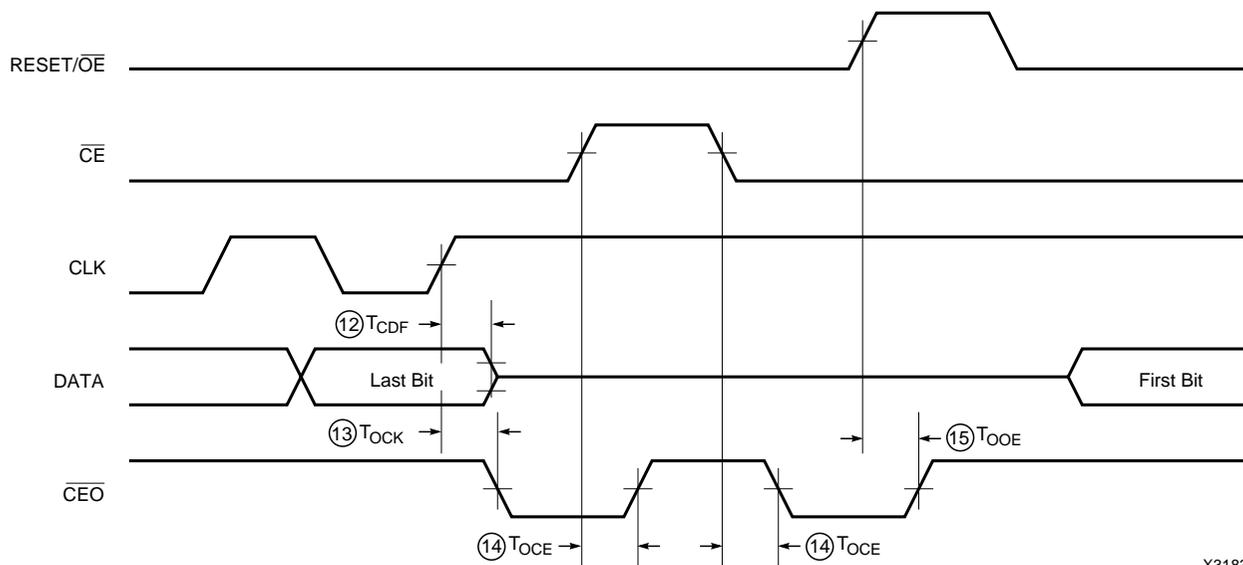
X3183

	Symbol	Description	Min	Max	Units
12	T_{CDF}	CLK to Data Float Delay[2 & 3]		50	ns
13	T_{OCK}	CLK to $\overline{CEO}$ Delay[3]		30	ns
14	T_{OCE}	CE to $\overline{CEO}$ Delay[3]		35	ns
15	T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay[3]		30	ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at +200mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.
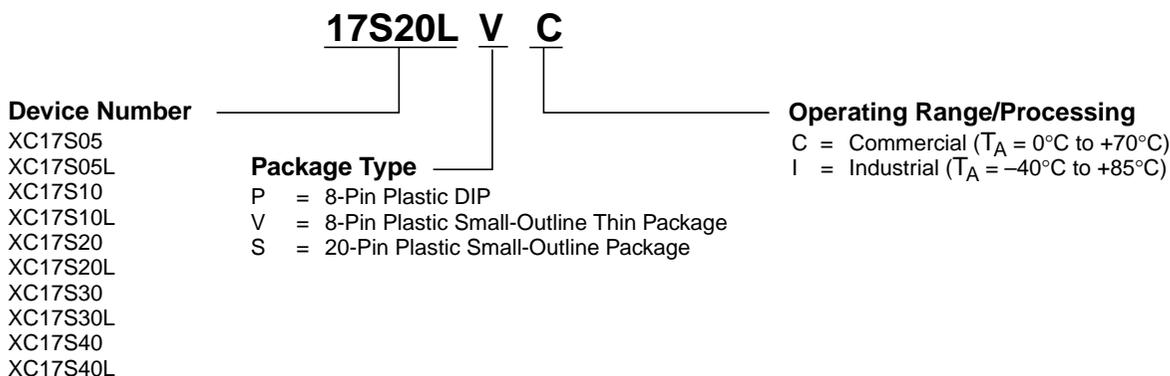
Ordering Information

XC17S20XL VO8   C

Device Number
XC17S05
XC17S05XL
XC17S10
XC17S10XL
XC17S20
XC17S20XL
XC17S30
XC17S30XL
XC17S40
XC17S40XL

Package Type
PD8 = 8-Pin Plastic DIP
VO8 = 8-Pin Plastic Small-Outline Thin Package
SO20 = 20-Pin Plastic Small-Outline Package

Operating Range/Processing
C = Commercial (T_A = 0°C to +70°C)
I = Industrial (T_A = –40°C to +85°C)
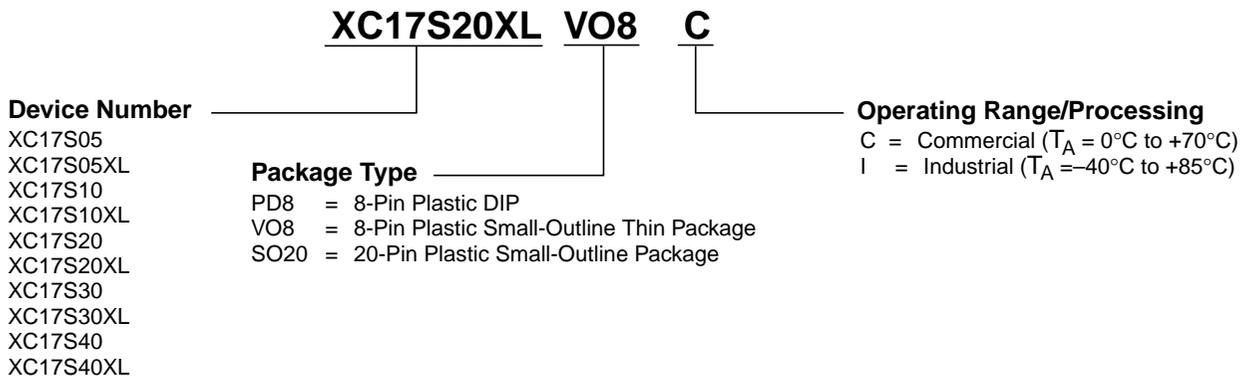
Valid Ordering Combinations

XC17S05PD8C	XC17S10PD8C	XC17S20PD8C	XC17S30PD8C	XC17S40PDC
XC17S05VO8C	XC17S10VO8C	XC17S20VO8C	XC17S30VO8C	XC17S40SO20C
XC17S05PD8I	XC17S10PD8I	XC17S20PD8I	XC17S30PD8I	XC17S40PD8I
XC17S05VO8I	XC17S10VO8I	XC17S20VO8I	XC17S30VO8I	XC17S40SO20I
XC17S05XLPD8C	XC17S10XLPD8C	XC17S20XLPD8C	XC17S30XLPD8C	XC17S40XLPD8C
XC17S05XLVO8C	XC17S10XLVO8C	XC17S20XLVO8C	XC17S30XLVO8C	XC17S40XLSO20C
XC17S05XLPD8I	XC17S10XLPD8I	XC17S20XLPD8I	XC17S30XLPD8I	XC17S40XLPD8I
XC17S05XLVO8I	XC17S10XLVO8I	XC17S20XLVO8I	XC17S30XLVO8I	XC17S40XLSO20I

Marking Information

Due to the small size of the serial PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.

17S20L V C

Device Number
XC17S05
XC17S05L
XC17S10
XC17S10L
XC17S20
XC17S20L
XC17S30
XC17S30L
XC17S40
XC17S40L

Package Type
P = 8-Pin Plastic DIP
V = 8-Pin Plastic Small-Outline Thin Package
S = 20-Pin Plastic Small-Outline Package

Operating Range/Processing
C = Commercial (T_A = 0°C to +70°C)
I = Industrial (T_A = –40°C to +85°C)

Note: When marking the device number on the XL parts, an L is used in place of an XL.