Xilinx HardWire™ FpgASIC Overview

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Introduction

When a system incorporating Xilinx FPGA's moves to high volume production, HardWire FpgASIC products should be the first consideration for cost reduction. HardWire products are the only devices developed specifically for Xilinx FPGA's which provide 100% pin compatible replacements. The HardWire conversion flow coupled with the HardWire test methodology provides a no risk path for customers to achieve dramatic cost reductions. Using Xilinx FPGA's and HardWire technology provides the customer with a single source for systems, software and silicon. This combination provides the fastest method for prototype development and production of systems based on leading edge programmable logic technology. Each HardWire product family is developed to match the performance and features of specific Xilinx FPGA's including the popular XC2xxx, XC3xxx, XC4xxx and XC5xxx series families. The newest family of HardWire FpgASIC's are designed to provide a cost reduced device incorporating the latest features of Xilinx FPGA's including E, EX and XL technology.

Technology Overview

Xilinx Hardwire ASIC products are FPGA specific ASIC's (FpgASIC's). They are a family of devices ranging from 1.0µ single mask mapped ASIC's to state-of-the-art sea-of-gates 0.5µ and 0.35µ multi-mask ASIC devices. The HardWire product families have been developed to match the performance and features of each generation of Xilinx FPGA's.

The HardWire flow is the simplest method for cost reducing an FPGA based system. The Xilinx "Design Once" methodology offers Xilinx customers the advantages of developing prototypes, building pre-production and initial production volumes using Xilinx FPGAs. Once the design is stable and cost reduction is critical, customers can convert the FPGA to a HardWire device developed especially for the features and performance of that FPGA.

The turnkey conversion process allows production quality HardWire prototypes to be developed in half the time of traditional gate arrays. The HardWire methodology provides this without using customers' engineering resources. HardWire FpgASIC's provide a cost - effective alternative to gate arrays.

Xilinx HardWire product families use a combination of industry standard and Xilinx patented test generation methods to achieve the most complete fault coverage possible. This testing strategy allows Xilinx to offer a cost reduction path that is 100% guaranteed to perform in the user's application.

Advantages of the Xilinx HardWire Methodology

Converting a device from programmable logic to a HardWire FpgASIC has many advantages over standard gate array redesign. The most important is that HardWire devices are developed using a fully turnkey process. No additional customer engineering is required to convert the programmable logic design into a fully tested, completely verified HardWire device. This ease of conversion is available only from Xilinx. HardWire devices are developed using the actual physical database previously created and verified in the process of developing the FPGA design. The HardWire conversion methodology preserves all the attributes of the original physical database file. If the design is mapped to a third party library at the schematic level for conversion to another technology, the design must be verified and prototyped. Third party implementations will change the placement and routing, thereby changing the design's performance characteristics. This means the new device must be re-verified and re-tested in the system to be certain that the performance and functionality still meet the applications requirements. A comparison of the activities required to convert a HardWire FpgASIC versus a generic gate array is shown in Figure 1.

Re-verifying the Design

In conventional gate array conversion (redesign), the design must be re-verified after the schematic is translated or recaptured. The process of re-verifying a design is rigorous and time consuming. Functional simulation vectors need to be created, and the device must be exhaustively simulated before and after place and route. A suitable test methodology must be considered and implemented. All this is usually done by the customer, at the customers' expense and risk.

In contrast, no additional effort is required when converting to a HardWire FpgASIC. The HardWire design is self-verifying because the actual FPGA database files are used for the conversion. This makes the HardWire conversion process the only guaranteed, fully turnkey FpgASIC conversion.

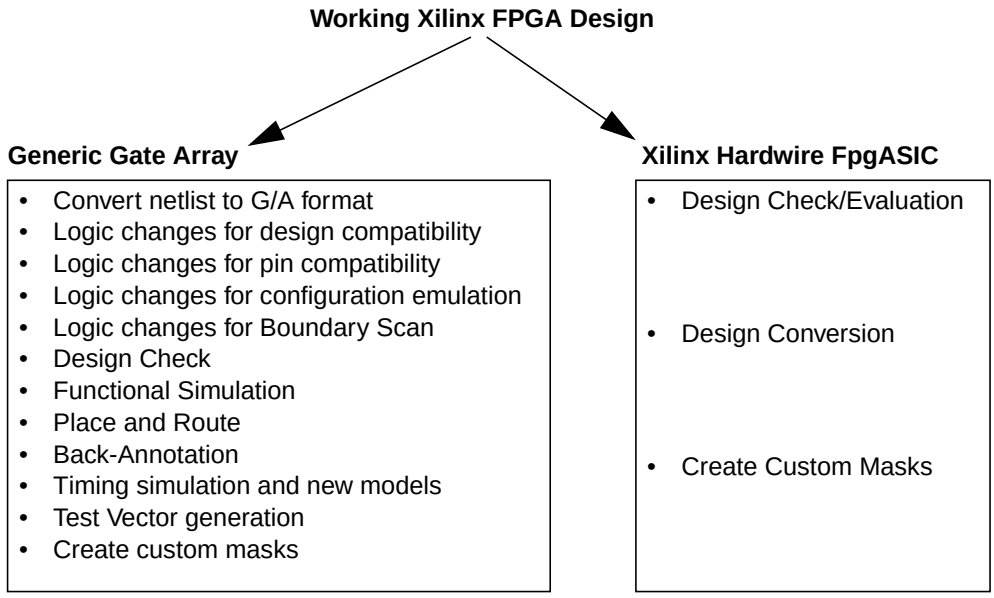

Figure 1: Steps Involved in Converting a PLD Design to a Gate Array as Compared to a HardWire FpgASIC

Fault Coverage and Test Vectors

All designs need to be testable. In a traditional gate array, the designer is required to build in testability and generate test vectors to verify chip performance by exercising as much of the device circuitry as possible. Most designers strive for greater than 90% fault coverage. However, they often settle for significantly less because the iterative process is time consuming and increases exponentially as fault coverage is increased. A third party conversion from a Xilinx FPGA to a generic gate array or other similar technology will require test vector generation. Typically, the original designers create test vectors, since they are most familiar with the FPGA's design. This method misuses valuable design resources and reverses the value of the decision to use programmable logic for their ease of design and time-to-market advantage. Another method is to contract with the conversion or gate array vendor to create the test vectors. This method is both expensive and time consuming. In some cases, conversion or gate array vendors will accept a design without test vectors, but the customer accepts the liability of determining whether the resulting device is production worthy. In today's competitive market, most projects can not afford the risk of possible re-spins if the design doesn't work.

Converting from a Xilinx FPGA to a HardWire FpgASIC requires no test vector generation by the customer. HardWire devices use a combination of industry standard and Xilinx patented test generation methods to achieve the most complete fault coverage possible. Xilinx guarantees greater than 95% fault coverage for most designs. All HardWire FpgASIC's are tested using a full scan test methodology. The HardWire conversion and test methodology provides a cost reduction path that is guaranteed to work in the customer's application.

Packaging and Silicon Considerations

All of the physical attributes of HardWire FpgASIC's are virtually identical to the Xilinx FPGA. HardWire devices are manufactured in the same fabrication facilities used by Xilinx for the production of FPGA's. The same design rules, IC process, as well as packaging, assembly, and test facilities are used. This allows a significant reduction in the time and cost associated with qualifying HardWire devices.

Converting from a Xilinx programmable logic device to any third party device means a change in silicon, packaging, assembly and test. Each of these changes adds an element of risk into the qualification process.

Support for the entire Product Life Cycle

Figure 2 shows the typical life cycle of a high-volume product. It illustrates the optimal way of using the programmable and HardWire devices. During development, prototyping and initial production cycles, the programmable device is the best choice. As the system moves into higher volume production and no additional modifications are being made to the design, a HardWire FpgASIC can be used in place of the original programmable logic device.

Since the HardWire device and the programmable logic device are functionally and physically identical, production can be switched back to the programmable device if the situation warrants. For example, if the demand for the customer's product increases dramatically, production can be increased immediately by full-filling the additional demand with programmable devices. The change can be made immediately since there is virtually no lead-time for an off-

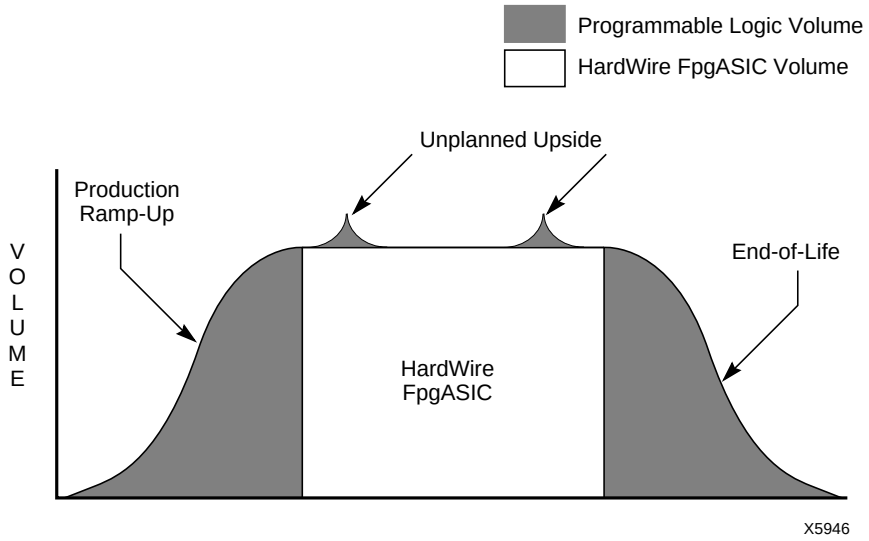

Figure 2: Typical High Volume Product Life Cycle

the-shelf programmable device. Production can also be switched to the programmable device as the product ends its life cycle and volume decreases. This eliminates the need for end-of-life buys and the risk of obsolescence.

Furthermore, designs implemented with multiple static RAM based programmable devices can be cost reduced incrementally, converting one or more of the programmable devices to a HardWire FpgASIC with the balance remaining as FPGAs. As each FPGA is converted to a HardWire device, the user benefits by having a lower cost for that device. This also allows the user to maintain the ease of use of off-the-shelf programmable logic in the other sockets. When all of the devices are converted, the storage element (PROM) can be removed, giving even further cost reductions. This flexibility is unique to Xilinx, and allows customers to achieve cost reduction quickly with minimal effort.

HardWire Design/ Production Interface

Figure 3 illustrates how the design, development and production activities for both Programmable Logic devices and HardWire FpgASICs are sequenced. Notice that by using the Xilinx “Design Once” methodology, no additional customer activity is needed to develop the HardWire FpgASIC. If design simulation is done in the programmable logic device during development, special HardWire speed files may be also be used for design verification. This allows Xilinx to perform a very simple design check procedure prior to generating the HardWire device. After the design check is complete the HardWire prototypes can be manufactured. The customer then performs in-system verification of the prototypes. Once this verification is complete the HardWire FpgASIC can be released to production. Since the functionality of the FPGA and HardWire device are identical, virtually no customer engineering resources are needed to move from the programmable to the HardWire devices or vice versa. By comparison, using a traditional gate array to reproduce functions implemented in the FPGA would require extensive simulation and test development.

Design Submittal Process

Once the complete design submittal kit is received the HardWire conversion process takes from 3 to 8 weeks. The conversion time will vary with the addition of features such as Select-RAM, Configuration Emulation and JTAG. A complete design submittal kit contains the following:

1. Files: .LCA (or .NGD for M1 designs), .MBO, and .BIT files on disk.
2. Hard copy of a board level schematic showing how the FPGA interfaces with other components on the board (if possible).
3. A detailed explanation of any special requirements for the conversion.
4. A design submittal form and NRE PO.

All forms can be found in the HardWire data book and on the Xilinx web page under HardWire products.

Summary of the Conversion Process

The HardWire FpgASIC conversion process is the simplest way to cost reduce systems designed using FPGAs. The customer is involved in tracking and approving milestones. Xilinx handles the day-to-day activities of converting the design to a HardWire device. Once Xilinx receives a complete design submittal kit the conversion process begins.

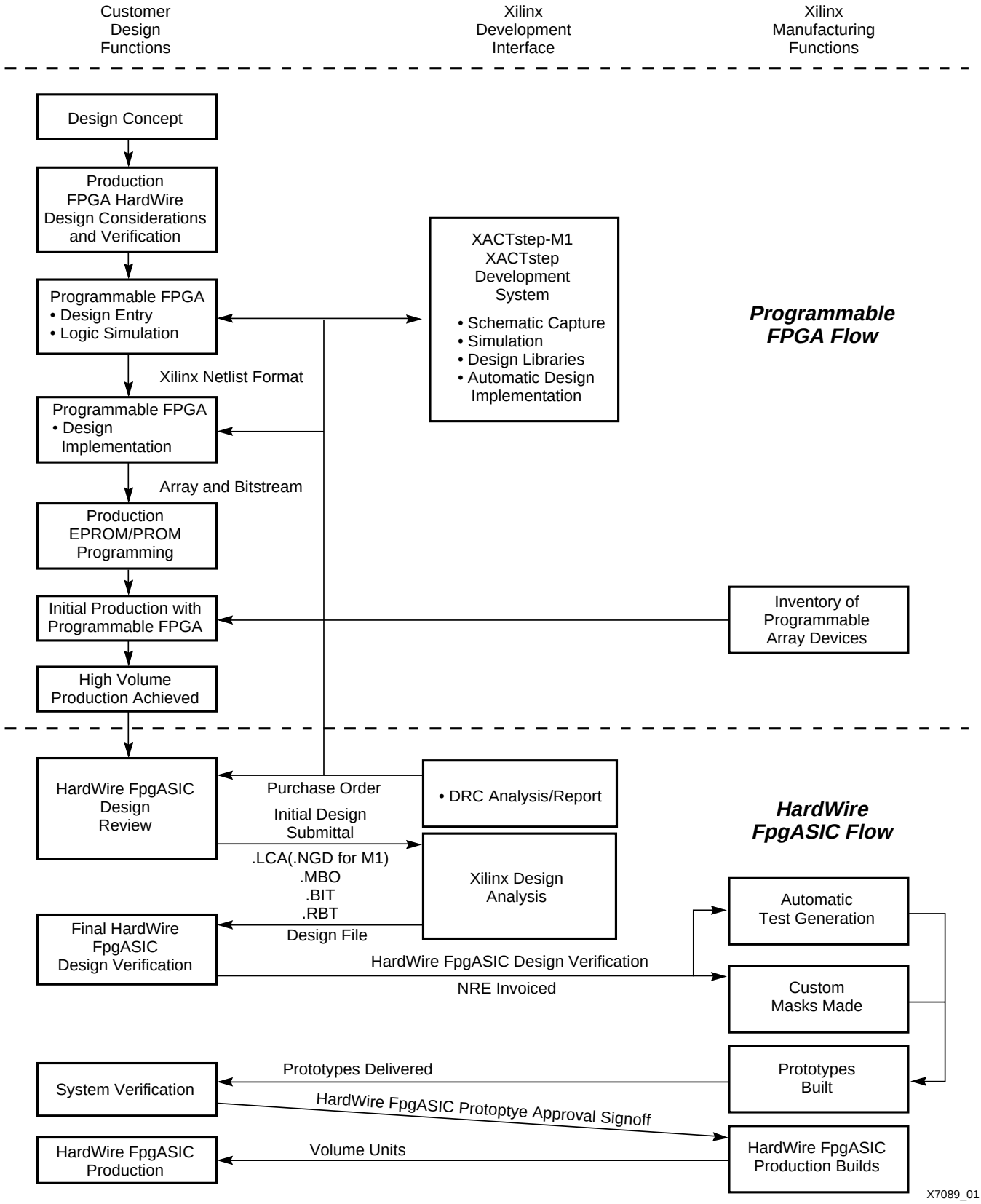

Figure 3: Programmable/HardWire Design/Production Interface

Table 1: HardWire Products

Device Family	Speed Grade	Features Supported	Hardwire FpgASIC Family	Notes
XC2xxx	All	All	XC2318	1
XC3xxx	All	All	XC33xx	1
XC4xxx	-4 and slower	No E features	XC43xx	1
XC4xxxE/EX/XL	-3 and slower	E, EX, XL	XC44xx	
XC4xxxE/EX/XL	-3 and faster	E, EX, XL	XH3xx	
XC5xxx	All	Non XL	XC54xx	

Note 1: Some devices require re-routing before conversion. Refer to the HardWire Data Book

Xilinx first reviews the design to determine any items that could impact the performance of the HardWire device. A conversion evaluation report is sent to the customer. After the report has been reviewed and the customer is satisfied, conversion begins. At the completion of the conversion a Design Verification Report and Design Verification Form (DVF) are sent to the customer. Once the DVF is completed the HardWire files are sent to the mask shop for prototyping. If any custom markings are required they must be submitted to Xilinx with the Design Verification Form (DVF). Prototypes are produced, tested and shipped to the customer for in-system testing. The customer signs the prototype approval form and returns it to Xilinx. Production can begin.

HardWire Product Families

Each HardWire product family is developed to support the features, density and performance of a specific generation of Xilinx FPGA's. See Table 1 for product family details. For designs developed using Xilinx XC2xxx, XC3xxx or XC4xxx (no E features) FPGAs, the XC23xx, XC33xx and 43xx product families provide a fast and simple cost reduction path. For designs developed using Xilinx XC4xxx (E, EX and XL) and XC5xxx FPGAs, the XC44xx and XC54xx product families provide the most effective technology, cost and performance. For customers using fast, dense Xilinx XC4xxxE, EX and XL or XC5xxx FPGA's the XH3 product family provides the most efficient and cost effective solution available. Most HardWire FpgASIC's are available in 3.3v versions. All HardWire devices support commercial and industrial temperature ranges.

Xilinx HardWire Product Descriptions

XC23xx, XC33xx and XC43xx Product Description

The initial HardWire product family was developed to match the performance of Xilinx XC2xxx, XC3xxx and slower XC4xxx family FPGA's. This family is still in production today. In standard programmable logic, the functions and interconnections are determined by configuration data stored in memory cells. In the first generation HardWire technology, the memory cells and programmable interconnect logic they control are replaced by metal connections. All other circuitry in the resulting HardWire device is identical to the corresponding FPGA internal circuitry. The resulting HardWire FpgASIC is a semi-custom device manufactured to provide a specific function, yet it is completely compatible with the FPGA. This product family is the fastest and most simple method of converting first generation Xilinx FPGA's. For more details on XC23xx, XC33xx and XC43xx products please see the Xilinx HardWire Data Book.

XC23xx, XC33xx and XC43xx Summary

Features

- Designed for conversion of XC2xxx, XC3xxx and XC4xxx (no E features) FPGAs.
- Single Mask
- Direct Mapped - Turnkey conversion from FPGA device.
- On-chip scan path test latches.
- Fully pin-for-pin compatible.

Benefits

- Simple and efficient conversion process.
- Very fast conversion completion time.
- Conversion success rate over 95%.
- No customer developed test vectors needed, 99% fault coverage.
- Drop-in replacement for Xilinx FPGAs.

XC44xxE/EX/XL and XC54xx Product Description

The second generation HardWire FpgASIC product family was developed to match the performance, density and features of Xilinx XC4xxxE, EX, XL and XC5xxx family of FPGA's. This HardWire FpgASIC product family supports all the features of Xilinx second generation FPGAs. This includes –3 speed grades, Configuration Emulation (CE), JTAG and Select-RAM. The XC44xx and XC54xx product family follows a more traditional sea-of-gates approach to mapping used CLBs of the FPGA. The used memory cells and programmable interconnect logic of the FPGA are mapped into a corresponding area of a traditional gate

array base. The FPGA's unused CLBs are not mapped into the resulting HardWire device. The HardWire device uses the smallest base array possible while maintaining the performance and functionality of the corresponding FPGA. These devices support most 3.3 volt and 5 volt FPGAs. The feature sizes of the arrays used in the XC44xx and XC54xx product family (1.0µ through .45µ) are highly competitive with traditional gate arrays. The wide range of base array feature sizes available allows Xilinx to provide a HardWire device with the smallest possible die size. The same guaranteed turnkey conversion methodology is used. XC44xx and XC54xx devices provide the most cost-effective method for converting XC4xxxE, XC4xxxEX, XC4xxxXL and XC52xx FPGA's to a low cost HardWire FpgASIC.

XC44xx/E/EX/XL and XC54XX Summary

Features

- Designed for conversion of XC4xxxE, EX, XL and XC5xxx FPGAs.
- Only used CLBs are mapped.
- Multiple mask, state-of-the-art, gate array process.
- On-chip scan path test latches.
- Fully pin-for-pin compatible.
- Smallest possible die size.

Benefits

- All Xilinx FPGA features supported, including CE, JTAG and Select-RAM.
- Smallest possible die size used to achieve the lowest possible cost.
- Technology feature size matched to performance requirements.
- No customer developed test vectors needed. Greater than 95% fault coverage (design dependent).
- Drop in replacement for Xilinx FPGAs.

XH3 Product Description

The third generation HardWire FpgASIC product family, known as XH3, was developed to match the density, performance and features of the fastest, most fully featured Xilinx XC4xxxEX, XL and XC5xxx family of FPGAs. Initial XH3 products are based on 0.5µ, 5-volt process technology, followed by 0.35µ, 3.3-volt XH3L technology. XH3 technology was developed specifically for Xilinx FPGA conversions. It uses a dense sea-of-gates CMOS gate array technology. At 0.5µ and 0.35µ, the process geometry is small enough that die sizes are driven by pad count and not gate count.

Important features used in Xilinx FPGAs such as Configuration Emulation, JTAG, and Select-RAM are easily implemented in XH3 technology. The control logic for Configuration Emulation, Power on Reset (POR), Oscillators and full JTAG are built into the XH3 base array. These features can usually be implemented with no additional silicon overhead. RAM blocks are incorporated with maximum efficiency. The XH3 architecture implements Select-RAM 30% more efficiently than generic gate arrays.

In generic gate array methodologies, features such as Configuration Emulation, JTAG and Select-RAM usually require additional silicon area. The result is a larger, more expensive die and changes to the FPGA netlist throughout the conversion process. In many cases implementing Xilinx Select-RAM in a third party gate array may require substantially more gates than the Xilinx XH3 device. XH3 devices incorporate these features without silicon overhead or changes to the netlist.

XH3 Summary

Features

- Designed for conversion of XC4xxxE, EX, XL and XC5xxx FPGAs.
- Xilinx FPGA features built in to the base array.
- Multiple Mask, state-of-the-art 0.5µ and 0.35µ process technology.
- Pad counts and gate counts available for the densest FPGA devices.
- On chip scan path test latches.
- Fully pin for pin compatible.
- Package flexibility available.

Benefits

- All Xilinx FPGA features supported, including CE, JTAG and Select-RAM.
- Patented, turnkey conversion flow.
- Pads and package required determine device used.
- No customer developed test vectors needed. Greater than 95% fault coverage (design dependent).
- Drop in replacement for Xilinx FPGAs.
- Conversions to smaller packages available.

HardWire Summary

Xilinx Hardwire ASIC products are FPGA specific ASIC's (FpgASIC's). They are a family of devices ranging from 1.0µ single mask mapped ASIC's to state-of-the-art sea-of-gates 0.5µ and 0.35µ multi-mask ASIC devices. The HardWire flow is the most simple method of cost reduction for FPGA based systems. They are developed using the FPGA's design files. This guarantees the HardWire FpgASIC will be functionally equivalent to the FPGA. No customer generated test vectors are required with HardWire. Each HardWire device is tested using a combination of industry standard and Xilinx patented test methods in a full scan methodology. The full scan test methodology provides greater than 95% fault coverage depending on the design. HardWire prototypes can be developed in half the time of traditional gate array prototypes. HardWire process technologies, conversion methods and testing procedures provide the most cost - effective alternative to traditional gate arrays.