November 21, 1997 (Version 2.0)

Quality Assurance Program

All aspects of the Quality Assurance Program at Xilinx have been designed to eliminate the root cause of defects, rather than to try to remove them by inspection. A quality system was put in place which is in full compliance with the requirements of ISO9002. Xilinx was found to be in full compliance of the requirements of ISO9002:1994 by an independent auditor in October, 1995. At that time Xilinx was registered for “the manufacturing and testing of programmable logic devices”. Last November, Xilinx was audited by DSCC and found in full compliance with the requirements of MIL 38535 for a QML supplier. In January 1997 Xilinx was formaly granted transitional QML approval by DSCC.

The aspects of ISO compliance in place at Xilinx include the following seventeen points:

- **Management Review:** a comprehensive system of management attention and direction for all aspects of company performance that directly affect our customers. These include (among others) Xilinx performance in the areas of Quality, Reliability and On-Time Delivery. Management assures that this quality policy is understood, implemented and maintained at all levels in the organization.
- **Quality Systems:** are in place to ensure that product conforms to customer specifications. These systems facilitate, measure and continuously improve Xilinx performance in those areas that affect customer satisfaction. Xilinx remains committed to achieving 100% customer satisfaction.
- **Contract Review:** is conducted to ensure each contract adequately defines and documents requirements, that differences between customer and Xilinx standard specifications are mutually satisfactorily resolved, and that Xilinx has the capability to meet contract requirements.
- **Document Control:** procedures are established and maintained to control all documents and data that relate to the performance of Xilinx business and processing requirements. All organizations who need access to such documentation during the performance of their functions are assured availability of the latest, controlled versions of that documentation.
- **Purchasing:** procedures are in place to ensure that all purchased products conform to the specified requirements. As Xilinx is a “fabless” manufacturing company, special attention is paid to our subcontract partners. They are required to demonstrate the type of control and capabilities that our customers require. All key Xilinx subcontract partners are ISO certified.
- **Product Identification & Traceability:** is maintained throughout the manufacturing process. Traceability back to the starting materials is available through unique product identification techniques and markings throughout the manufacturing process.
- **Process Control:** is assured by identifying and controlling those processes that directly affect the quality of our products, whether those processes are performed directly by Xilinx, or by our subcontract partners.
- **Inspection & Test**: is performed to ensure that incoming product is not used or processed until it has been verified as conforming to required specifications. This inspection is done jointly by Xilinx and by its subcontract partners.
- **Inspection, Measuring and Test Equipment:** is calibrated in conformance with the requirements of Mil Ref 45662 and/or other international standards. Equipment is maintained in such a manner to ensure that measurement uncertainty is known and is consistent with specification requirements.
- **Inspection & Test Status:** of product is uniquely identified throughout the manufacturing process both at Xilinx and at our subcontract partners. Records are kept to identify the authority responsible for the release of conforming production.
- **Control of Non-Conforming Product:** is assured through disposition procedures that are defined in such a manner as to prevent the shipping of non-conforming products. The responsibility and authority for the disposition of such products are well defined.
- **Corrective Action:** processes are documented and implemented to prevent the recurrence of nonconforming product. These processes are the key to implementing the Xilinx strategy of eliminating the root causes of nonconformity, rather that to apply inspection to try to remove nonconformity.
- **Handling, Storage, Packing & Delivery:** procedures are defined and implemented to prevent damage or deterioration of product once the manufacturing process is complete.
- **Quality Records:** procedures are established and maintained for the identification, collection, indexing, filing, storage, maintenance and disposition of quality records.
- **Internal Quality Audits:** are carried out to verify whether quality activities comply with planned

arrangements and to determine the effectiveness of the quality system. These audits are regularly supplemented by quality audits performed by our customers, and by our independent ISO auditors.

- **Training:** procedures have been established and are maintained to identify the training needs of all personnel affecting quality during the production of Xilinx products. Personnel performing such activities are qualified based upon appropriate education, training and/or experience.
- **Statistical Techniques:** are in place at Xilinx and at our subcontract partners for verifying the acceptability of process capabilities and product characteristics.

These key requirements are in place at Xilinx and at our subcontract partners to ensure our ability to achieve customer satisfaction through the **on-time delivery** of **quality products** that **meet customer requirements** and are **reliable**.

Device Reliability

Device reliability is often expressed in a measurement called *Failures in Time* (FITs). In this measure one FIT equals one failure per billion (10^9) device operating hours. A failure rate in FITS must include the operating temperature to be meaningful. Hence failure rates are often expressed in FITS at 70°C (or some other temperature in excess of the application).

Since one billion hours is well in excess of 100,000 years, the FIT rate of modern ICs can only be measured by accelerating the failure rate by testing at a higher junction temperature (usually 125°C or 145°C). Extensive testing of Xilinx devices (performed on actual production devices taken directly from finished goods) has been accomplished continuously since 1989 and reported quarterly. Quarterly reports on the reliability of Xilinx products are available through your Xilinx sales representative and at the WebLINX web site (www.xilinx.com). During the last two years, over 20,000 devices have accumulated a total of over 36,000,000 hours of both static and dynamic operation at 125°C (equivalent) to yield the FIT rates shown in Figure 1.

Description of Tests

Die Qualification

1. **High Temperature Life**: This test is performed to evaluate the long-term reliability and life characteristics of the die. It is defined by the Military Standard from which it is derived as a “Die-Related Test” and is contained in the Group C Quality Conformance Tests. Because of the acceleration factor induced by higher temperatures, (typically 125°C and/or 145°C) data representing a large number of equivalent hours at a normal temperature of 25°C can be accumulated in a reasonable period of time.
2. **Biased Moisture Life**: This test is performed to evaluate the reliability of the die under conditions of long-term exposure to severe, high-moisture environments that could cause corrosion. Although it clearly stresses the package as well, this test is typically grouped under the die-related tests. The device is operated at maximum-rated voltage, 5.5 Vdc, and is exposed to a temperature of 85°C and a relative humidity of 85% throughout the test.

Package Integrity and Assembly Qualification

1. **Unbiased Pressure Pot**: This test is performed at a temperature of 121°C and a pressure of 2 atm of saturated steam to evaluate the ability of the plastic encapsulating material to resist water vapor. Moisture penetrating the package could induce corrosion of the bonding wires and nonglassivated metal areas of the die (bonding pads only for FPGA devices). Under extreme conditions, moisture could cause drive-in and corrosion under the glassivation. Although it is difficult to correlate this test to actual field conditions, it provides a well-established method for relative comparison of plastic

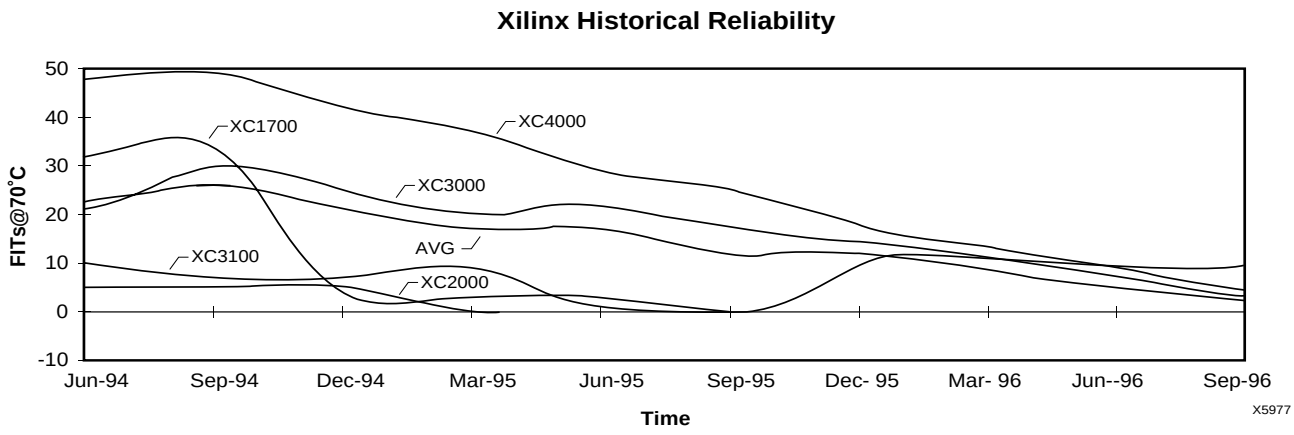

Figure 1: Failure Rates in FITs

packaging materials and assembly and molding techniques.

2. **Thermal Shock**: This test is performed to evaluate the resistance of the package to cracking and resistance of the bonding wires and lead frame to separation or damage. It involves nearly instantaneous change in temperature from -65°C to +150°C (condition “C”).
3. **Temperature Cycling**: This test is performed to evaluate the long-term resistance of the package to damage from alternating exposure to temperature extremes. The range of temperatures is -65°C to +150°C (condition “C”). The transition time is longer than that in the Thermal Shock test but the test is conducted for many more cycles.
4. **Salt Atmosphere**: This test was originally designed by the US Navy to evaluate resistance of military-grade ship-board electronics to corrosion from sea water. It is used more generally for non-hermetic industrial and commercial products as a test of corrosion resistance of the package marking and finish.
5. **Resistance to Solvents**: This test is performed to evaluate the integrity of the package marking during exposure to a variety of solvents. This is an especially important test, since an increasing number of board-level assemblies are subjected to severe conditions of automated cleaning before system assembly. This test is performed according to the methods specified by MIL-STD-883.
6. **Solderability**: This test is performed to evaluate the solderability of the leads under conditions of low soldering temperature following exposure to the aging effects of water vapor.
7. **Lead Fatigue**: This test is performed to evaluate the resistance of the completed assembly to vibrations during storage, shipping, and operation.

Testing Facilities

Xilinx has complete capability to perform High Temperature Life Testing, Thermal Shock, Temperature Cycling, Biased Moisture Life Test, Unbiased Pressure Pot, Solderability and Hermeticity, as well as complete Failure Analysis in house. Table 1 and Table 2 show typical qualification requirements for new and/or changed process flows. Table 3 is a list of current failure analysis capabilities. These laboratories are dedicated exclusively to increasing customer satisfaction through continuous improvements in our processes and technologies.

Table 1: Plastic Package/Product Qualification Requirements

							New Assy Techniques (Mat'l/Process/Method								
Test Seq	**Test Description (note 1)**	**Acc# S.Size (note 2)**	**New Assy Plant**	**New Pkg Type I (note3)**	**New Pkg Type II (note4)**	**New Pkg Type III LF Design (note5)**	**Lead Frame**	**Die Attach**	**Die Coat**	**Wire Bond**	**Mold CLP**	**Lead Finish**	**New Device Mask (note6)**	**New Fab Proc**	**Full Qual**
B1	* Phy. Dimension	0/5	X	X	X							X			X
B2	* Resist. to Solvents	0/3	X								X	X			X
B3	* Solderability Test (note 7)	0/5	X				X					X			X
B4	Solder Heat Test (Optn'l)	0/15				X	X				X				X
B5	Auto Clave (SPP)(Optn'l) 0/76	0/76	X	X	X	X	X		X		X		X		X
B6	* Ball Shear/Bond Pull (note 7)	0/5	X	X					X	X	X		X	X	X
B7	** X-Ray (note 7)	0/5	X	X	X	X			X	X	X		X		X
B8	* S.A.T/Dye Pen Test (note 7)	0/10	X	X	X	X	X				X	X			X
B9	* Adhesion of L/Finish (Optn'l)	0/3	X				X					X			X
B10	* External Visual (note 7)	0/25	X	X	X	X	X				X				X
B11	Internal Visual (note 7)	0/5	X	X	X		X	X	X	X			X	X	X
B12	* Die Shear (note 7)	0/5	X					X					X	X	X
B13	Flammability Test (note 7)	Per lot									X				X
C1-A	High Temp Life Test	0/76							X				X	X	X
C1-B	Low Temp Life Test (note 7)	0/22											X	X	X
C2	C2-A:HAST (0/22) or C2-B: 85/85	0/76	X	X		X	X	X	X		X			X	X
C3	ESD (HBM)	0/3											X	X	X
C4	High Temp Storage (Optn'l)	0/77									X		X	X	X
D1	* Lead Integrity	0/3	X	X	X							X			X
D2	Thermal Shock (Optn'l)	0/76													X
D3	Temp Cycle	0/76	X	X	X	X	X	X	X	X	X			X	X
E1	Electrical Test & Data Log	0/30											X	X	X
E2	Electrical Characterization	0/30											X	X	X
E3	T.D.D.B (note 7)	–											X	X	X
E4	Latch-up	0/9											X	X	X
E5	Electromigration (note 7)	–											X	X	X
E6	Photosensitivity (Optn'l)	0/11											X	X	X
E7	Data Retention Bake EPLD & EPR	0/22											X	X	X
E8	Input/Output Capacitance	0/5											X	X	X
E9	Power Cycling (Optn'l)	0/22											X	X	X
Qty required per lot		E.Good	239	238	162	248	248	157	314	86	325	0	393	464	636
		E.Reject	63	48	43	35	43	5	5	5	43	29	10	10	64
		Total	302	286	205	283	291	162	319	91	368	29	403	474	700

Notes:
1) Test method and stress conditions available upon request.
2) For any QUAL which does not meet the standard requirements, approval from Product Engineering and Product QA is required.
3) Any new package which has not been qualified in the qualified assembly facility.
4) Any new package where the same body size with different lead pitch has been qualified.
5) New leadframe design whereby the paddle size is larger than the existing leadframe paddle size used in the same qualified package.
6) For new mask from same device family, only high temp life test, ESD, Latch & Capacitance are required.
7) In-process monitor data may be used to satisfy this requirement.
*) Electrical rejects can be used as test sample.
**) This is a non-destructive test, sample can be re-used.

Table 2: Hermetic Package/Product Qualification Requirements (Commercial)

						New Assy Techniques (Mat'l/Process/Method									
Test Seq	**Test Description (note 1)**	**Acc# S.Size (note 2)**	**New Assy Plant**	**New Pkg Family (note3)**	**New Pkg Qual Family (note4)**	**Lead Frame**	**Die Attach**	**Die Coat**	**Wire Bond**	**Type of Seal**	**Lead Finish**	**New Cavity Size (note6)**	**New Device (note6)**	**New Fab Proc**	**Full Qual**
B1	Solder Heat Test (Optn'l)	0/15		X	X					X		X			X
B2	* Resist. to Solvents (note 7)	0/3	X	X							X				X
B3	* Solderability Test (note 7)	0/3	X	X		X					X				X
B4	* Die Shear/Stud Pull (note 7)	0/5	X	X	X		X						X	X	X
B5	* Bond Pull (note 7)	0/2	X	X	X	X		X	X				X	X	X
B6	* External Visual (note 7)	0/25	X	X	X	X			X		X				X
B7	Internal Visual (note 7)	0/5	X	X	X	X	X	X	X				X	X	X
C1-A	High Temp Life Test	0/76	X	X				X	X				X	X	X
C1-B	Low Temp Life Test (note 7)	0/22											X	X	X
C2	High Temp Storage (Optn'l)	0/77						X					X	X	X
C3	ESD (HBM)	0/3											X	X	X
D1	* Phy. Dimension	0/15	X	X	X						X	X		X	X
D2	* Lead Integrity	0/3	X	X	X	X					X			X	X
D3	Thermal Shock + Temp Cycl + Moisture Resistance	0/32	X	X	X	X	X	X	X	X	X	X	X	X	X
D4	Mech. Shock + Vibration + Constant Acceleration	0/32	X	X	X	X	X		X	X		X	X	X	X
D5	* Salt Atmosphere	0/15	X	X	X						X			X	X
D6	* Internal Vapor Content (note 7)	0/3	X	X	X		X	X		X		X		X	X
D7	* Adhesion of L/Finish (Optn'l)	0/2	X	X	X	X					X			X	X
D8	* Lid Torque	0/5	X	X	X					X		X		X	X
D9	Temp Cycle	0/45	X	X	X		X	X	X	X		X	X	X	X
E1	Electrical Test & Data Log	0/30											X	X	X
E2	Electrical Characterization	0/30											X	X	X
E3	T.D.D.B (note 7)	–											X	X	X
E4	Latch-up	0/9											X	X	X
E5	Electromigration (note 7)	–											X	X	X
E6	Photosensitivity (Optn'l)	0/11											X	X	X
E7	Data Retention Bake	0/22											X	X	X
E8	Input/Output Capacitance	0/5											X	X	X
Qty required per lot		E.Good	190	205	129	69	114	235	190	124	32	124	399	399	414
		E.Reject	81	81	75	50	8	5	2	33	41	48	7	50	81
		Total	271	286	204	119	122	240	192	157	73	172	406	449	495

Notes:
1) Test method and stress conditions available upon request.
2) For any QUAL which does not meet the standard requirements, approval from Product Engineering and Product QA is required.
3) Package Family - A set of package type with the same package, material, Package construction techniques, terminal pitch, lead shape, row spacing and with identical package assembly tech.
4) Package Type - A package with a unique case outline, configuration, material, piece parts and assembly process.
5) Application to new piece parts or leadframe where cavity size is larger than the largest cavity size for the same package.
6) For new mask from same device family, only high temp life test, ESP, Latch & Capacitance are required.
7) In-process monitor data may be used to satisfy this requirement, for Qual data, data from Assy. lot traveler maybe used.
*) Electrical rejects can be used as test samples

Table 3: Failure Analysis Equipment List

Item	Equipment	Vendor	Model Number
1	Scanning Electron Microscope	JEOL	JMS-6401F
2	Gold Sputter (SEM Sample Prep)	ANATECH	Hummer VIII
3	Energy Dispersive X-Ray	OXFORD INST.	LINK ISIS-L200C
4	F.I.B. - Focused Ion Beam Workstation	F.E.I.	FIB-600
5	Real-Time X-Ray Imaging System	FEIN FOCUS	FXS-100.10
6	Scanning Acoustic Microscopy	Sonix	Micro-Scan 4HF-200
7	Ball Shear Strength Tester	KELLER	MBS-200
8	XRF Lead Finish/Composition Measurement System	Twin City, Inc.	XRF-5500
9	Liquid Crystal Hot Spot Detection System/Kit, with 3 temp.	Technology Associates	P/N 4330
10	Emission Microscope for Multilayer Inspection (EMMI)	Hypervision	Visionary 2000
11	Curve Tracer	BID Services	
12	Metallurgical High Power Microscope	Scientific Instrument Company	see quote (various)
13	Stereozoom Low Power Microscope - video camera + monitor	Scientific Instrument Company	see quote (various)
14	Micro-Etcher System	TM Associates	
15	Viseco Camera Interface with High Power Microscope	Computer Modules	
16	Hermeticity Test System - Fine Leak - Gross Leak	BID Services	-Trio-tech 486 - Veeco MS-170
17	Die-Shear Tester	KELLER	see #7
18	Steam Aging System	Robotic Systems	ST2D
19	Solder Wave/Pot	Robotic Systems	RPS-202
20	Lead Fatigue Tester	B & G	004-012-00
21	Conventional Oven (C.D.A.)	BID Services	
22	Drill-bit to open MQUADS + Decapping vise		
23	Color Printer	Tektronic	Tektronic Phaser IISD
24	Stud Pull Tester	B & G	003-010-00
25	Work Benches		
26	Cabinets		
27	Facilities (Lab Area and Equipment Installation Costs)		
28	Tool Maker Microscope		
29	Flowhood & Rinse Station		
30	Precision X-Sectioning Equipment		
31	Plasma Etcher	March Instruments	CS-1701
32	E-Beam IDS-3000		

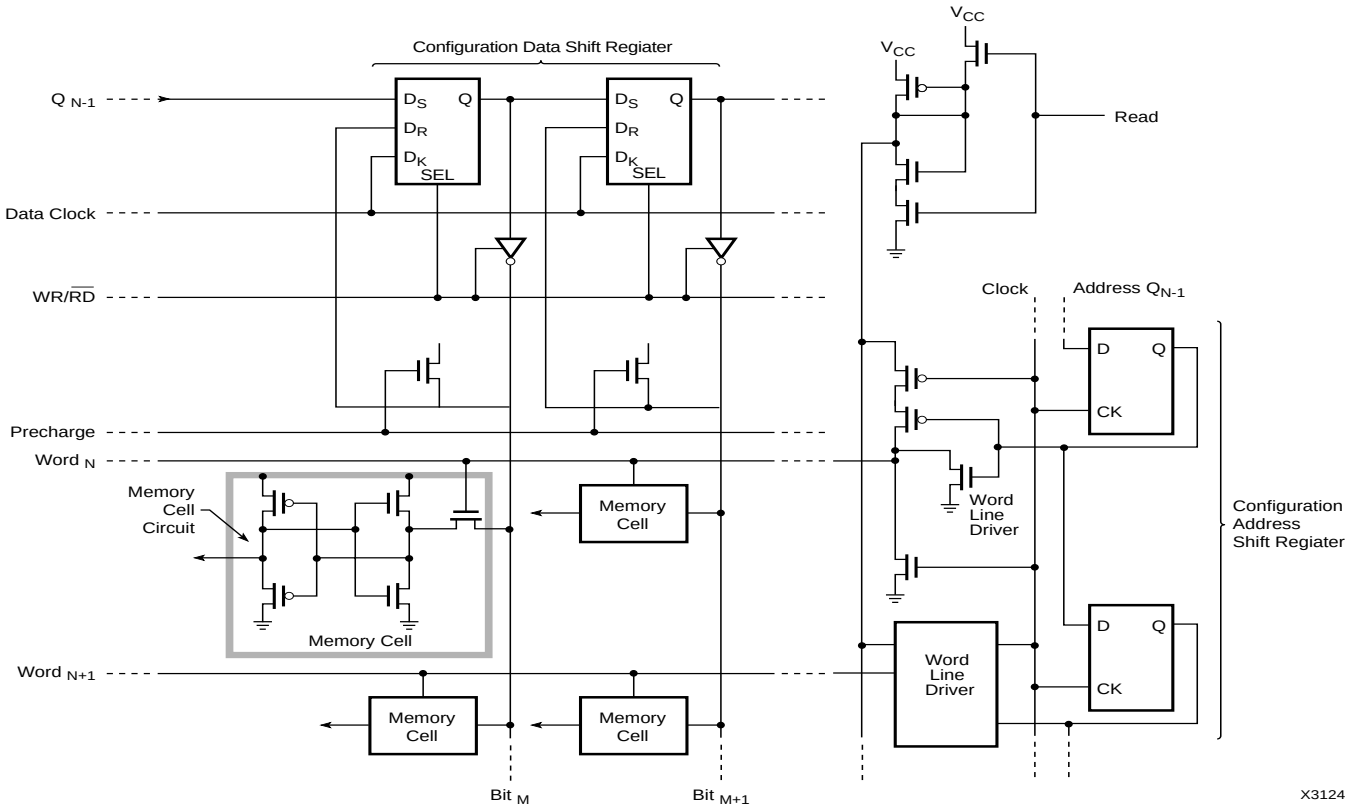

Figure 2: Configuration Memory Cell

Data Integrity

Memory Cell Design in the FPGA Device

An important aspect of SRAM-based FPGA device reliability is the robustness of the static memory cells used to store the configuration program.

The basic cell is a single-ended 5-transistor memory element (Figure 2). By eliminating a sixth transistor, which would have been used as a pass transistor for the complementary bit line, a higher circuit density is achieved. During normal operation, the outputs of these cells are fixed, since they determine the user configuration. Write and readback times, which have no relation to the device performance during normal operation, will be slower without the extra transistor. In return, the user receives more functionality per unit area.

This explains the basic cell, but how is the FPGA user assured of high data integrity in a noisy environment? Consider three different situations: normal operation, a Write operation and a Read operation. In the normal operation, the data in the basic memory element is not changed. Since the two circularly linked inverters that hold the data are physically adjacent, supply transients result in only small relative differences in voltages. Each inverter is truly a complementary pair of transistors. Therefore, whether the output is High or Low, a low-impedance path exists to the supply rail, resulting in extremely high noise immunity. Power supply or ground transients of several volts have no effect on stored data.

The transistor driving the bit line has been carefully designed so that whenever the data to be written is opposite the data stored, it can easily override the output of the feedback inverter. The reliability of the Write operation is guaranteed within the tolerances of the manufacturing process.

In the Read mode, the bit line, which has a significant amount of parasitic capacitance, is precharged to a logic one. The pass transistor is then enabled by driving the word line High. If the stored value is a zero, the line is then discharged to ground. Reliable reading of the memory cell is achieved by reducing the word line High level during reading to a level that insures that the cell will not be disturbed.

Electrostatic Discharge

Electrostatic-discharge (ESD) protection for each pad is provided by circuitry that uses distributed transistors and/or diodes, represented by the circles in Figure 3. In older devices, these protection circuits are conventional diffused structures. In newer designs, Xilinx utilizes proprietary device structures which exhibit substantially enhanced ESD performance (see Table 4).

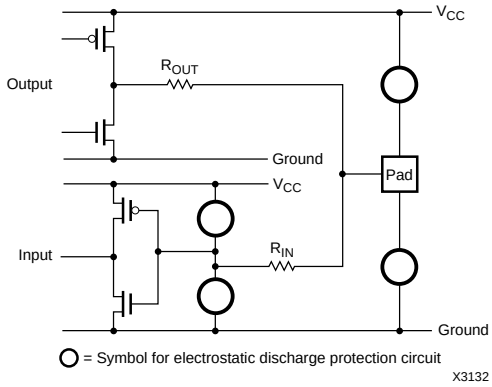

Figure 3: Input/Output Protection Circuity

Table 4: ESD Performance of Xilinx Components

Circuit Family	Human Body Model Method 3015	Machine Model EIAJ 20	Charged Device Model CDM
XC1700D	>6,000v	500– 900v	>2,000v
XC2000	1,500–2,500v	250–325v	pend
XC3000A	4,500-7,000v	325-600v	>2,000v
XC3100A	1,750-5,000v	700-800v	>2,000v
XC4000	4,000-8,000v	800-900v	>1,000v
XC4000E	4,000-8,000v	pend	>2,000v
XC4000E	4,000-6,000v	pend	>2,000v
XC5200	3,000-5,000v	pend	>2,000v
XC7000	2,000-4,000v	250-300v	>2,000v
XC9000	2,000-5,000v	pend	>2,000v

Whenever the voltage on a pad approaches a dangerous level, current flows through the protective structures to or from a power supply rail (V_{CC} or ground). In addition, the capacitances in these structures integrate the pulse to provide sufficient time for the protection networks to clamp the input, avoiding damage to the circuit being protected. Geometries and doping levels are chosen to provide ESD protection on all pads for both positive and negative voltages.

Latchup

Latchup is a condition in which parasitic bipolar transistors form a positive feedback loop (Figure 4), which quickly reaches current levels that permanently damage the device. Xilinx uses techniques based on doping levels and circuit placement to avoid this phenomenon. The beta of each parasitic transistor is minimized by increasing the base width. This is achieved with large physical spacings. The butting contacts effectively short the n+ and p+ regions for both wells, which makes the V_{BE} of each parasitic very close to zero. This also makes the parasitic transistors very hard to forward bias. Finally, each well is surrounded by a dummy collector, which forces the V_{CE} of each parasitic almost to zero and creates a structure in which the base width of each parasitic is large, thus making latchup extremely difficult to induce.

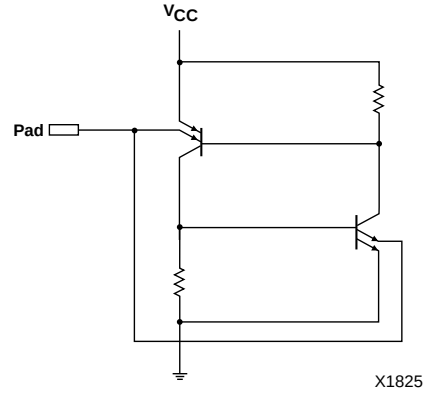

Figure 4: SCR Model

At elevated temperatures, 100 mA will not cause latchup. At room temperature, the FPGA can withstand more than 300 mA without latchup; the EPLD device can withstand more than 200 mA without latchup. However, to avoid metal-migration problems, continuous currents in excess of 10 mA are not recommended.

High Temperature Performance

Although Xilinx guarantees parts to perform only within the specifications of the data sheet, extensive high temperature life testing has been done at 145°C with excellent results.