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Xilinx FPGAs: A Technical Overview for the First-Time User

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Introduction

In the Spartan™, XC3000, XC4000, and XC5200 device families, Xilinx offers several evolutionary and compatible generations of Field Programmable Gate Arrays (FPGAs). Here is a short description of their common features.

Every Xilinx FPGA performs the function of a custom LSI circuit, such as a gate array, but the FPGA is user-programmable and even reprogrammable in the system. Xilinx sells standard off-the-shelf devices in multiple families, and many different sizes, speeds, operating-temperature ranges, and packages. The user selects the appropriate device and then converts the schematic or High-Level-Language description into a configuration data file, using the Xilinx development system software running on a PC or workstation, and then loads this file into the Xilinx FPGA.

This overview describes two aspects of Xilinx FPGAs:

- what logic resources are available to the user
- how the devices are programmed.

User Logic

Different in structure from traditional logic circuits, or PALs, EPLDs and even gate arrays, the Xilinx FPGAs implement combinatorial logic in small look-up tables (16 x 1 ROMs); each such table either feeds the D-input of a flip-flop or drives other logic or I/O. Each FPGA contains a matrix of identical logic blocks, usually square, from 8 x 8 in the XC4002XL to 68 x 68 in the XC40125XV. Metal lines of various lengths run horizontally and vertically in-between these logic blocks, selectively interconnecting them or connecting them to the input/output blocks.

Logic Blocks

This modular architecture is rich in registers and powerful function generators that can implement any function of up to five variables. For wider inputs, function generators are easily concatenated. Generous on-chip buffering makes logic block delays insensitive to loading by the interconnect structure, but interconnect delays are layout-dependent and must be analyzed if they are performance-critical.

Clocks

Clock lines are well-buffered and can drive all flip-flops with < 2 ns skew from chip corner to corner, even throughout the biggest device. The user need not worry about clock loading or clock-delay balancing, or about hold-time issues on the chip, if the designated global clock lines are used. There are eight such global low-skew clock lines in XC4000 and Spartan devices, four in XC5200 devices, and two in XC3000 devices.

Special Features

All devices can implement internal bidirectional busses. The Spartan, XC4000- and XC5200-family devices have dedicated fast carry circuits that improve the efficiency and speed of adders, subtractors, comparators, accumulators and synchronous counters. These families also support boundary scan on every pin.

Spartan and XC4000-series devices can use any of their logic-block look-up tables as distributed RAM, with synchronous write and dual-port options. This makes FIFOs, shift registers and DSP distributed multipliers very fast and efficient.

Inputs/Outputs

All device pins are available as bidirectional user I/O, with the exception of the supply connections and a few dedicated configuration pins. All inputs and outputs within each family have identical electrical characteristics, but output current capability varies among families. The outputs on XC3000 and XC5200 devices always swing rail-to-rail. Spartan and XC4000E/EX outputs have a global choice between “TTL = totem pole” or “CMOS = rail-to-rail” output swing.

The original families operate from a 5-V supply, but have added 3.3-V variants. These 3.3-V devices, designated by an “L” in their product name, have rail-to-rail outputs.

Inputs of all 5-V devices can be globally configured for either TTL-like input thresholds or mid-rail CMOS thresholds. All 3.3-V devices have CMOS input thresholds (50% of Vcc). All inputs have hysteresis (Schmitt-trigger action) of 100 to 200 mV. SpartanXL and XC4000XL inputs are unconditionally 5-V tolerant, even while their supply voltage is as low as 0 V. This eliminates all power-supply sequencing problems.

Global Reset

All Xilinx FPGAs have a global asynchronous reset input affecting all device flip-flops. In the Spartan, XC4000- and XC5200-family devices, any pin can be configured as a reset input; in XC3000-families, RESET is a dedicated pin.

Power Consumption

Since all Xilinx FPGAs use CMOS-SRAM technology, their quiescent or stand-by power consumption is very low, microwatts for XC3000 devices, max 25 mW to 75 mW for the other 5-V families. The operational power consumption is totally dynamic, proportional to the transition frequency of inputs, outputs, and internal nodes. Typical power consumption is between 100 mW and 5 W, depending on device size, clock rate, and the internal logic structure.

All devices monitor V_{CC} continuously and shut down when V_{CC} drops to 3 V (2 V for 3.3-V devices). The device then 3-states all outputs and prepares for reconfiguration.

Programming or Configuring

Design Entry

A design usually starts as a schematic, drawn with one of the popular CAE tools, or as a High-Level Language textual description. Most CAE tools have an interface to the Xilinx development system, running on PCs or workstations.

Design Implementation

After schematic- or HLL design entry, the logic is automatically converted to EDIF. The Xilinx software first partitions the design into logic blocks, then finds a near-optimal placement for each block, and finally selects the interconnect routing. This process of partitioning the logic, placing it on the chip, and routing the interconnects runs automatically, but the user may also affect the outcome by imposing specific timing constraints, or selectively editing critical portions of the design, using the graphic design editor. The user thus has a wide range of choices between a fully automatic implementation and detailed involvement in the layout process.Once the design is complete, a detailed timing report is generated and a serial bitstream can be downloaded into the FPGA, into a PROM programmer, or made available as a computer file.

Configuring the FPGA

The user then exercises one of several options to load this file into the Xilinx FPGA device, where it is stored in latches, arranged to resemble one long shift register. The data content of these latches customizes the FPGA to perform the intended digital function. The number of configuration bits varies with device type, from 14,819 bits for the smallest device (XC3020) to 2,797,040 bits for the largest device (XC40125XV). Multiple FPGA devices can be daisy-chained and configured with a common concatenated bitstream. Device utilization does not change the number of configuration bits. Inside the device, these configuration bits control or define the combinatorial circuitry, flip-flops, interconnect structure, and the I/O buffers, as well as their pull-up or pull-down resistors, input threshold and output slew rate.

Power-up Sequence

Upon power-up, the device waits for V_{CC} to reach an acceptable level, then clears the configuration memory, holds all internal flip-flops reset, and 3-states the outputs but activates their weak pull-up resistors. The device then initiates configuration, either as a master, (clocking a serial PROM to receive the serial bitstream or addressing a byte-parallel EPROM), or as a slave, (accepting a clock and bit-serial or 8-bit parallel data from an external source).

Bit-Serial Configuration

The Xilinx serial PROM is the simplest way to configure the FPGA, using only three or four device pins. Typical configuration time is around one microsecond per bit, but this can be reduced by a factor of eight. Configuration thus takes from a few milliseconds to a several hundred milliseconds. Xilinx serial PROMs come in sizes from 36K to 4M bits. Serial PROMs can also be daisy-chained to store a longer bitstream.

Byte-Parallel Configuration

Xilinx XC3000, XC4000, and XC5200 FPGA devices can also be configured with byte-wide data, either from an industry-standard PROM or from a microprocessor. The FPGA drives the PROM addresses directly, or it handshakes with the microprocessor like a typical peripheral. The byte-wide data is immediately converted into an internal serial bitstream, clocked by the internal Configuration Clock (CCLK). Parallel configuration modes are, therefore, not faster than serial modes.

Reconfiguration

The user can reconfigure the device at any time by pulling the PROGRAM pin Low, to initiate a new configuration sequence. During this process, outputs not used for configuration are 3-stated. Partial reconfiguration is not possible.For high-volume high-density applications, Xilinx offers lower-cost, fixed-programmed HardWire versions.

Readback of Configuration Data

After the device has been programmed, the content of the configuration "shift register" can be read back serially, without interfering with device operation. Spartan, XC4000- and XC5200-family devices include a synchronized simultaneous transfer of all user-register information into the configuration registers.

Quality and Reliability

Since 1985, Xilinx has shipped over 70 million FPGA devices. Industry-leading quality and reliability (ESD protection, AQL and FIT) and aggressive price reductions have undoubtedly contributed to this success.