A Quick JTAG ISP Checklist

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Summary

ISP circuitry is beneficial for fast prototype development. However, even the most robust circuitry needs minimal consideration to deliver the best in system programming results. This application brief describes a short list of considerations needed to get the best performance from your ISP designs.

Family

XC9500

Overview

Charge pumps, the heart of the XC9500 ISP circuitry require a modest amount of care. The voltages to which the pumps must rise are directly derived from the external voltage supplied to the VCCINT pins on the XC9500 parts. Because these elevated voltages must be within their prescribed values to properly program the CPLD, it is vital that they be provided with very clean (noise free) voltage within the right range. This suggests the first two key rules:

1. Make sure VCC is within the rated value: 5V +/- 5%.
2. Provide both 0.1 and 0.01 µF capacitors at every VCC point of the chip, and attached directly to the nearest ground.

JTAG specifications do require pull-up resistance to be supplied internally to the TDI and TMS pins by the chips, but no particular value is required. This lets vendors supply whatever they choose and still remain in full compliance. Because of this, very long JTAG chains or chains using parts from multiple vendors may present significant loading to the ISP drive cable. In these cases, it is wise to:

3. Use the latest Xilinx download cables. This would be Parallel Cables with serial numbers greater than 5000 or any X-Checker cable.
4. Consider including buffers on TMS or TCK signals interleaved at various points on your JTAG circuitry to account for unknown device impedance.

As more was learned about the ISP process, Xilinx JTAGProgrammer downloading software has become significantly more robust in handling ISP issues. With that in mind, it is appropriate to:

5. Always be certain to use the latest version of the Xilinx JTAGProgrammer software.

Finally, some people have noted that their designs appear to experience erase time or programming time extension as the design progresses - particularly for long chains. This is probably due to the likely fact that parts being reprogrammed will have lots of switching signals delivered into them, which is different from the initial case where a blank part is being programmed. If this occurs, there is a way to lower the noise:

6. Put the rest of the JTAG chain into HIGHZ when programming a troublesome part.

This will limit the number of additional signals presented both to the system and frequently to a troublesome part (because parts within a given chain tend to be connected amongst themselves). The main detail to accomplish step 6 is simply to select the HIGHZ option from the JTAGProgrammer preferences selection dialog.

7. If free running clocks are delivered into the ISP CPLD, it may be necessary to disconnect or disable their entry into the CPLD while programming.

This is best accomplished by using the commercially available clock generation chips that permit electrical disabling of the clock output. This seldom occurs, but advanced planning makes it painless.

Checklist

- ❑ Make sure VCC is within the rated value: 5V +/- 5%.
- ❑ Provide both 0.1 and 0.01 µF capacitors at every VCC point of the chip, and attached directly to the nearest ground.
- ❑ Use the latest Xilinx download cables. This would be a Parallel Cable with serial numbers greater than 5000 or any X-Checker cable.
- ❑ Consider including buffers on TCK and TMS interleaved at various points on your JTAG circuitry to account for unknown device impedance.
- ❑ Always be certain to use the latest version of the Xilinx JTAGProgrammer Software.
- ❑ Put the rest of the JTAG chain into HIGHZ when programming a troublesome part.
- ❑ If free running clocks are delivered into the ISP CPLD, it may be necessary to disconnect or disable their entry into the CPLD while programming.