Supply-Voltage Migration, 5V to 3.3V

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For the past 30 years, 5 V has been the standard supply voltage for digital circuits. It was born as the best compromise between processing capabilities, bipolar circuit requirements, power consumption, and required system noise immunity. When CMOS gradually supplanted LS-TTL in the 1980s, it adopted this popular supply voltage, as well as the standard 5 V logic level definitions (V_{OH}=2.4 V min, V_{OL}=0.4 V max, V_{IH}=2.0 V min, V_{IL}=0.8 V max) despite the fact that these definitions were dictated by bipolar TTL circuit considerations and did not naturally apply to the more symmetrical CMOS structure.

The relentless pressure to achieve higher speed, higher density, lower cost and lower power consumption is driving CMOS IC manufacturers to ever-thinner gate oxides and smaller geometries, from 2µ in the early 1980s, to 0.8µ in 1990, and since then to 0.6µ, 0.5µ, and now, 0.35µ and even 0.25µ, with 0.18µ expected next year. The whole industry, from designers and manufacturers to users, benefits from this rapid process migration, but it comes at a price: The power supply voltage must be changed (see Figure 1).

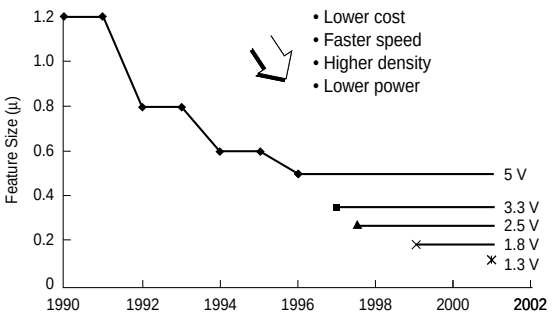

Figure 1: Process Technology & Supply Voltage

At 0.35µ, CMOS circuits do not reliably tolerate a 5 V supply voltage. Instead, they must move to the next lower standard of 3.3 V. Similarly, at 0.25µ, the supply voltage must be lowered again to 2.5 V, and 0.18µ technology will probably require 1.8 V. (Note this accidentally very simple numeric relationship between minimum geometries and maximum supply voltage).

The lower supply voltage brings the benefit of lower power consumption, proportional to the square of the supply voltage. Thus, compared to 5 V, a circuit running from 3.3 V consumes half the power, and a circuit running from 2.5 V consumes only a quarter of the power. This is a welcome reprieve from the unavoidable power increase and associated thermal problems caused by higher circuit complexity and ever faster clock rates.

The user who wants to take advantage of the technical and economic benefits of smaller process geometries faces several new issues:

- How to generate and distribute multiple supply voltages on the PC board
- How to interface between CMOS devices with different supply voltages
- How to cope with supply-voltage sequencing.

Distributing Multiple Supply Voltages on the Board

At today's circuit speeds, the PC-board and its analog characteristics play a strong, if not dominating, role in determining digital system performance. Even modest-length (3 inch) interconnects must be treated as transmission lines, and ground- and V_{CC} planes must be kept reasonably free from synchronous and asynchronous voltage transients.

The designer must pay attention to each signal path, including the complete current loop, from the positive supply connection, through the IC and interconnects, back to ground distribution, and through the decoupling capacitors back to the positive supply terminal.

Modern designs require PC boards with at least four layers, and usually more. At least one inner layer must be dedicated as a ground plane and must be kept as undisturbed as possible. Any major hole in the ground plane would force the ground current to take detours, which increases the inductance and causes ground-voltage spikes. In simple designs, 5 V and 3.3 V can share a common power plane; however, the 3.3 V distribution requires greater attention, since it affects the signal-noise margin more than does noise on the 5-V plane.

The 3.3 V supply can either be brought in from off-board, or it can be generated by an on-board 5-V-to-3.3-V DC-to-DC converter. This latter method has been pioneered and proven by the PentiumPro, with very compact and inexpensive switchers for up to 12 A now available from many manufacturers (NSC, Linear, Maxim, Cherry and traditional power supply houses).

Also, low-impedance ceramic decoupling capacitors are needed to supply the dynamically changing I_{CC} inside the chip, and to provide a return path for external current

changes. These instantaneous current peaks are much higher than the average dc current, which is typically between 100 mA and 2 A for the larger FPGA devices.

To demonstrate the importance of good V_{CC} decoupling, let's assume the example of a synchronous, single 40-MHz clock design consuming 1 A. Most of the current flow will be in the first 5 ns of the 25 ns clock period. This 5 A peak current must be supplied by the sum of the decoupling capacitors. In this example, 5 A times 5 ns creates a 250 mV drop on a 0.1 µF decoupling capacitance. That is, at best, borderline acceptable.

Here are some solutions. First, decoupling capacitors must have very low inductance and series resistance. The total capacitance value is less important, as long as it exceeds 0.1 µF. The best way to achieve low impedance at gigahertz speeds is to use multiple capacitors in parallel. Use 0.01 to 0.1 µF ceramic capacitors, mounted very close to each V_{CC} pin and directly connected to the ground plane.

Second, keep the lines very short. A 0.25 inch (6 mm) long narrow trace represents an inductance of 20 nH. A current transient of 100 mA/ns causes a voltage drop of 2 V across this inductance, which is of course unacceptable.

Some board manufacturers also elect to use an extremely thin (down to 2 mils or 0.05 mm) dielectric layer between the ground and V_{CC} planes to achieve excellent distributed decoupling capacitance.

Ground Bounce

Ground bounce describes the dynamic voltage difference between the on-chip ground and the system ground plane, caused by current changes in the chip-to-package bonding wire and the lead frame inductance. In the best of cases, this inductance is as low as 3 to 5 nH. Fast output current changes cause the chip-internal ground to bounce up and down with respect to the system ground plane. Ground bounce becomes a serious problem when many outputs change simultaneously, at a fast slew rate, and in the same direction. 32-bit address/data busses are a notorious example. The ground-bounce problem might get slightly relieved at 3.3 V, since the output swing is reduced from 5 V, while the input threshold, and thus noise immunity, is unchanged from the typical 5-V logic with its TTL-like inputs.

Luckily, synchronous single-clock systems tolerate surprising amounts of ground bounce: The disturbing output transitions occur a few nanoseconds after the active clock edge, but data inputs are sampled a few nanoseconds before the next active clock edge, well after the ground bounce has settled, usually in about 5 ns. As long as the ground or V_{CC} changes do not directly upset internal flip-flops, and as long as all asynchronous inputs, including clocks, have good noise margins, ground bounce looks more scary than it really is, but it must remain a concern for all system designers.

To minimize ground bounce, cross-talk and other external noise, Xilinx provides a slew-rate-limited output option, individually programmable for each pin, so that the user can slow down the transition rate on all uncritical outputs.

Supply current values will become critical for large chips that are clocked at high rates. In such, often heavily pipelined, designs, the user will be tempted to run the chips up to their thermal limits, perhaps with a glued-on or clipped-on heatsink and even a built-in small fan. PentiumPro and DEC Alpha CPUs already dissipate 15 to 30 W at dc currents of 6 to 12 A, with significantly higher transient currents supplied by the decoupling capacitors. At a given upper limit of practical power dissipation, lower V_{CC} will mean higher currents, requiring more demanding V_{CC} distribution and decoupling methods. Electro-magnetic interference (EMI) will be another concern, and a reason for designers to brush up on their high-frequency analog skills.

Recommended reading: *High-Speed Digital Design, a Handbook of Black Magic.* by H. Johnson and M. Graham, 1993 Prentice Hall.

Interfacing Between Devices with Different Supply Voltages

Since all supply voltages share a common ground, there are no problems interfacing logic at low levels in either direction. All potential problems are in interfacing logic at high levels (see Figure 2). For example:

- 3.3 V logic High driving a 5-V input:

There is no problem when the 5-V device has a so-called “TTL-level” input threshold of ~1.3 V. This is true for most CMOS devices. The driving 3.3-V output High level is close to V_{CC}, and thus well above the required V_{IH} of 2.0 V.

- 5-V logic High driving 3.3-V input:

In most cases, the high 5-V output voltage will force excessive current into the 3.3 V input. The pins on older Xilinx 3.3 V FPGAs and on most other manufacturers' 3.3-V devices have a clamp diode between each pin and V_{CC} to protect the circuit against electrostatic discharge (ESD). This diode starts conducting when the pin is driven more than 0.7 V positive with respect to its V_{CC}. This diode presents a problem in mixed-voltage systems, since it clamps whenever a 5-V logic High is driven to a 3.3 V input.

Xilinx has overcome this difficulty by eliminating the clamp diode between the pin and V_{CC} in the circuit structure of the Xilinx XC4000XL family. The pin can thus be driven as High as 5.5 V – irrespective of the actual supply voltage on the receiving input. These devices are,

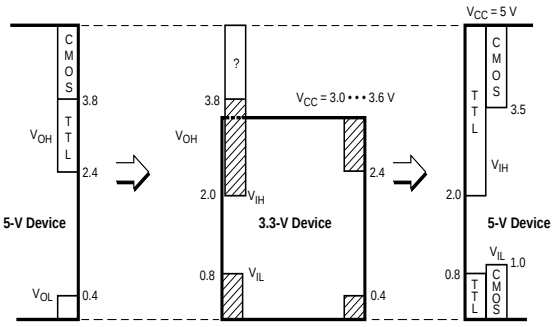

Figure 2: Interface Levels

therefore, unconditionally 5-V tolerant, and the user can ignore all interface precautions. Excellent ESD protection (up to several thousand volts) is achieved by means of a patented diode-transistor structure that does not connect to V_{CC}. From a design perspective, it is important to remember that directly connecting an active High 5-V CMOS output to an active High 3.3 V output creates contention and must be avoided.

When mixed voltage inputs are being driven from a “TTL-level” output with an n-channel pull-up transistor – available as an option on all XC4000 and XC4000E devices – then the input current is naturally limited to less than a few mA, even when the 5 V supply is at 5.25 V while the 3.3 V supply is at 3.0 V, a very unlikely combination. At nominal supply voltage levels, the current is ~ 1 microamp. This interface poses no problems.

When such non-5-V-tolerant inputs are driven from a “CMOS-level” complementary, rail-to-rail output, the user must somehow limit the current. A 1 kilohm resistor limits the current to less than 2 mA, but causes a slight speed penalty (1 kilohm x 35 pF = 35 ns)

- 3.3 V logic High driving a “CMOS threshold” 5-V input:

This interface situation should be avoided. An active High 3.3-V output cannot be pulled higher, since the internal pull-up transistor represents a ~50 Ω impedance for current in either direction. A pull-up resistor to 5 V is therefore meaningless. If the internal pull-up transistor is disabled (“open drain output”) the pin can be pulled higher, until the ESD clamp becomes conductive. The outputs on XC4000XL devices can thus be configured as open drain, and an extend resistor can pull them all the way to 5 V, albeit with an RC speed penalty.

XC4000XL I/O

The XC4000XL-family I/O is designed to be PCI compliant and also to be 5-V tolerant. PCI compliance requires a clamping diode to V_{CC}.

5-V tolerance, on the other hand, does not permit such a diode. It thus requires that the n-well of the p-channel output transistor not be tied to the 3.3 V V_{CC}, since the parasitic diode would prevent the I/O pin from going substantially more positive than 3.3 V.

To satisfy these conflicting requirements, an internal diode is added to each output, with its cathode connected to an internal V_{TT} rail. For PCI compliance, this rail must be connected externally to the appropriate V_{CC} supply (5 V or 3.3 V). For 5-V tolerance, the V_{TT} rail is left floating (see Figure 3).

Since the XC4000XL devices do not have a diode between the n-well of the p-channel output transistor and the chip V_{CC} pin, Electro-Static Discharge protection against positive going voltage spikes is provided by dedicated special bipolar circuits that are turned on by junction breakdown >7 V.

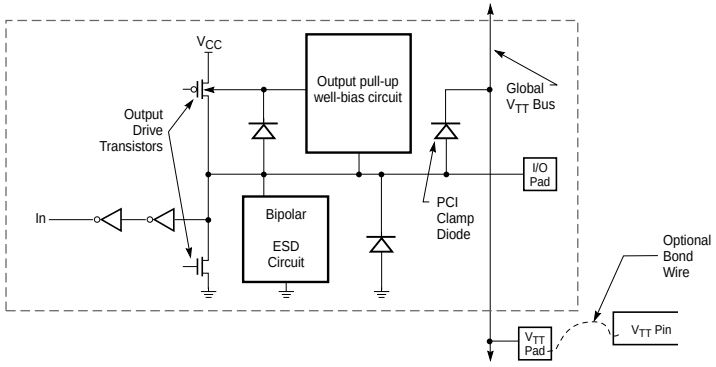

Figure 3: XC4000XL I/O

Supply-Voltage Sequencing

Any system with more than one supply voltage faces the possibility of these voltages being applied in an undefined or uncontrolled sequence. For most ICs, this means the designer must calculate the maximum current potentially flowing into the pins of the unpowered device. The current value depends on the powered-up device's output structure (complementary outputs drive the highest current) and on the voltage compliance (impedance) of the unpowered V_{CC} distribution net. If it is held rigidly to ground, the undesired current will be high. If the unpowered V_{CC} can easily be pulled High, the current will be far less. Most inputs will tolerate 50 mA for a few seconds, and 10 mA for unlimited time. For significantly higher currents there might be the short-term risk of latch-up, and the long-term risk of metal migration if the high current persists for thousands of hours.

The Xilinx XC4000XL family is 5-V tolerant, even when V_{CC} is zero. These devices, therefore, have no problem with arbitrary power sequencing or even with “hot plug-in”. When 5V is applied first, there is no current into the Xilinx FPGAs. When 3.3 V is applied first, the device outputs can be kept three-stated by connecting the 5-V V_{CC} line as an active-Low Global three-state input to the 3.3-V devices, again eliminating any undesirable current.

Migration from 5-V Designs to 3.3-V Designs

Xilinx 3.3-V FPGAs are functionally and pin-out compatible with their 5-V equivalents. The user can thus start a design using 5 V supplies, later plugging in the 3.3-V equivalent devices without any concern about functionality, speed, pin locations or even logic levels. The only required accommodation is that the PC-board must accept the V_{CC} change-over and perhaps the additional voltage regulator or switcher. Mixed 5-V/3.3-V systems will be common for several years to come, so it is important to give the user the maximum amount of freedom and cause the least amount of rework when migrating to the lower supply voltages of the future.

Within a year after the change to 3.3 V comes 2.5 V. This change will be less traumatic since most FPGA suppliers will - at least originally - use 2.5 V only for the internal logic core, while running the I/O from 3.3 V (see Figure 4). The user must provide the additional V_{CC}, distribute and decouple it appropriately, but need not be concerned about signal level incompatibilities. Most suppliers will increase the number of V_{CC} and perhaps also ground pins, and the user might want to plan ahead and leave these designated pins unused in the 3.3 V design. All in all, the transition to 2.5 V will be easier than the earlier change to 3.3 V.

After 2.5 V comes 1.8 V, but it is too early to give detailed directions for that transition. 1.8 V logic will not directly interface with 5-V logic. The industry is planning to accommodate direct interfacing between three successive generations: 5 V - 3.3 V - 2.5 V, or 3.3 V - 2.5 V - 1.8 V.

Conclusion

New improvements in IC technology enable a wealth of new, smaller systems with higher performance and lower power requirements. To take advantage of these improvements, designers must provide new supply voltages, 3.3 V now and 2.5 V in the near future. In many cases, these new voltages must be applied side-by-side with older, 5 V parts. These mixed-voltage environments could create a variety of design challenges, especially when using FPGAs that are not specifically designed to operate in mixed-voltage environments. The new 3.3-V and 2.5-V Xilinx FPGA families are immune to all power sequencing problems and can be interfaced directly with older-technology 5-V devices, making them an ideal solution for many mixed-voltage systems.

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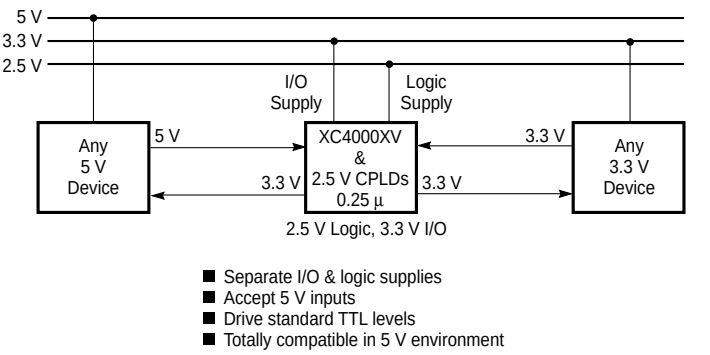

Figure 4: Xilinx PLDs