The XC4000XV:

Introducing The Industry's First 500K Gate FPGA Family

The new XC4000XV FPGA family delivers densities up to 500,000 system gates (20,000 logic cells). This new family includes four devices, offering system performance greater than 100 MHz, and featuring 2.5-volt internal operation with 3.3-volt I/Os to allow optimum performance and compatibility with existing voltage standards.

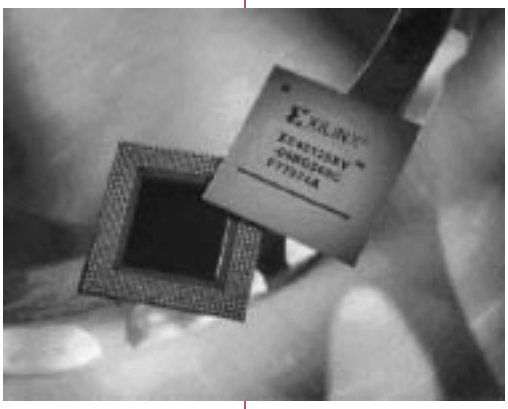
"We announced our five-year roadmap last January, which clearly defined our plans to provide higher-density FPGA families on advanced processes. In the course of six months, we have delivered ten members of the XC4000XL family of high-density and high-performance FPGAs. These are widely accepted by customers as leaders in density and performance," said Wim Roelandts, Xilinx president and chief executive officer. "With our migration to a 0.25-micron process, the XC4000XV FPGA family represents our next leadership step to bring the benefits of FPGA reconfigurability and time-to-market advantages to traditional ASIC users who demand high-performance and high-density logic."

Delivering ASIC Performance and Density, Today

Digital designers who have traditionally used custom ASIC devices are now considering the time-to-market benefits that Xilinx high-density, high-performance FPGAs can offer. According to Jordan Selburn, principal analyst at Dataquest, the Xilinx XC4000XV family, in conjunction with the Xilinx HardWire ASIC capability, can address approximately 45 percent of the 1997 gate-array design starts, based on the XC4000XV maximum performance and density levels.

Vincent Coli, director of product marketing at Aptix, the leader in reconfigurable system prototyping solutions, says "We use Xilinx for their density because it's here today. Our customers are demanding several million gates of programmable logic in our most advanced product, the System Explorer. By using the XC40125XV, the highest density programmable logic device available today, we are able to achieve these density levels."

Architectural Advantages of The XC4000X Series



The XC4000XV family is a more advanced implementation of our XC4000EX/XL architecture, which uses segmented routing and distributed RAM. These features make an ideal platform for implementing cores. For example, our segmented routing architecture allows predictable performance regardless of device size or how much logic is employed. With the non-segmented routing used by our competitors, cores will slow down unpredictably as surrounding logic is added or when designs are moved to larger devices. Our performance predictability is a requirement for designs using intellectual property (cores) because you want to choose cores independently of device density, and you expect the core's performance to remain the same as the design evolves. In addition, due to footprint-compatibility advantages, current XC4000XL customers can easily and immediately upgrade to our higher-density XC4000XV products. ◆

The XC4000XV Family

Device	Logic Cells	System Gates	Available
XC40125XV	10,982	80,000 - 265,000	now
XC40150XV	12,312	100,000 - 300,000	Q198
XC40200XV	16,758	130,000 - 400,000	1H98
XC40250XV	20,102	180,000 - 500,000	1H98