How to Design Today for the Upcoming Spartan-XL FPGA Family

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Summary

This application note explains how to design a prototype for a Spartan-XL FPGA today. By following the design guidelines presented in this note, such a prototype can easily be converted to using a Spartan-XL device, once the new family becomes available.

Xilinx Families

Spartan-XL family

Introduction

The new Spartan series is composed of two low cost, high performance FPGA families: the Spartan family which uses a 5.0 V supply and the Spartan-XL family which uses a 3.3 V supply. Recent advancements in CMOS technology together with a streamlined feature set make it possible for Spartan devices to achieve unprecedented levels of performance at lower cost than ever before. The Spartan series shares many functional traits with the XC4000 series upon whose architecture it is based. Five different densities are available ranging from 5,000 to 40,000 system gates.

Xilinx offers the ability of developing prototypes for the upcoming Spartan-XL devices using pin-compatible devices. When parts do become available, such designs will be able to take quick advantage of the low cost, low power and high performance benefits that only Spartan-XL devices can deliver.

Depending on what power supplies are available to the prototype board, there are two basic design strategies. If both 3.3 V and 5.0 V supplies are available, then it is possible to use a Spartan device (presently available) for an early prototype, later to replace it with a Spartan-XL device of the same density for the final design. The speed files may differ slightly between the Spartan device and the equivalent Spartan-XL device; therefore, the design must be re-run with Spartan-XL speed files when available. The corresponding members of the two Spartan families are compatible with respect to logic, routing, function, and pin-out. A jumper determines which of the two supplies must feed the FPGA's V_{CC} pins.

How to carry out the design with only a 3.3 V supply is the object of this application note. For this case, the guidelines set forth below show how a design can easily be prepared to accept a Spartan-XL device by first preparing a prototype for an XC4000XL device of comparable density.

Spartan-XL and XC4000XL

To begin a Spartan-XL design using an XC4000XL prototype, one must first understand the differences between the two FPGA families. Then one can create a design whose proper operation depends only on the features, logical functioning, timing, packages, pinouts and software conventions the two families hold in common. Only in this way can compatibility be ensured. The discussion that follows describes the differences between the Spartan-XL and the XC4000XL families. It also explains how the designer can use this information to maintain compatibility while changing to a Spartan-XL design from an XC4000XL prototype.

Package Compatibility

Once a particular Spartan-XL device has been chosen for the final design, then it should be matched to an XC4000XL device of comparable density for prototype purposes. In Table 1, each member of the Spartan-XL family (left column) is shown along with its maximum CLB and usable I/O count. For each Spartan-XL device, the table recommends the XC4000XL device (fourth column from the left) most suitable for prototype development. The XC4000XL entry is accompanied by its maximum CLB and usable I/O count. The column furthest to the right shows packages with pin configurations common to each matched pair of devices. To ensure pin-compatibility for a given match, one of the corresponding package types listed in the table must be used.

The PQ208 package requires special consideration. The PQ208 pin-out for the XCS20XL, XCS30XL and XCS40XL is different from that for the corresponding XC4000XL devices. It is, however, the same as that for the corresponding Spartan devices. If a 5.0 V supply is available, use the equivalent Spartan device as a pin-compatible prototype. This method is described in the section entitled "Introduction".

Table 1: Package Compatibility

Spartan-XL (Production)			XC4000XL (Prototype)			Common Package
Part No.	**Total CLBs**	**Usable I/O**	**Part No.**	**Total CLBs**	**Usable I/O**	
XCS05XL	100	61	XC4005XL[1]	196	61	PC84
		77			77	VQ100
XCS10XL	196	61	XC4005XL	196	61	PC84
		77			77	VQ100
		112			112	TQ144
XCS20XL	400	113	XC4010XL	400	113	TQ144
XCS30XL	576	192	XC4013XL	576	192	PQ240
		192			192	BG256
		113			113	TQ144 (HT144[2])
XCS40XL	784	193	XC4020XL	784	193	PQ240
		205			205	BG256

Note: 1. There is no closer XC4000XL match for the density of the XCS05XL than the XC4005XL.
2. The TQ144 package for the XCS30XL package and the HT144 package for the XC4013XL are pin-compatible.

If no 5.0 V supply is available, then the only other alternative for achieving plug-in compatibility at present is to choose another package, one of those listed in Table 1

The new PQ208 pin configuration will offer eight additional V_{CC} pins on the XCS20XL, XCS30XL and XCS40XL as well as nine additional user I/Os on the XCS30XL and XCS40XL. More information on how to achieve PQ208 package compatibility will be provided in a future version of this application note.

Choosing a Speed Grade

Matching the speed grade of an XC4000XL device to its replacement Spartan device deserves careful attention, especially since the speed grades are assigned to the two device types in different ways. For the XC4000XL, the slowest speed grade is -3 (i.e. “dash-three”). From here, the number decreases to -1 and lower. For Spartan-XL, the slowest speed grade is -3, from which point the number increases to -4, the fastest speed grade.

In order to make sure that the Spartan-XL device used in the final design will be able to meet the original AC timing requirements demanded of the XC4000XL prototype, design to an XC4000XL speed file that is one grade slower than the Spartan speed file. (By doing so, all AC parameters for the Spartan-XL device will be faster than the corresponding ones for the XC4000XL device). Recommended speed grade matches are shown in Table 2. Note that the two speed grades are not equivalent. The speed grade match provides sufficient slack to negotiate any differences between the two devices’ timing.

If the design will ultimately use a -3 Spartan-XL device, then the initial prototype should start with a -3 XC4000XL device. If the final device is a -4 Spartan-XL, then use a -2 XC4000XL device for prototype development.

Table 2: Recommended Speed Grades

	Spartan-XL (Production, faster grade)	XC4000XL (Prototype, slower grade)
Speed Grade	-3	-3
	-4	-2

Note: 1. This table shows the de-rated XC4000XL speed grades needed for Spartan-XL.

Configuration

Whereas the XC4000XL uses three mode pins, M0, M1, and M2, to select one of seven different configuration modes, the Spartan series has only one such pin called MODE. This pin chooses between two different configuration modes: Slave Serial (High) and Master Serial (Low). These two modes are common to both device families. The prototype design must use either one of these or a third method, configuration via the JTAG port (also common to both device families). Note that a serial daisy chain, formed of a master device and other slave devices connected in a serial chain, is an acceptable configuration technique for the prototype under discussion.

The Spartan MODE pin is at the same pin location as the XC4000XL’s M0 input. The pin locations for the M1 and M2 signals on the XC4000XL are designated “Don’t Connect” on the Spartan device. Figure 1 shows how to connect the mode pins on the XC4000XL in such a way as to facilitate replacement with the Spartan-XL device. On the XC4000XL, either GND, for Master Serial mode, or V_{CC}, for Slave Serial mode, is applied via external resistors to all three mode pins. The recommended value for the external resistors is 3.3 kΩ.

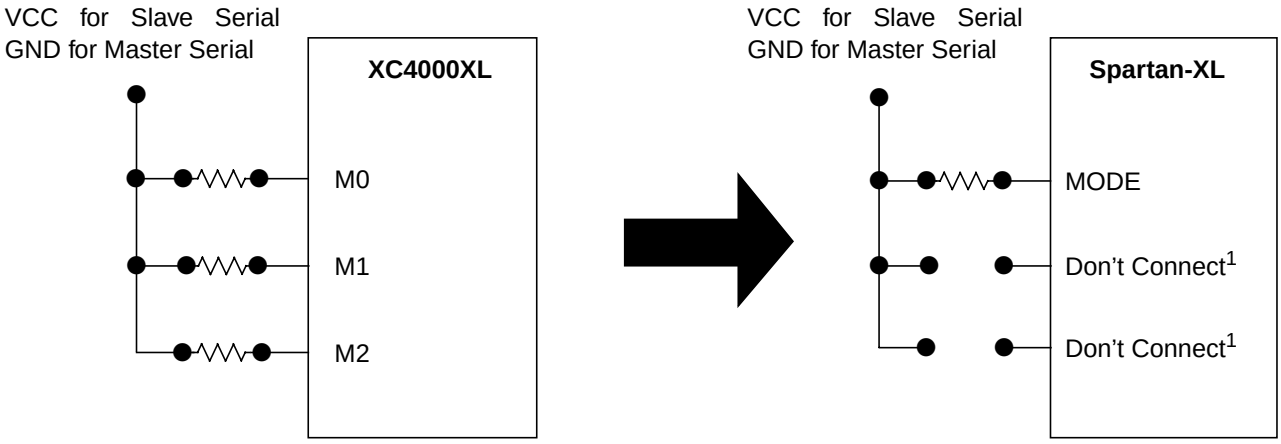

Figure 1: Connecting the Mode Pins

Note: 1. The two pins with the "Don't Connect" designation are reserved for Xilinx testing and future Spartan enhancements.

Regardless of which configuration mode is chosen, the MODE input on the Spartan device must be driven at the same level (GND or V_{CC}) as the three mode inputs on the XC4000XL device. When making the transition to the Spartan-XL device, the resistors that were connected to M1 and M2 are removed so that the two Don't Connect pins on the Spartan device will be open.

Note that since all mode inputs for both device types have weak on-chip pull-up resistors (as high as 100 kΩ) during configuration, they can be left open to select Slave Serial mode.

Following configuration of the XC4000XL, M0 and M2 can be used as inputs and M1 can be used as a 3-state output; however, the designer must avoid these options, since they are not possible on the Spartan-XL. Do not use the pad symbols MD0, MD1, and MD2.

Wired-AND Logic

On the XC4000XL, the 3-state buffers driving the internal horizontal longlines can be configured to perform three functions: (1) a standard 3-state buffer or (2) wired-AND function or (3) a wired-OR-AND function. The two last open-drain functions are not permitted on the Spartan-XL devices. Therefore, to achieve the compatibility necessary for prototype conversion, one must avoid designing with wired-AND and wired-OR logic. Use neither the WANDx nor the WOR2AND symbol.

Wide-Edge Decoders

Spartan devices do not have wide-edge decoder capability. The designer must not use this XC4000XL feature. Avoid using DECODEx as well as WAND with the DECODE attribute.

Implementing Memory

Both the XC4000XL and Spartan families support synchronous single-port and dual-port RAM in addition to ROM. It is acceptable to use any of these features. However, the level-sensitive (asynchronous) RAM feature, not available on the Spartan-XL, should be avoided. Do not instantiate symbols denoting level-sensitive RAM (i.e. RAM16X1, RAM32X1, etc.); however, other library symbols for memory (i.e. RAM16X1S, RAM16X1D, ROM32X1, etc.) are acceptable.

Other XC4000XL Caveats

Aside from what has already been described, the XC4000XL family provides still other features not available with the Spartan-XL family. The designer must avoid the features described below:

1. Global Early Buffer (BUFGE).
2. Fast-Capture Latches in the IOBs (ILFFX and ILFLX).
3. Output multiplexer and two-input function generator in the IOBs (OMUX2, OAND2, etc.).
4. Latch in the CLBs (LD, LDC, etc.).

Design Fit and FPGA Utilization

The Spartan-XL design can be implemented using the current development software to check the fit of a design into a Spartan device target. If successful, then the design can be run in the XC4000XL device. Since corresponding members of the two Spartan families have identical logic and routing resources, if the design fits into a Spartan device, then it will also fit into the related Spartan-XL device. This implementation process includes a Design Rule Check (DRC) that prevents the use of architectural features not supported by the Spartan series.

If the designer's version of the Xilinx development software does not support the Spartan family, an alternative way to ensure a good fit for both a Spartan-XL device and an XC4000XL device is to keep the utilization of the XC4000XL device's logic resources (in terms of CLBs and IOBs) under 80% of the Spartan-XL device's total available

logic resources. This is important since a given XC4000XL device has more routing resources than a Spartan-XL device of comparable density.

As an example of the calculation, recall from Table 1 on page 2, that an XCS05XL design should use the XC4005XL for prototype purposes. Though the XC4005XL has considerably more logic resources than the XCS05XL, of the available XC4000XL devices, it comes closest to the density of the Spartan-XL device.

Assuming use of the VQ100 package, the XCS05XL has 100 CLBs and 77 usable IOBs. (This number comes from Table 1.) Therefore, the initial XC4005XL design should not use more than 0.8 x 100 = 80 CLBs and 0.80 x 77 = 61 IOBs, even though it has a total of 196 CLBs and 77 usable IOBs available.

Implementation Flow

Using Xilinx development software that supports the Spartan family, any design destined for a Spartan-XL device must be able to place and route successfully when the corresponding Spartan device is selected for implementation. In addition to this test, the design must also be able to place and route successfully when the XC4000XL device is selected for implementation.

The entire implementation procedure for the XC4000XL prototype is shown in Figure 2. First, implement the design, without constraints, for the Spartan equivalent of the Spartan-XL device that will actually be used. If that implementation is "successful", that is, when the design meets all timing constraints, fits into the device and produces a working pinout, then lock down the pin assignments and implement the design again, this time, for the XC4000XL. At this point, a successful result can be used to configure the XC4000XL. If timing needs are not met, the design will need to be re-run with tighter timing constraints.

If, at any step along the way, the implementation fails the criteria for success, consider the following strategies for "corrective action":

1. Make sure all compatibility guidelines are met.
2. Adjust timing constraints.
3. Change design to demand less routing and logic resources.
4. Select a larger Spartan-XL/XC4000XL device combination.

Following corrective action, return to the beginning of the procedural flow and try again.

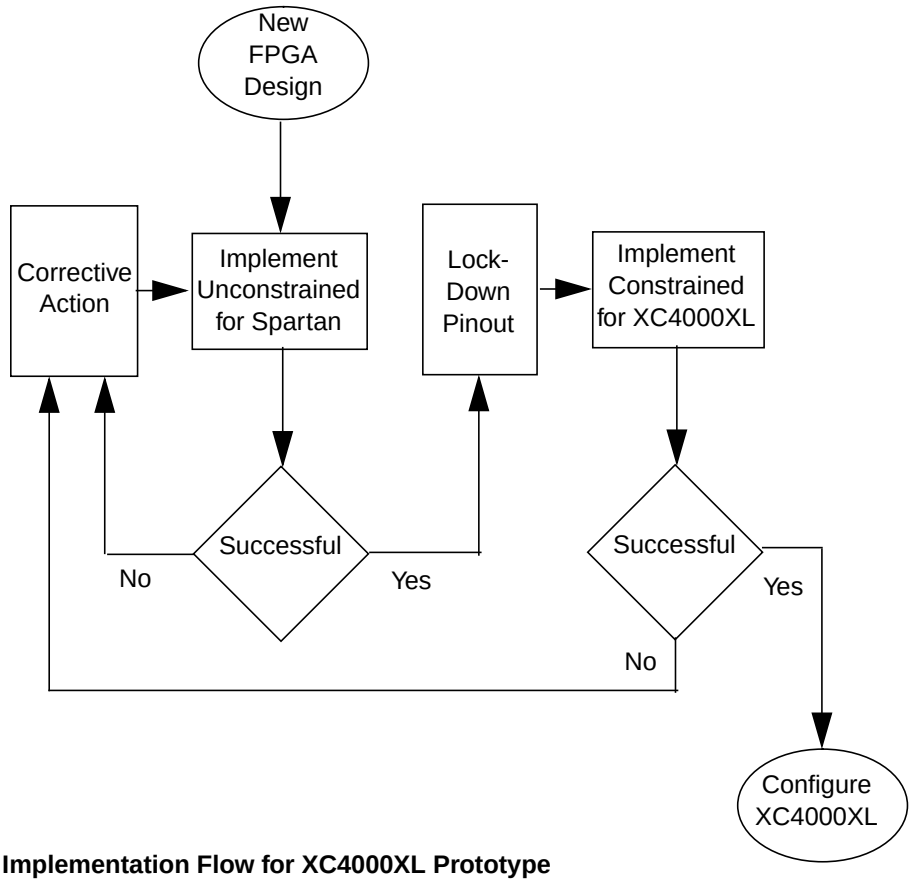

Figure 2: Design Implementation Flow for XC4000XL Prototype

Conclusion

Xilinx offers the advantage of using pin-compatible families to develop prototypes for new devices until they become available. In this way, it is possible to design for Spartan-XL today using the XC4000XL family for an early prototype. The salient issues discussed in this note include how to connect the mode pins, what features should (or should not) be used, how to implement the design as well as how to select the appropriate device, package and speed grade. Following the recommended guidelines helps make the transition from an XC4000XL prototype to a final Spartan-XL design both straightforward and reliable.

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