I/O Characteristics of the XC4000XL/XV and Spartan XL Families

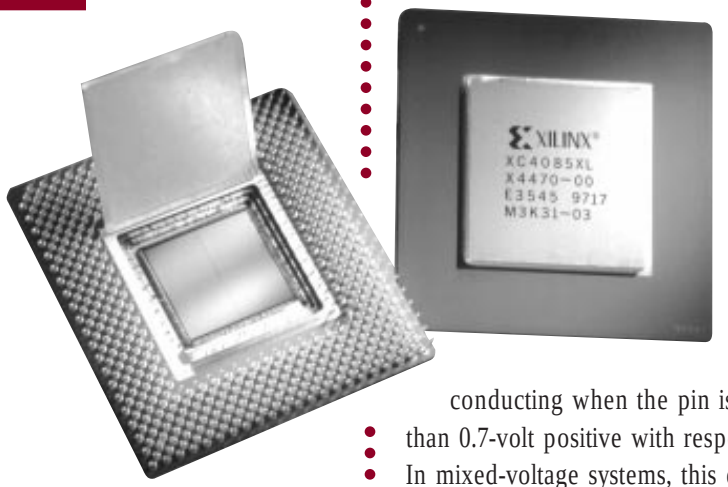
By Peter Alfke

This article describes the electrical input and output characteristics of our new 3.3-volt device families. Input thresholds and 5-volt tolerance are described, the output source and sink impedances are listed, and the effect of additional capacitive loading on delays, rise-times, and fall-times is explained.

Inputs

Input threshold is stable over temperature, but proportional to Vcc: 37-38 percent of Vcc for the falling threshold, 39-42 percent for the rising threshold. And, there is 50-150 mV of hysteresis, smallest at hot and high Vcc, largest at cold and low Vcc.

Many systems will still use a mixture of older 5-volt devices and newer 3.3-volt devices. This can pose a problem when a 5-volt logic High drives a 3.3-volt input. On most CMOS ICs, each signal pin has a clamp diode to Vcc to protect the circuit against electrostatic discharge (ESD). This diode starts conducting when the pin is driven more than 0.7-volt positive with respect to its Vcc. In mixed-voltage systems, this diode presents a problem, because it might conduct tens of milliamps whenever a 5-volt logic High is connected to a 3.3-volt input.



In the XC4000XL/XV and Spartan XL devices, Xilinx has overcome this difficulty by eliminating the clamp diode between the device pins and Vcc. The pins can thus be driven as High as 5.5 volts, irrespective of the actual supply voltage on the receiving input. These devices are therefore unconditionally 5-volt tolerant; you can ignore all interface precautions, and need not worry about power sequencing.

Excellent ESD protection (up to several thousand volts) is achieved by means of a patented diode-transistor structure that connects to ground, and not to Vcc. The structure behaves like a Zener diode; it becomes conductive at greater than six volts and diverts the charge or current directly to ground. It can handle current spikes of several hundred milliamps, but continuous current must be kept below 20 mA to avoid reliability problems caused by on-chip metal migration.

For more information, see our application note: XAPP080 "Supply-Voltage Migration, 5 V to 3.3 V."

PCI-Compliance

The Xilinx 'XL I/O structure is designed to be PCI compliant and also 5-volt tolerant. PCI compliance requires a clamping diode to Vcc. On the other hand, 5-volt tolerance does not permit such a diode. Therefore, the n-well of

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the p-channel output transistor must not be tied to the 3.3-volt Vcc because the parasitic diode would prevent the I/O pin from going substantially more positive than 3.3 volts. To satisfy these conflicting requirements, an internal diode is added to each output, with its cathode connected to an internal Vtt rail.

In the PCI-compliant XC4000XLT devices, the Vtt rail is internally connected to eight device pins which externally must be connected to the appropriate Vcc supply (5-volt or 3.3-volt). In all other 'XL devices, the Vtt rail is internally left unconnected, thus assuring 5-volt tolerance.

Output Source and Sink Capability:

The strength of the pull-down transistor (sink capability) and the pull-up transistor (source capability) are shown below. Close to either rail, the outputs are resistive, which means the voltage is proportional to current.

The table below shows the condensed IBIS information expressed as output resistance in ohms, for a sink voltage less than one volt above ground, and a source voltage less than one volt below Vcc. IBIS gives minimum and maximum current values, converted here to min and max resistor values. This data is based on SPICE simulation.

Device Family	Sink Resistance to GND (ohms)		Source Resistance to Vcc (ohms)	
	min	max	min	max
XC4000E	22.1	27.7	53.3	60.5
XC4000EX	14.4	18.8	48.1	58.7
XC4000XL/XV SpartanXL	14.4	20.5	28.0	41.0

"These results are consistent with the IBIS-derived output impedance."

Effect of Additional Capacitive Loading on Transition Times and Delays

- **Transition Time:** At the specified 50 pF external load, the rise time is 2.4 ns, and the fall time is 2.0 ns. For additional capacitive loads, add 60 ps/pF to the rise time, and 40 ps/pF to the fall time.
- **Delay:** Add 30 ps/pF to the rising-edge delay at 3 volts, add 23 ps/pF at 3.6 volts. Add 25 ps/pF to the falling-edge delay at any supply voltage. These values were derived from measurements using the fast output option, but the slew-rate limited output option behaves almost identically.

These results are consistent with the IBIS-derived output impedance, because the delay increases with approximately one RC time constant, and the rise and fall times increase with approximately two time constants. These are not guaranteed and tested parameters; they were established by sampling a few devices. Therefore, we suggest that you add a 20 percent guardband (multiply by 1.2) when calculating additional delay due to capacitive loading above the guaranteed test limit of 50 pF.

For the same reason, subtract 20 percent (multiply by 0.8) when calculating reduced delay due to a capacitive load that is less than 50 pF, external.

When comparing Xilinx numbers to those from competitors who use 35 pF as a standard load, reduce the Xilinx-specified delay by 0.4 ns, the rise time by 1.0 ns, and the fall time by 0.6 ns, thus changing both to 1.4 ns.

For an external lumped capacitive load of 200 pF, the rising-edge delay increases by 1.2 x 150 pF x 30 ps/pF = 5.4 ns over the guaranteed data sheet value.

The rising-edge transition time increases by 1.2 x 150 pF x 60 ps/pF = 10.8 ns over the 50-pF transition time of 2.4 ns. The rise time is thus 13.2 ns. ◆