Xilinx DSP LogiCORE Advantages

The Xilinx CORE Generator, in conjunction with the XC4000XL segmented architecture, automatically produces highly efficient DSP designs that are predictable for any size device. Xilinx is the only FPGA supplier that can achieve this.

In the past, high-level VHDL designs (originally intended for gate arrays) could be used in FPGAs, but they produced inefficient, slow, and unpredictable results. Now, using the DSP LogiCOREs that are created from your design specifications, you can get performance and density that is equivalent to hand crafted designs.

In addition to logic design, the CORE Generator also produces a physical layout for each parameterized core, containing relative placement information for each CLB. Once the CLBs are mapped and placed relative to each other, multiple cores can be dropped into a Xilinx FPGA and still meet the predefined performance specifications of each individual core. This is made possible by our unique segmented routing architecture.

Xilinx is the only FPGA manufacturer that produces a physical layout in parallel with the core logic design. Our competition uses cores that must rely on the place and route software to build the physical design each time they are used. And, their non-segmented routing architecture means you cannot predict performance, which decreases as more logic is added to a device and varies between different software runs, as shown in **Figure 1.**

The Xilinx core performance is also independent of device size. For example, a 12x12 parallel multiplier achieves the same maximum clock rate when it's used in an XC4005XL as when it's used in an XC4085XL. Our competitor's non-segmented architecture cannot achieve this because their metal interconnections get longer as the device size increases, as illustrated in **Figure 2**. Because of this, our competitor's core performance cannot be specified or controlled during the design phase; you must wait until the design is completed to determine if your system requirements were met. The Xilinx segmented routing does not have this problem and therefore timing is always predictable, as illustrated in **Figure 3.**

Xilinx CORE Solutions and the new CORE Generator, provide predictable, consistent, high-performance designs that get your product to market in the least time with the least effort. See our *CORE Solutions Data Book* for more information. ◆

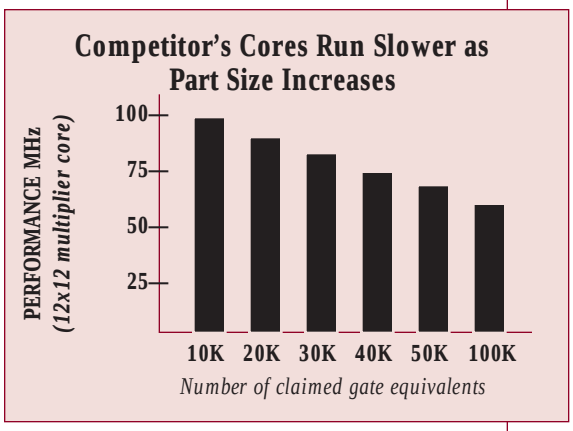

Figure 1: *Our competitor's FPGAs exhibit performance degradation as the device size grows, due to the increased capacitance of long non-segmented interconnections.*

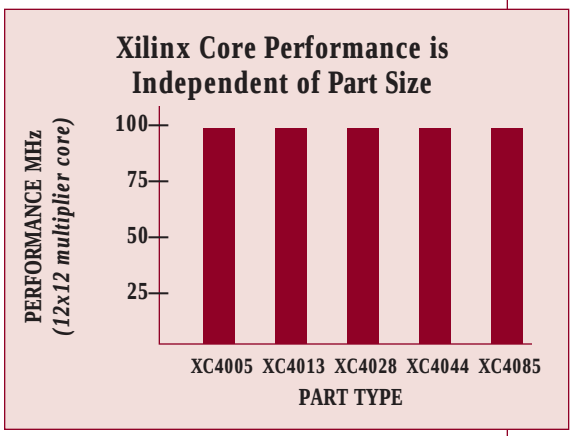

Figure 2: *The Xilinx segmented routing guarantees consistent performance as more logic is added.*

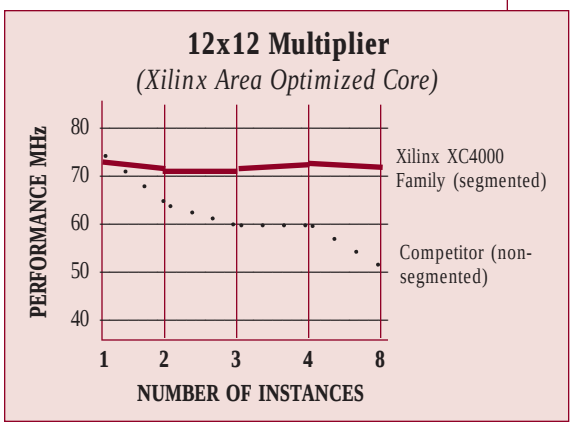

Figure 3: *Segmented routing and the Xilinx CORE Generator guarantee consistent performance between small and large FPGAs*