PLDs, Pins, and PCBs: The Importance of Pin-Locking and Footprint Compatibility

XBRF 004 November 19, 1996 (Version 1.1) Application Brief

Summary

The ability to maintain fixed I/O pin locations during PLD design and to migrate designs between footprint-compatible PLDs of varying densities helps isolate printed circuit board design from logic changes within the PLD device, thereby accelerating time-to-market and accommodating design changes throughout a product's life.

Xilinx Family

All

Introduction

Change is inevitable. The best system designers recognize this axiom and incorporate tolerance for change into their schedules, design methodologies, and even the physical realizations of their designs.

Changes can occur during all stages of a product's life cycle. Surveys suggest that as much as 50% of the typical product's development time is spent in the debug/modify/re-implement cycle that occurs after the first prototype is created. Even if the designer is skilled (and lucky) enough to create a working prototype on the first try, the product specification can change in the meantime in response to changing market conditions. In some cases, products that already have been produced and sold for months or even years have been modified to add features to extend the product's life or to correct some previously undetected flaw.

Tolerance of change is one of the prime attractions of programmable logic devices. With PLDs, design changes can be implemented quickly and easily, especially as compared to custom and semicustom IC technology. However, when it comes to tolerating changes, printed circuit boards (PCBs) are more like custom ICs than PLDs. To modify a PCB, new drawings (masks) must be created, and new prototypes must be manufactured, with all the associated expenses and delays.

Thus, to garner the true benefits of the adaptability of programmable logic, programmable logic device architectures should isolate the PCB design from logic changes that occur within the device. As a result, two concepts that should be of primary concern to PLD users are pin-locking and footprint compatibility.

Pin-Locking

Pin-locking refers to the ability to establish a fixed pin location for all the signals entering and leaving a PLD so that the PCB layout, in turn, can be fixed. Since PCB design and production is often a critical path in product development, most designers would prefer to lock PLD pin locations early in the design cycle. However, with some PLDs, this can be a risky proposition; the chosen pinout may prove to be less than optimal after the implementation of the inevitable design changes, leading to decreased performance, or, in the worse case, a design that cannot be implemented at all due to routing limitations within the PLD. Designers that used the earliest generations of CPLDs and FPGAs may recall that PLD manufacturers routinely warned their users not to begin their PCB design until the PLD design was completed and debugged. This reputation, established in the early days of high-density PLDs - that is, that design changes can be difficult or impossible to implement without changing the device pinout - lingers on today (and deservedly so, for some of our competitors' offerings!).

However, those days have long passed for Xilinx FPGA and CPLD devices.

Pin-locking is not an issue with Xilinx CPLDs. The XC7300 and XC9500 CPLD families offer the ultimate in pin-locking capability, with 100% connectivity through the CPLD's internal switch matrix. Thus, any I/O pin can be connected to any function block input or output, regardless of utilization levels. Design changes internal to the CPLD will seldom force pinout changes.

While the Xilinx FPGA families cannot provide the same guarantee of full connectivity offered by the Xilinx CPLDs, the latest generations do provide a high degree of flexibility in their I/O connections. All recent Xilinx FPGA architectures, including the XC5200, XC4000E, XC4000EX, and XC6200 families, embrace the "VersaRing" concept introduced in the XC5200 family. Simply put, these FPGAs include an extra layer of routing resources along the perimeter of the logic array to increase routing flexibility between the internal array and the I/O blocks. User feedback is confirming that these devices deliver on the promise of allowing last-minute design changes without changes to the I/O pin locations.

Actually, this capability also is present to a large degree in the "older" XC4000 series FPGAs. The popular XC4000 family was the subject of an independent research study

that examined pin-locking in FPGA architectures. As reported at the 3rd Canadian Workshop on Field-Programmable Devices (May, 1995), researchers at the University of Toronto implemented sixteen different designs in XC4000 devices. The designs were first routed with no placement constraints, then with "bad" pin constraints (wherein signals that were assigned to adjacent pins in the unconstrained design were now assigned to opposite ends of the device), and, lastly, with a randomly-generated pin placement. In every case, the designs routed to completion, albeit with a slight performance impact; the average signal delay increase was less than 5% for the "bad" constraints and 3% for the random constraints. Significantly, the researchers concluded that "For the Xilinx XC4000 series, there are sufficient tracks per channel to achieve good routability. Fixed pin assignment does impact routability significantly, because the amount of routing resources used was increased, but the Xilinx XC4000 series architecture provided sufficient resources to handle the increased demand." Incidentally, the Altera FLEX 8000 family - the only other device included in the study - did not fare nearly as well; several designs were unroutable with bad or random pin constraints, and the researchers recommended that users of FLEX FPGAs "should leave about 20% of the logic elements and I/O pins free to avoid routability problems due to pin constraints." Table 1 summarizes the results of the University of Toronto study.

Table 1: Results of the University of Toronto Study

	Xilinx XC4000 Family	Altera FLEX 8000 Family
Number of benchmark circuits[1]	16	14
% of designs fully routed with "bad" pin placement constraints	100%	86%
% of designs fully routed with "random" placement constraints	100%	79%
Average increase in path delays – "bad" constraints	5%	3.6%
Average increase in path delays – "random" constraints	3%	3%

Note: 1. Two benchmark circuits included on-chip memory and were implemented in the XC4000 family only

Thus, while "intelligent" placement of I/O pins is still recommended, Xilinx FPGA and CPLD devices are quite tolerant of design changes without forcing the redesign of the PCB layout. This facilitates an early release of the PCB design and eases the debugging process, thereby accelerating time-to-market, as well as accommodating changes that may occur later in the product's life.

Footprint Compatibility

Footprint compatibility is an equally important feature for maximizing the flexibility of PLD designs, and has been incorporated in all Xilinx component product lines since the introduction of our first products - the XC2000 family, the world's first FPGAs. Footprint compatibility refers to the availability of PLDs of various gate densities with the same package and with an identical pinout. When a range of footprint-compatible devices is available, users have the ability to migrate a given PLD design to a higher or lower density device without changing the printed circuit board.

There are several scenarios where a common device footprint provides a significant advantage. The most prevalent of these is when a design is being modified to add features without changing the pinout requirements, and, as a result, the design grows to exceed the gate density of the PLD device that was initially selected. By moving the design to a footprint-compatible device with higher capacity, a re-layout of the printed circuit board is avoided, saving both time and money.

On the other hand, a design can be initially prototyped in a larger device than needed, to allow room for expansion and experimentation. Once the design is fixed, it can be migrated to a smaller, less-expensive device in the same package as a cost reduction. Again, footprint compatibility between the devices avoids changes to the printed circuit board. (There is, however, one caveat to consider when migrating a design from a larger to a smaller PLD device. For some smaller devices, the package may have more physical pins than there are input/output pads on the device. Thus, some package pins may be left unconnected. A larger device in the same family may have more I/O pads on the die and, therefore, have connections to all the pins of the given package. Thus, if migration to a smaller part is anticipated, the initial design in the larger device should avoid using those pin locations that are not connected in the smaller device.)

In other words, footprint compatibility lessens any risks associated with the initial device selection, which often must be based on a rough estimate of the design's requirements. If the selected device turns out to be too small, the design is migrated to a larger device. If the selected device is too big, the design can be moved to a smaller device. In either case, with footprint-compatible devices potentially expensive and time-consuming changes to the PCB are avoided.

Footprint-compatible devices also provide the user with more inventory flexibility. Devices that are on-hand can be used for prototyping or initial production, and the design can then be migrated to a footprint-compatible device for quantity production. If a sudden demand 'upside' should develop, users have the option to move to a larger device in the same family or a similar-sized device from another footprint-compatible family.

Recognizing these benefits, Xilinx always has maintained footprint compatibility within component product families and sub-families whenever multiple devices share common packages. For example, the XC3030 and XC3042 share a common footprint in the PC84, PQ100, TQ100, and VQ100

packages. That same footprint is maintained in the equivalent density members of the XC3000A, XC3000L, XC3100A, and XC3100L sub-families. (The only exceptions are the XC3000 series and its derivatives in the PC 84 package, where some of the larger devices need two additional GND and VCC connections, and in the PQ208 package, where the XC3090 and XC3195 do not have compatible footprints.)

In the newer generations of Xilinx FPGAs, footprint compatibility even extends across product families. Members of the XC4000 series (and its derivatives), and the XC5000 series, share common footprints in common packages (Table 2). This provides designers with a wide choice of options. For example (as reported in XCell newsletter #19), VTEL Corp., a manufacturer of video teleconferencing systems and one of the first adopters of the XC5000 family, prototyped their designs in XC4000 series FPGAs while awaiting the availability of XC5000 components and development tools. The resulting designs were easily migrated to lower-cost, footprint-compatible XC5000 devices for production systems.

In a similar manner, members of the XC7000 and XC9500 CPLD families share common footprints in common packages.

Designers should avoid getting locked into programmable logic solutions that offer little flexibility in pin assignments and device selection. Xilinx CPLDs and FPGAs offer the best pin-locking capabilities in the industry, and the broadest spectrum of footprint-compatible devices. These features allow users to avoid modifications to printed circuit board designs, thereby accelerating time-to-market and accommodating the inevitable design changes that occur throughout a product's total life cycle.

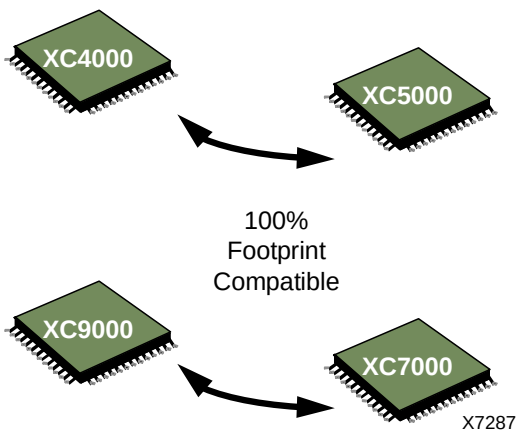

Figure 1: Package Footprints are 100% Compatible

Table 2: Footprint Compatible Members of the XC4000E and XC5200 FPGA Families

Package	XC4000E Family	XC5200 Family
84-pin PLCC	XC4003E XC4005E XC4006E XC4008E XC4010E	XC5202 XC5204 XC5206 XC5210
100-pin PQFP	XC4003E XC4005E	XC5202 XC5204 XC5206
100-pin VQFP	XC4003E	XC5202 XC5204 XC5206
144-pin TQFP	XC4005E XC4006E	XC5202 XC5204 XC5206 XC5210
156-pin PGA	XC4005E XC4006E	XC5202 XC5204
160-pin PQFP	XC4005E XC4006E XC4008E XC4010E XC4013E	XC5204 XC5206 XC5210 XC5215
191-pin PGA	XC4008E XC4010E	XC5206
208-pin PQFP*	XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E	XC5206 XC5210 XC5215
225-pin BGA	XC4010E XC4013E	XC5210 XC5215
240-pin PQFP*	XC4013E XC4020E XC4025E	XC5210 XC5215
299-pin PGA	XC4025E	XC5215

* includes both PQ and HQ packages

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