**I use Workview Office, but I don't like having to go to DOS or the EDIF Interfaces GUI to run the required programs for implementation and simulation. Is there any way to simplify these flows?**

Yes. The Tools menu in ViewDraw can be customized to include Xilinx-specific functionality. For example, when this command is run from a DOS session:

```
custmenu
 %XILINX%\viewlog\data\viewblox.txt
```

Two new commands appear in the Tools menu:

✔ Add LogiBLOX

✔ Change LogiBLOX

Three more Xilinx-specific commands can be added to the ViewDraw Tools menu. A file containing these commands, **xvdrawm1.zip**, can be found at: ftp://ftp.xilinx.com/pub/swhelp/viewlogic

or at:

http://www.xilinx.com/techdocs/htm_index/sw_viewlogic.htm.

Within this ZIP file are two script (.txt) files, an executable (**vfuncsim.exe**), and a **readme.txt**. After following the instructions in the **readme** file, open ViewDraw and check the **Tools** menu. In the **User** section, you will see three new commands:

✔ **Write Xilinx EDIF** – This command allows you to run **EDIFNETO** without going to the EDIF GUI or to DOS. It includes the **Level=Xilinx** property required for Xilinx designs.

✔ **Xilinx Functional Simulation** – This command prepares a **FUNC_SIM.VSM** file for simulation. This is necessary for designs with RAM, ROM, or instantiated netlists.

✔ **Read Xilinx Timing EDIF** – This command imports **TIME_SIM.EDN**, produced by the Design Manager in preparation for a timing simulation.

Reference solution # 1985: http://www.xilinx.com/techdocs/1985.htm

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**I've upgraded to Workview Office 7.4, and now I see errors when reading a timing simulation EDIF file back into Viewlogic for simulation. What's going on?**

**EDIFNETI** is the Viewlogic program that will read an EDIF netlist back into the Viewlogic realm as part of the simulation flow. A change was made with the 7.4 version of this tool, and the following error may been seen as a result:

```
viewbase: Error 413: Error -
 Schematic Pin Z on XBA1.1 is
 not on its symbol...
```

This message repeats for each pin mismatch it finds. This error occurs due to an increased level of error checking within **EDIFNETI**.

**Solution** — Viewlogic has built a patch to return to the functionality of version 7.31. This patch is located at:

ftp://ftp.viewlogic.com/pub/support/pc/Workview_Office/update/edfupdt1.exe

Viewlogic's readme for this patch is located at:

ftp://ftp.viewlogic.com/pub/support/pc/Workview_Office/update/edifneti.html

Also, when reading hierarchical EDIF into Viewlogic, do not name any port on a symbol the same as the symbol itself. To avoid any conflict, **EDIFNETI** changes the name of that port, potentially causing problems with annotation to the original schematic.

Reference solution # 3081: http://www.xilinx.com/techdocs/3081.htm

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