Increased Design Portability with XACT*step* Version M1

The Xilinx XACT*step* version M1 software technology enables users at every design level to increase optimization, manage design changes, and quickly complete designs with the entire spectrum of Xilinx FPGA and CPLD devices. For example, the version M1 tools are designed to support multiple device architectures using the same core physical implementation (i.e., map, place and route) software. To implement this capability, a new program has been introduced into the design flow: **NGDBuild**.

NGDBuild is responsible for two functions during the design implementation process. First, the design's elements are brought together into a single database so that subsequent operations, such as map, place and route, may be applied to the entire design at once. Second, NGDBuild re-expresses the design as a netlist of "technology-less" primitives that are common to all CPLDs and FPGAs. The components in this technology-independent library are known as "SimPrims."

NGDBuild's impact on the design is to make it instantly "re-targetable" between any of the Xilinx device architectures supported by the core software. Thus, a design's performance may be investigated in any Xilinx architecture, with little or no design rework required.

The core implementation tools (map, place and route) receive a netlist from NGDBuild that expresses the design as a netlist of SimPrims, and it's these technology-independent cells that are implemented within the target device. Consequently, the back-annotation process (that is the creation of a post-Map or post-PAR netlist describing the design's physical implementation) results in a netlist of SimPrims annotated with the appropriate block and net delay data that arises from the place and route process.

As a result of this strategy, different simulation libraries are needed to support simulation before and after NGDBuild has been applied to a design. Prior to NGDBuild, designs will be expressed as netlists containing Unified Library components. After NGDBuild, designs will be expressed as netlists consisting of SimPrims. ◆

XACT*step* M1 VHDL Design Flow

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